Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement

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Outline

- Research Objective
- Single-Bit & Multi-Bit ΣΔ TDCs
- Multi-Bit ΣΔ TDC with DWA
- Multi-Bit ΣΔ TDC with Self-Calibration
- Circuit Design
- Conclusion

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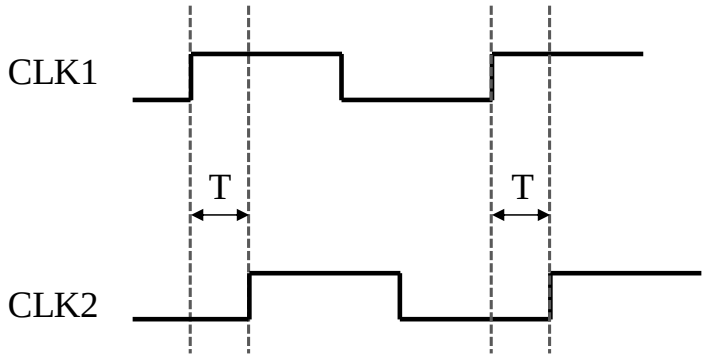
Research Purpose

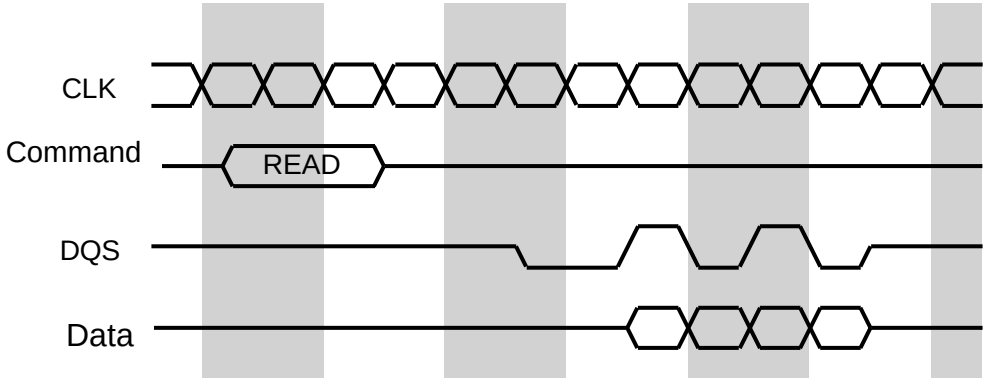
- Testing timing difference between two repetitive digital signals.

Ex.

Data and clock in Double Data Rate (DDR) memory



- Short testing time
- Good accuracy



Implemented with small circuitry

Our Work

Using Multi-bit ΣΔ Time-to-Digital Converter (TDC)

- Repetitive digital signals
  - ⇒ ΣΔ TDC can be used
- Simple circuit
- Fine time resolution

	Testing time	Linearity
Single-bit	Long	Good
Multi-bit	Short	Bad

due to delay elements mismatches

⇓

Two methods for their compensation

- Data-weighted-averaging (DWA)
- Self-calibration

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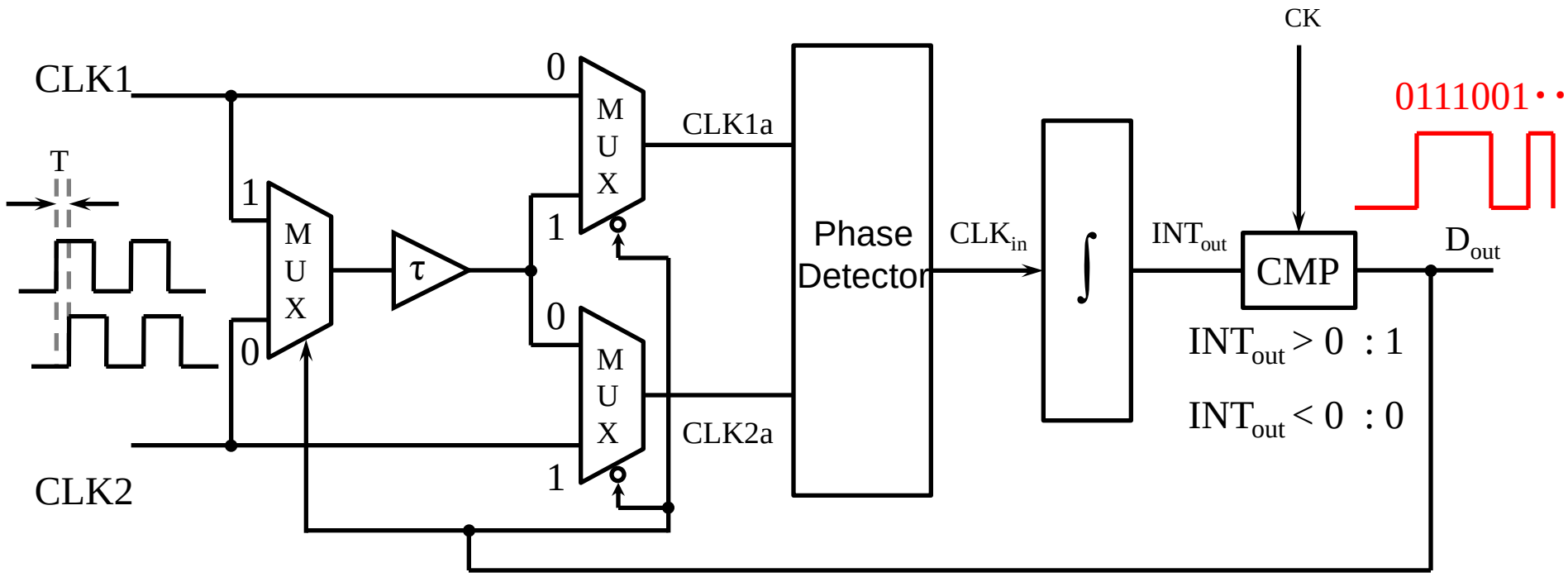
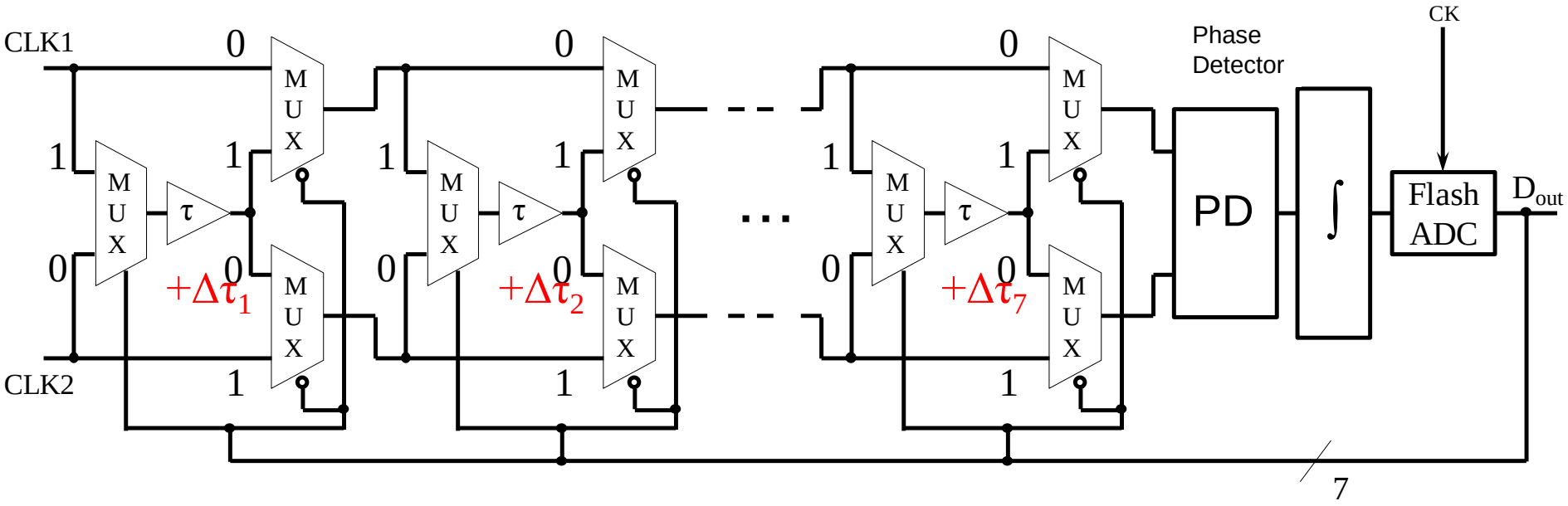
Single-Bit ΣΔ TDC



- Measurement of timing *T* between repetitive CLK1 and CLK2.
- Number of 1's at *Dout* is proportional to *T* .
- Time resolution becomes finer as measurement time becomes longer.

Multi-Bit ΣΔ TDC



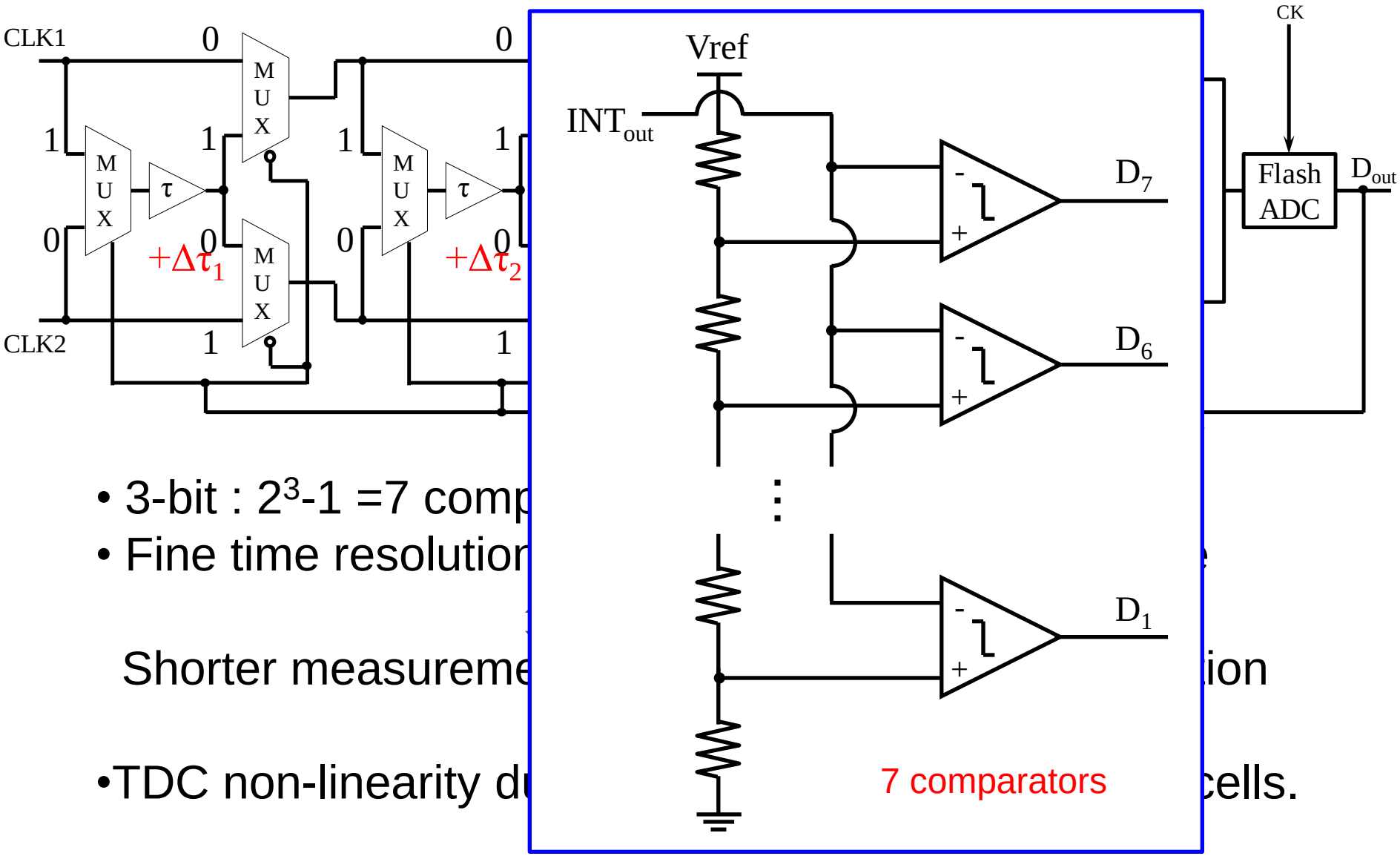
- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

⇕

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.

Multi-Bit ΣΔ TDC

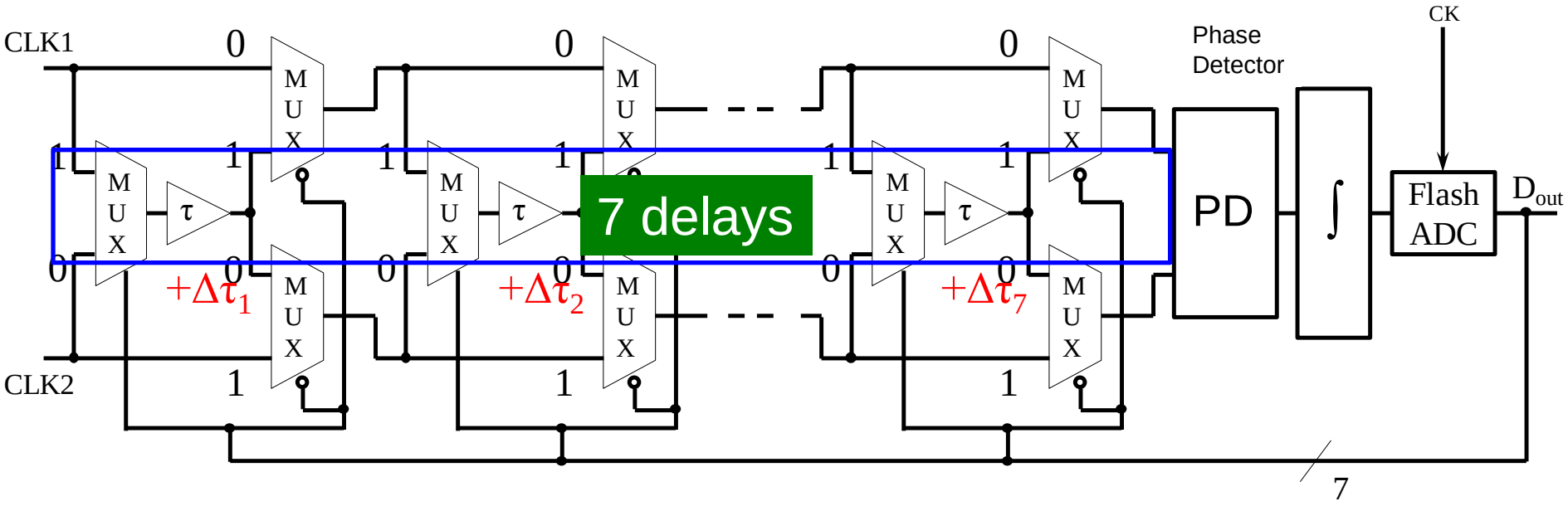


- 3-bit : 2^3-1 =7 comp
- Fine time resolution

Shorter measureme ion

- TDC non-linearity d cells.

Multi-Bit ΣΔ TDC



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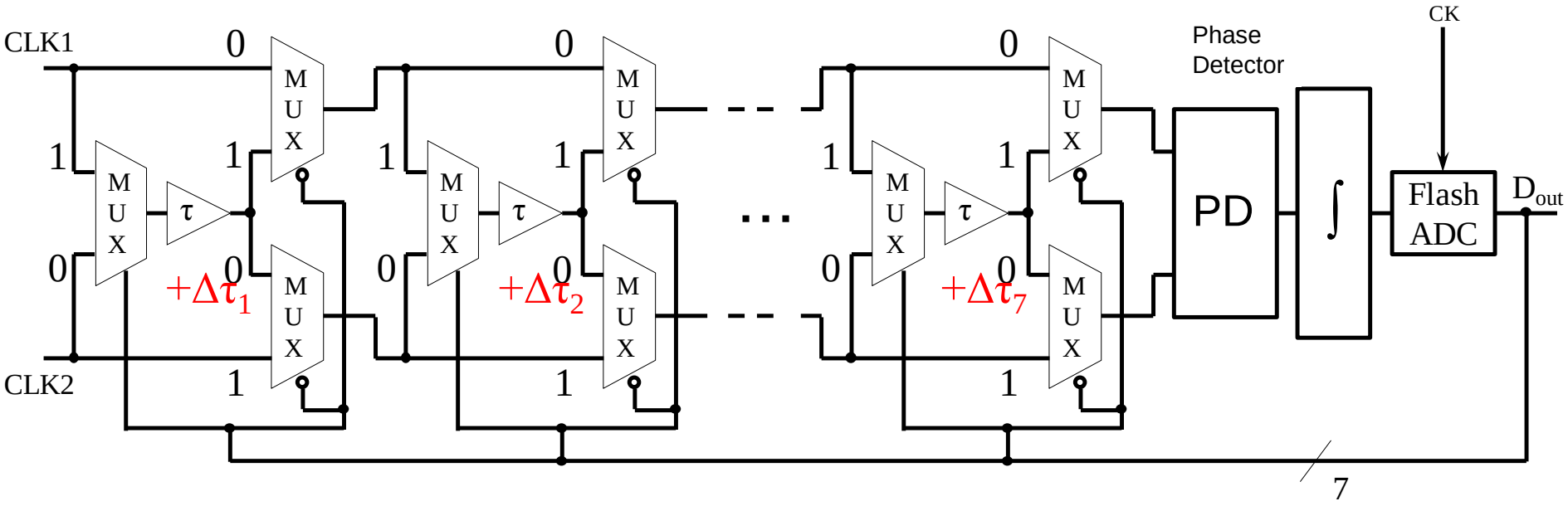
Multi-Bit ΣΔ TDC



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Shorter measurement time with a given time resolution

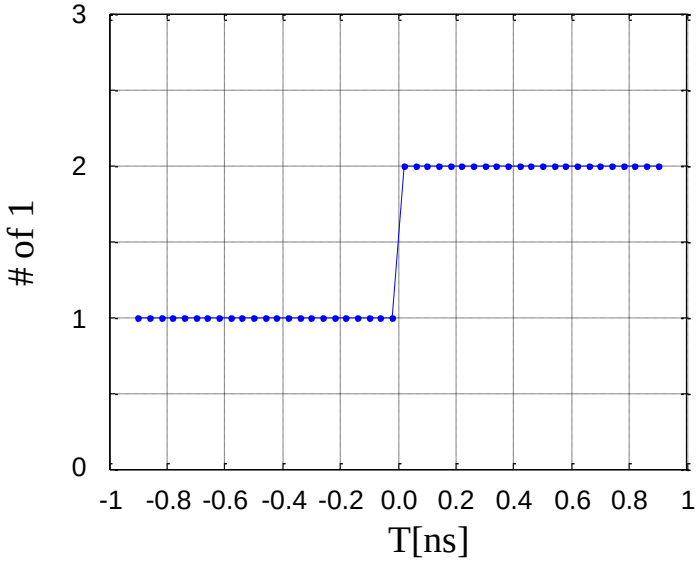
- TDC non-linearity due to mismatches among delay cells.

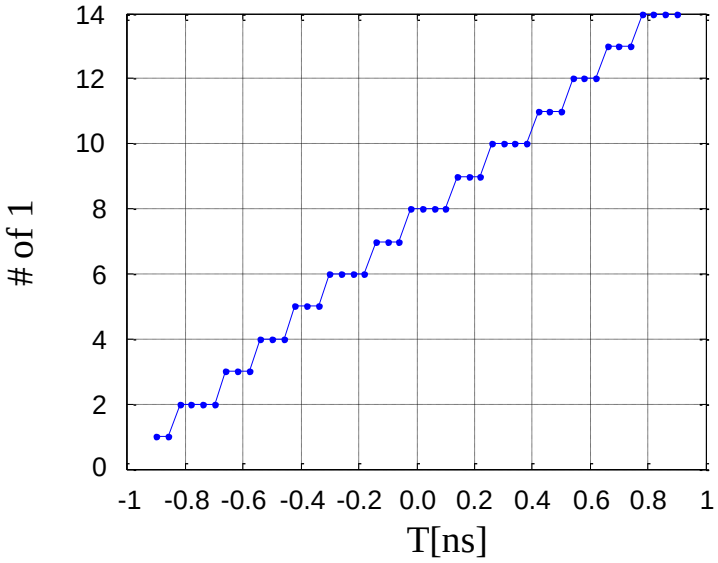
Difference in Measurement Time

- Simulation conditions

	1-bit ΣΔ TDC	3-bit ΣΔ TDC
Rising timing edge difference (T)	-0.9 ∼ 0.9ns (Resolution : 0.04ns)	-0.9 ∼ 0.9ns (Resolution : 0.04ns)
Delay time (τ)	1ns	0.145ns
The number of digital outputs	2	2

■ A rising number of outputs for the interval T





✓Multi-bit takes short measurement time for a given time resolution ⇒ **Low cost**

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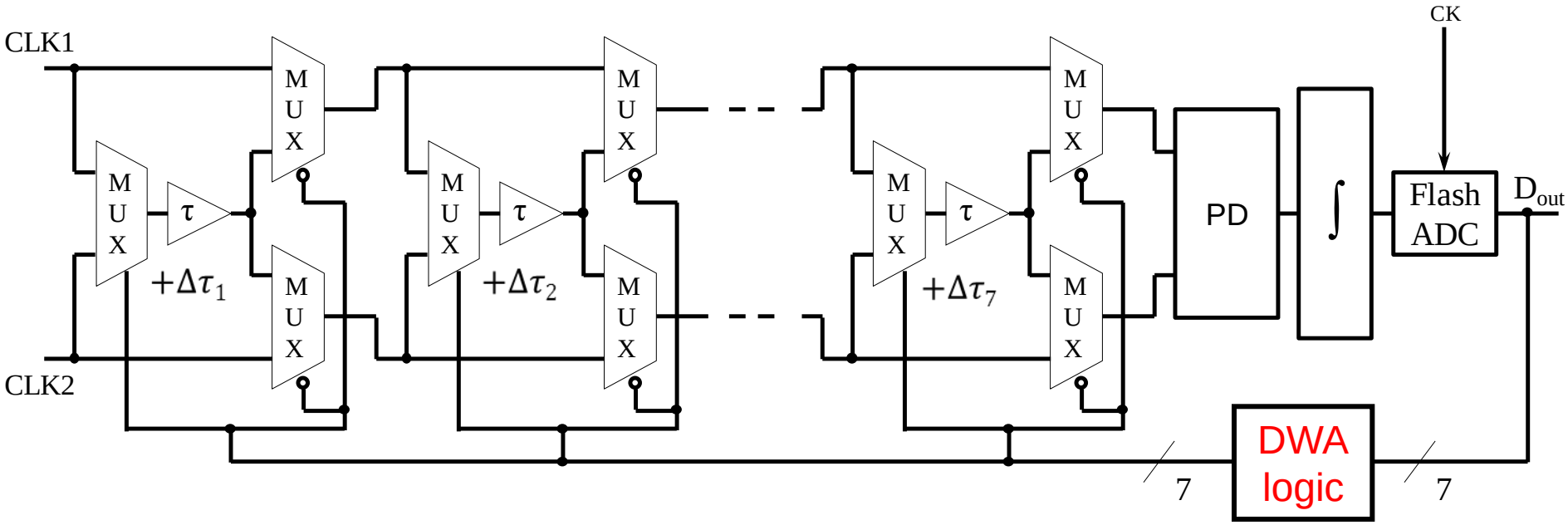
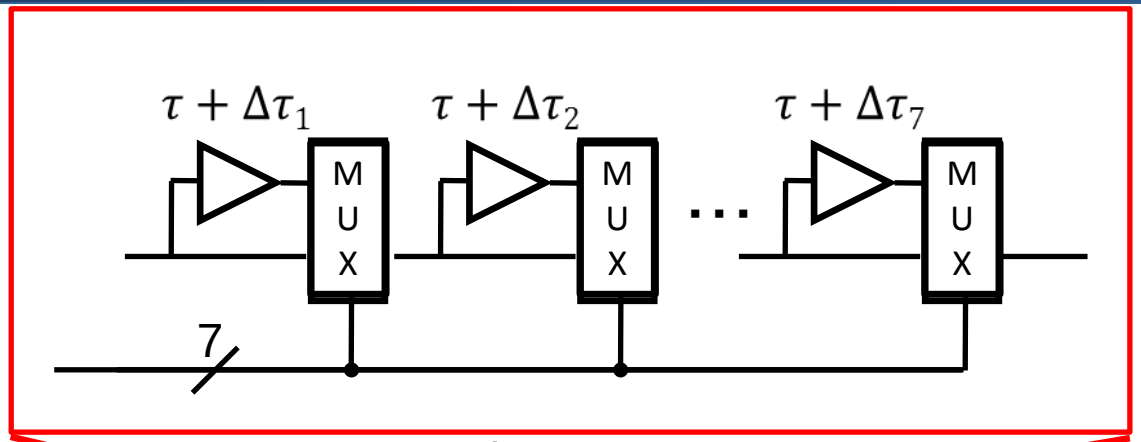
DWA (Data Weighted Averaging)

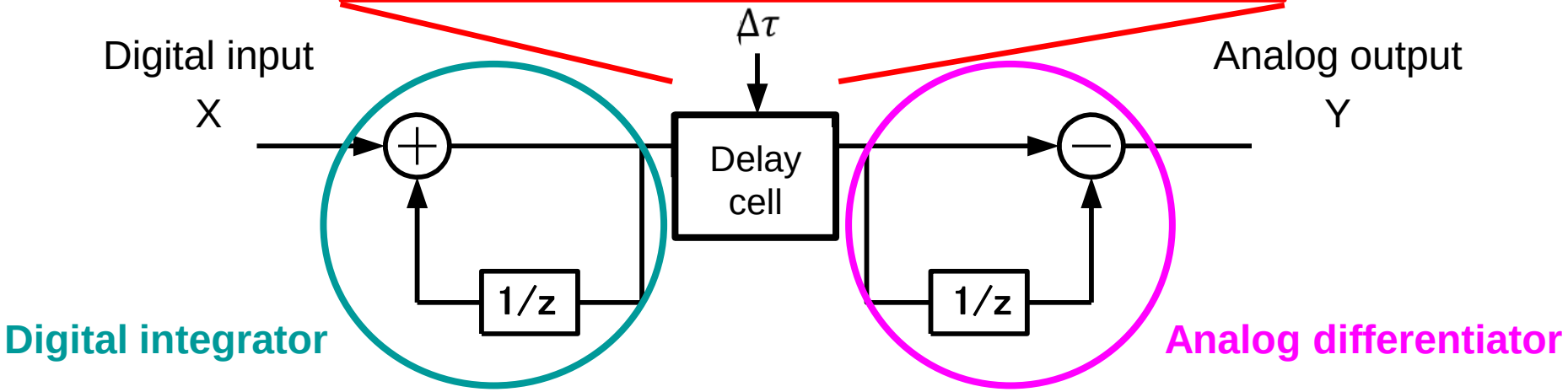


- Flash ADC outputs
  - ➡ shuffled by DWA logic, fed into MUXs as select signals

- Delay mismatch effects
  - ➡ moved to high-frequency (noise-shaping)

Noise-Shaping

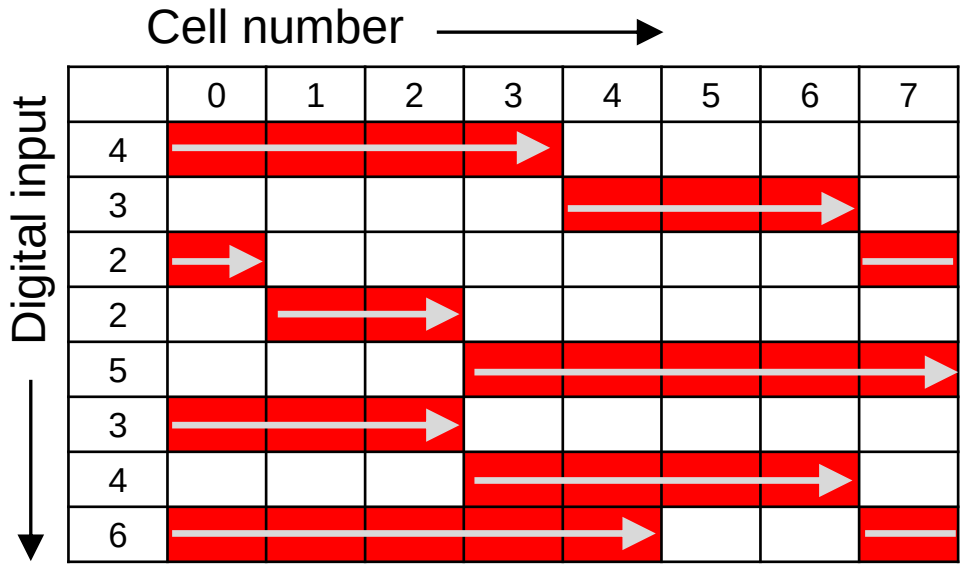




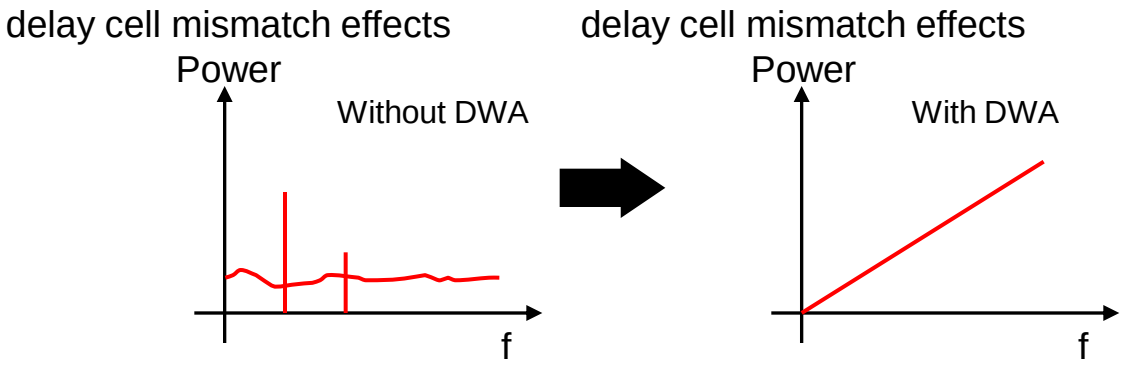
$$Y(z) = X(z) + (1 - 1/Z)\Delta\tau(z)$$

Delay mismatch $\Delta\tau$ is fist-order noise-shaping.

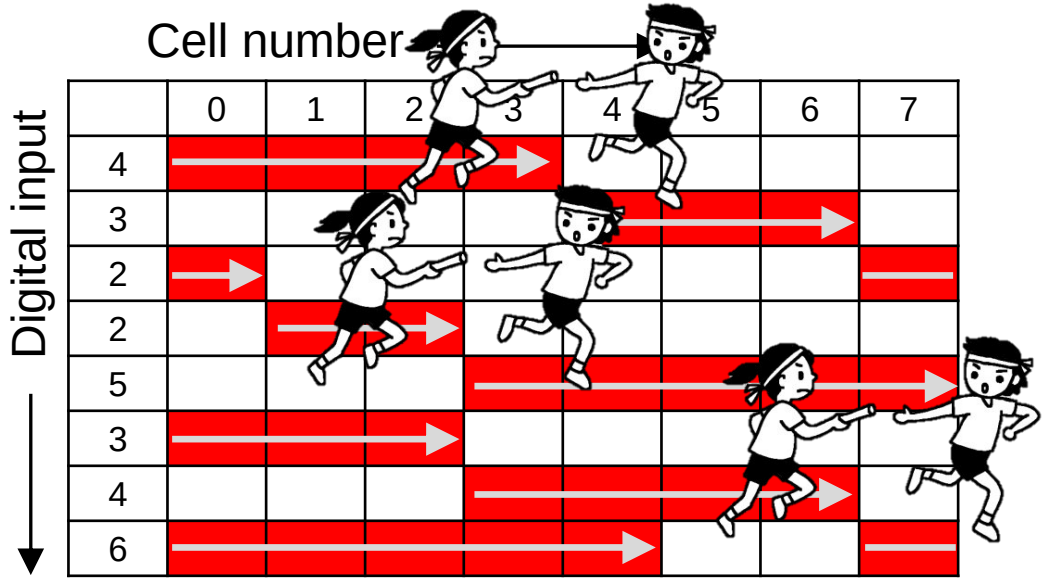
DWA & Noise Shaping



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

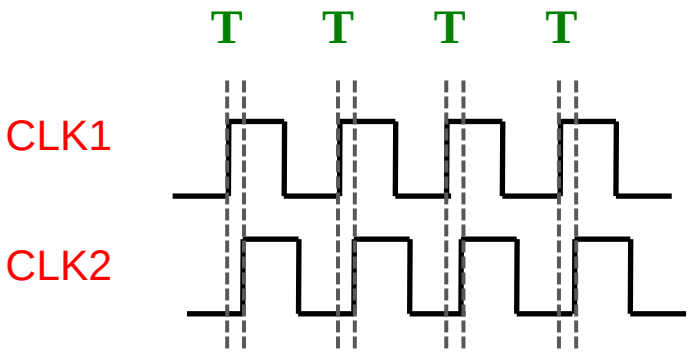


DWA Operation



Passing a baton in relay race !

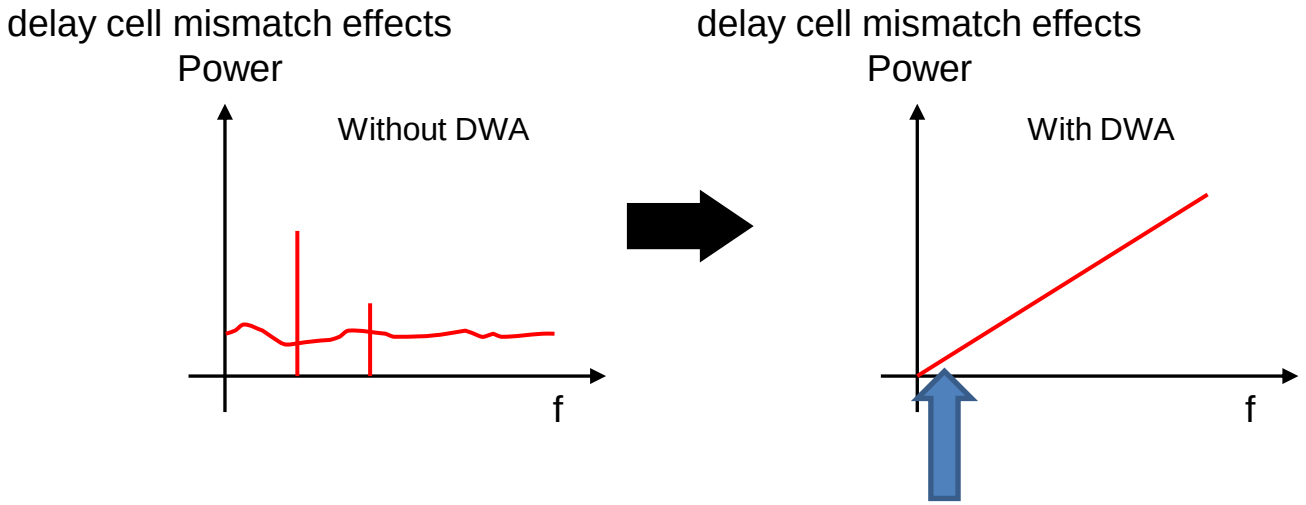
DWA Effect



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

Measure **T**

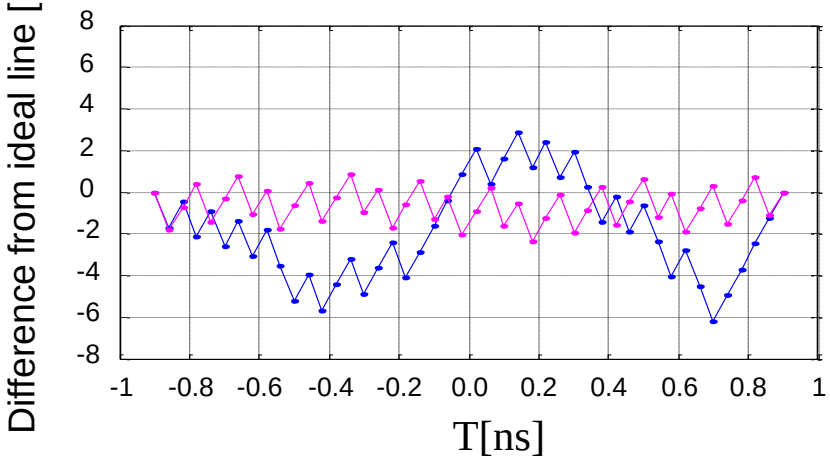
T is DC signal.



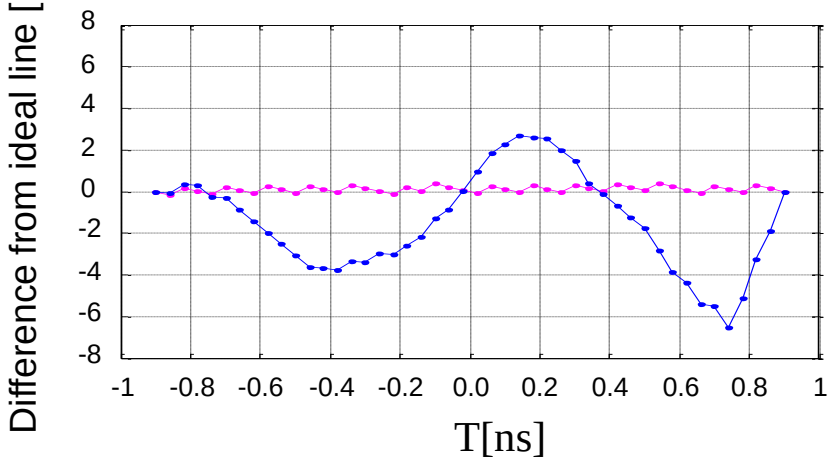
Mismatch effects reduction at DC

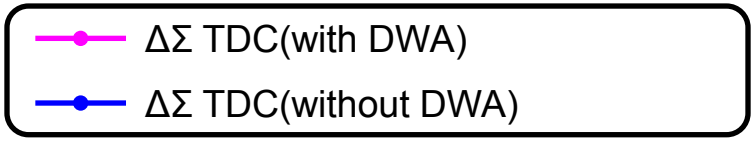
Simulation of ΣΔ TDC with DWA

- Output：99 points



- Output：599 points





✓Reduce the effect of delay mismatches.

- ΣΔ TDC linearity is improved.

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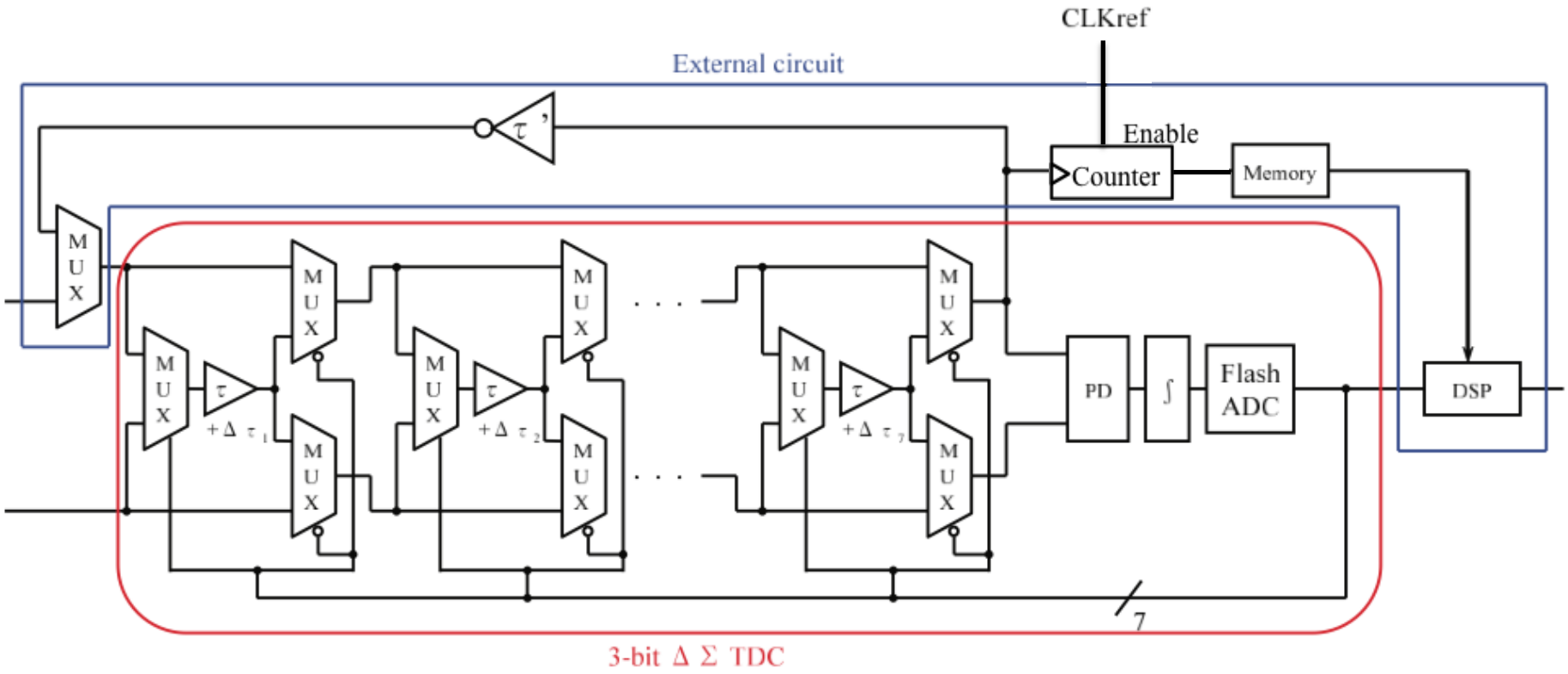
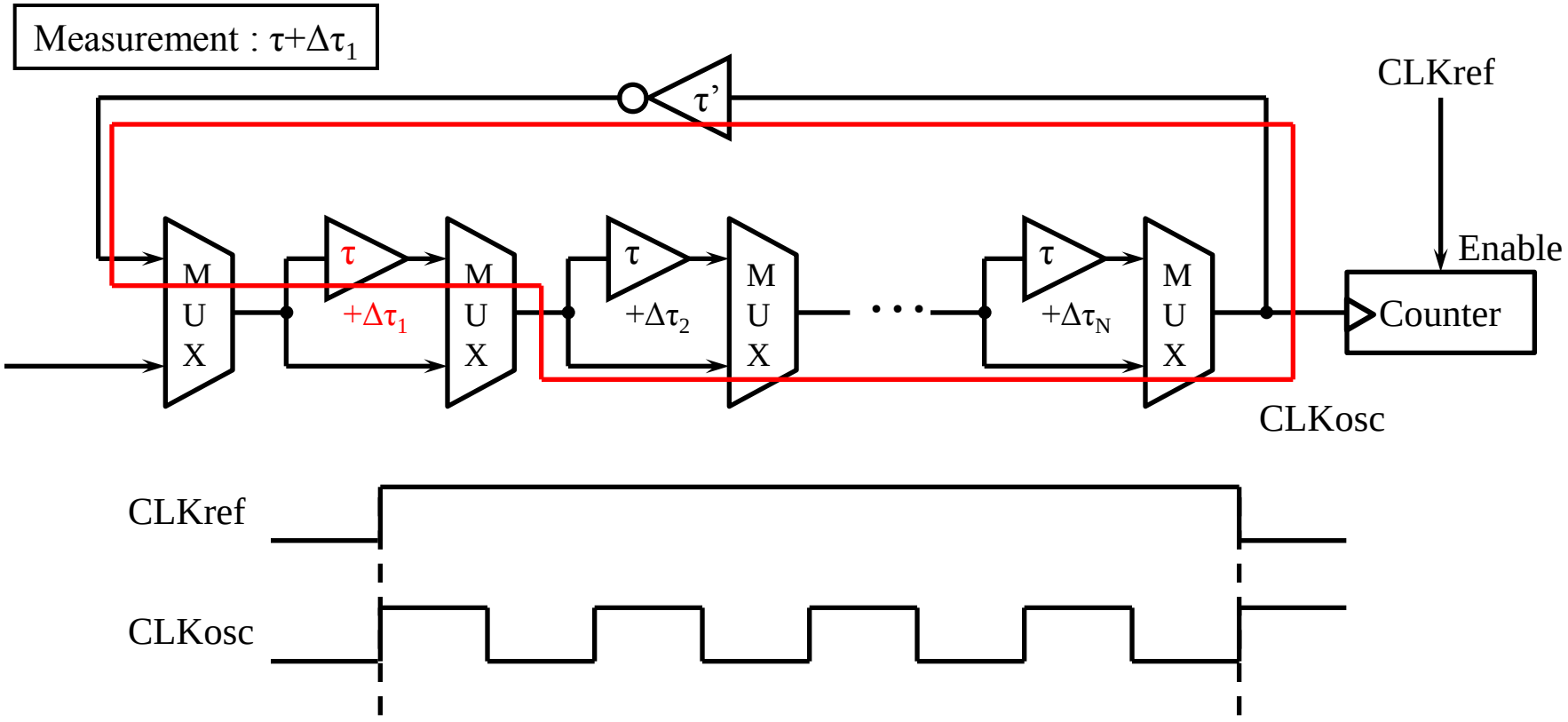
ΣΔ TDC with Self-Calibration



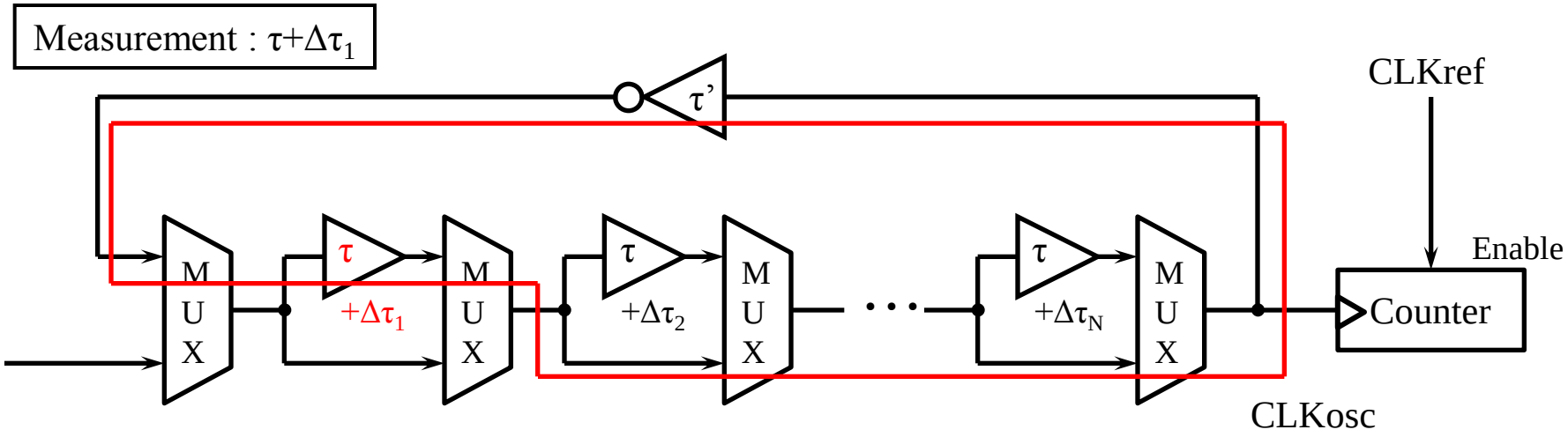
- Self-calibration circuit: inverter, MUX, counter, memory
- Measure delay values and store them in memory.

Self-Measurement of Delay

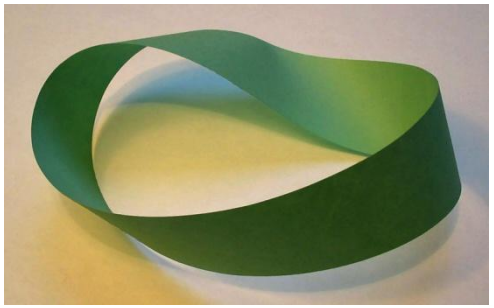


- Ring oscillator with a delay cell to be measured.
- Counter measure the number of the pulses.
- $\Delta\tau_1$ can be calculated.
- Measured delay values are stored in memory.

Time Signal & Ring Oscillator

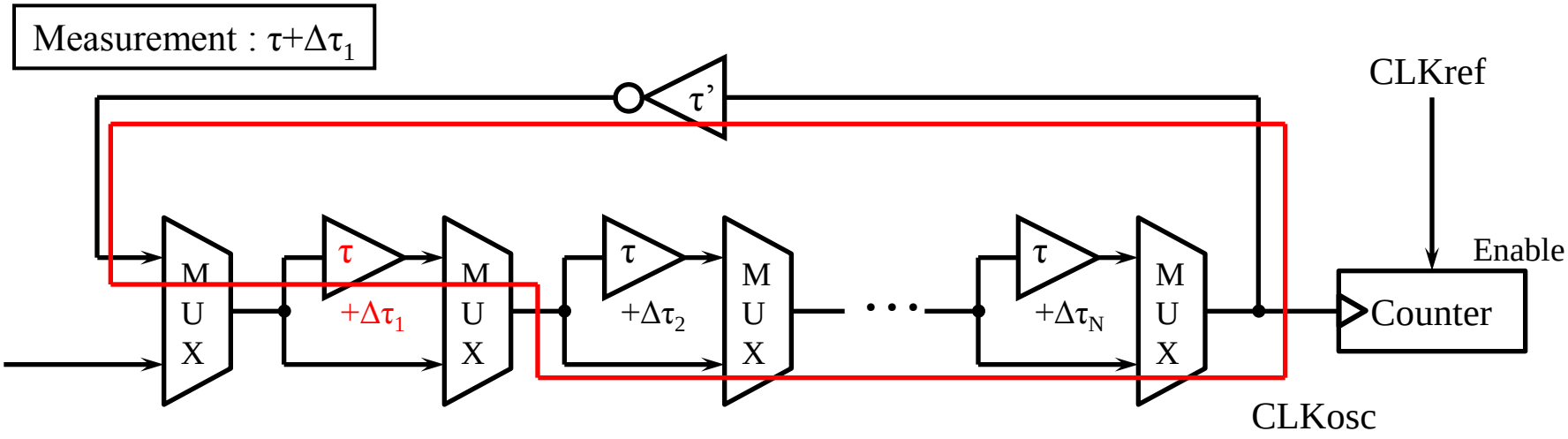


Ring oscillator



Möbius strip

Self-Measurement of Delay



Oscillation frequency

$$f = \frac{1}{2\left(\tau' + \tau + \Delta\tau_1\right)}$$

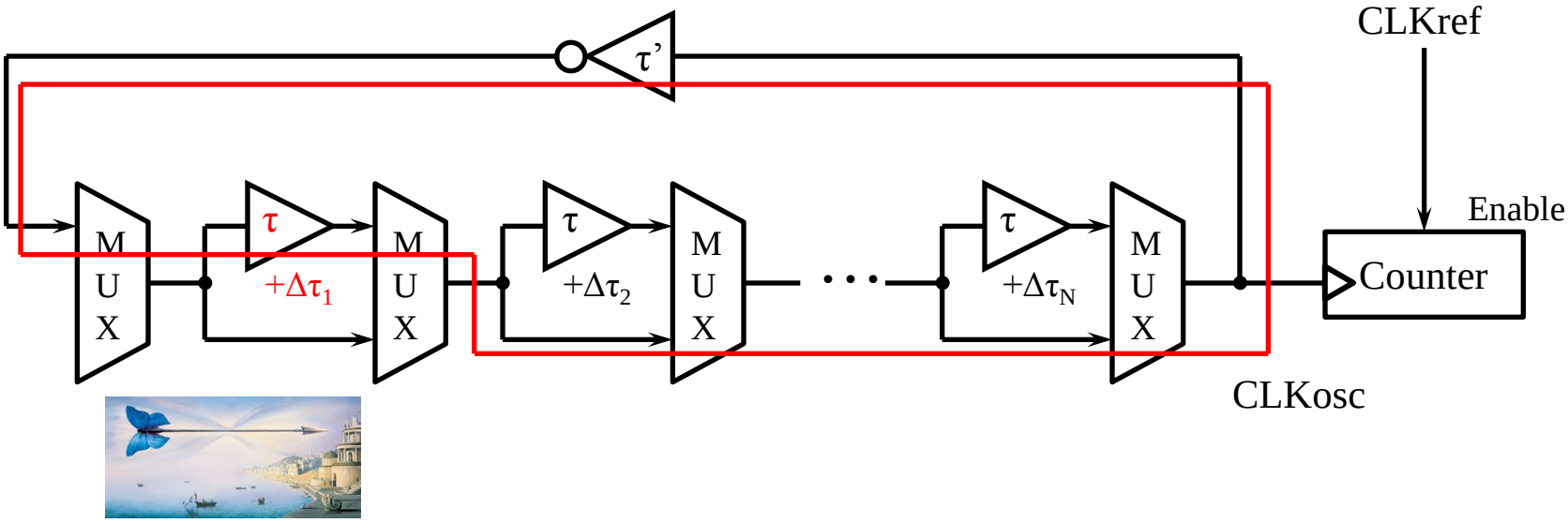
Measure $\Delta\tau_2, \Delta\tau_3, \Delta\tau_4, \ldots \Delta\tau_N$ one by one.

$\Delta\tau_1$ can be calculated from the oscillation frequency

Essence of Proposed Method

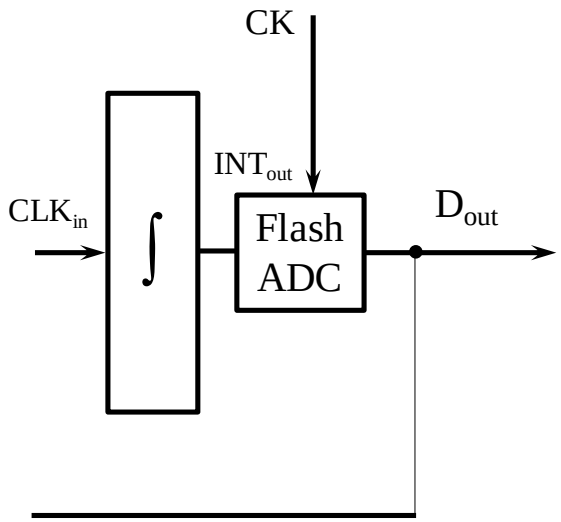
- All operations are done in digital domain.
- Signal is Time instead of Voltage.

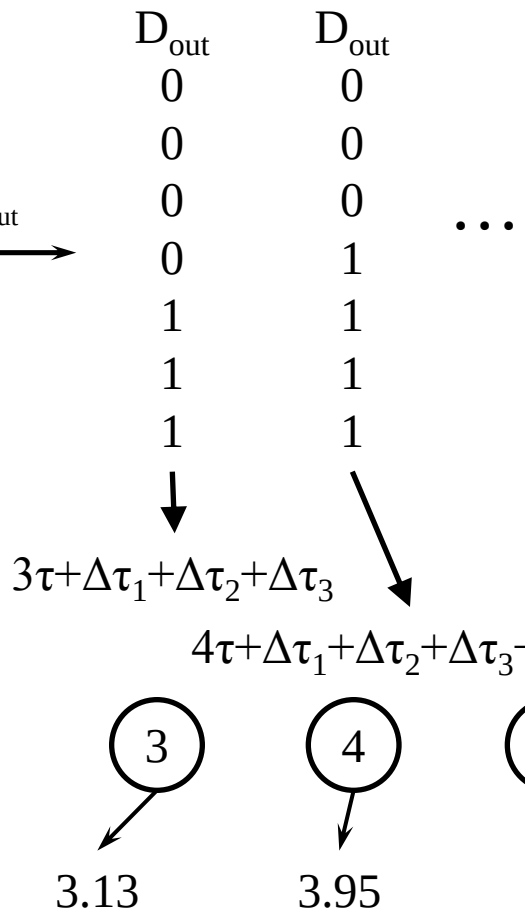
  ⇒ Easy, accurate measurement of $\Delta\tau$

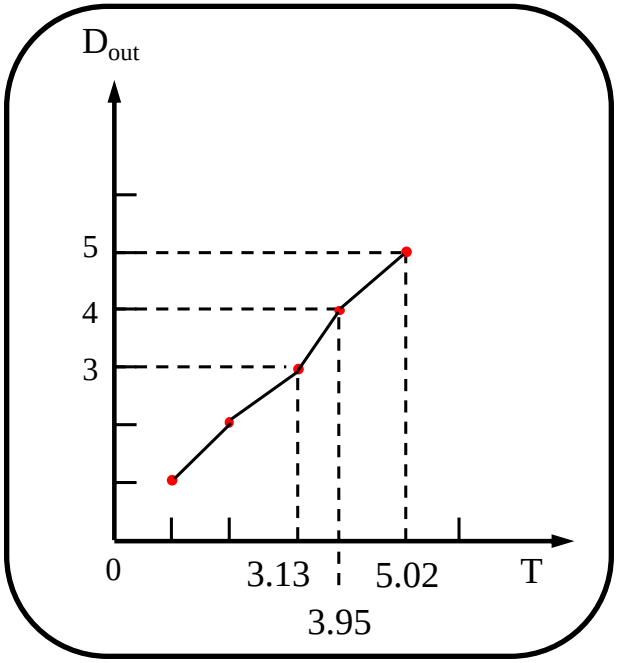


Time flies like an arrow!

Proposed Error Correction Scheme



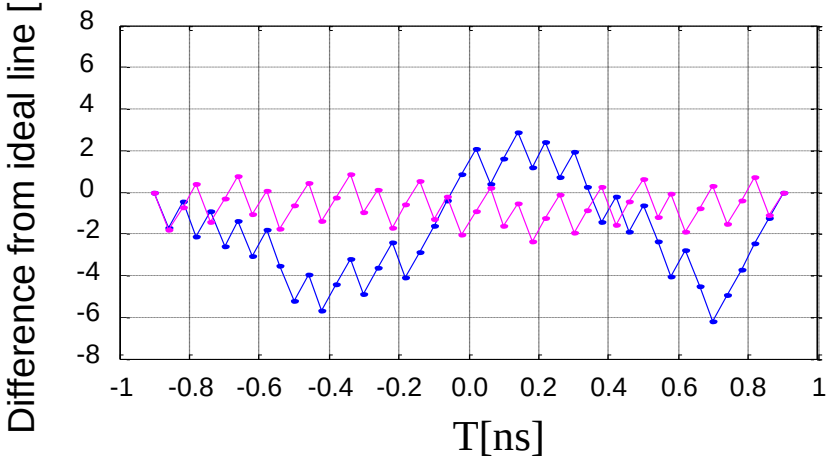




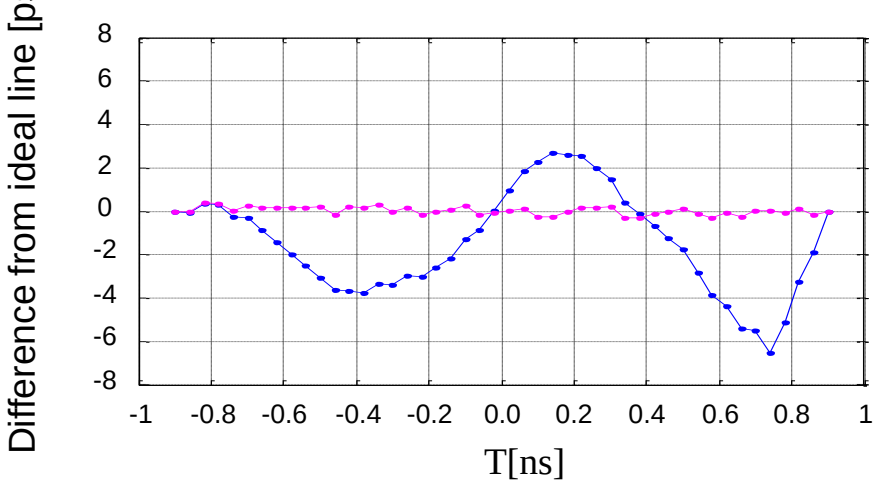
- Obtain TDC raw output (Dout) for two input clocks.
- Read delay values from memory,
  and compensate for the output based on them.

Simulation of Self-Calibration

● Output：99 points



● Output：599 points



ΔΣ TDC(with Self-Calibration)

ΔΣ TDC(without Self-Calibration)

ΣΔ TDC linearity is improved.

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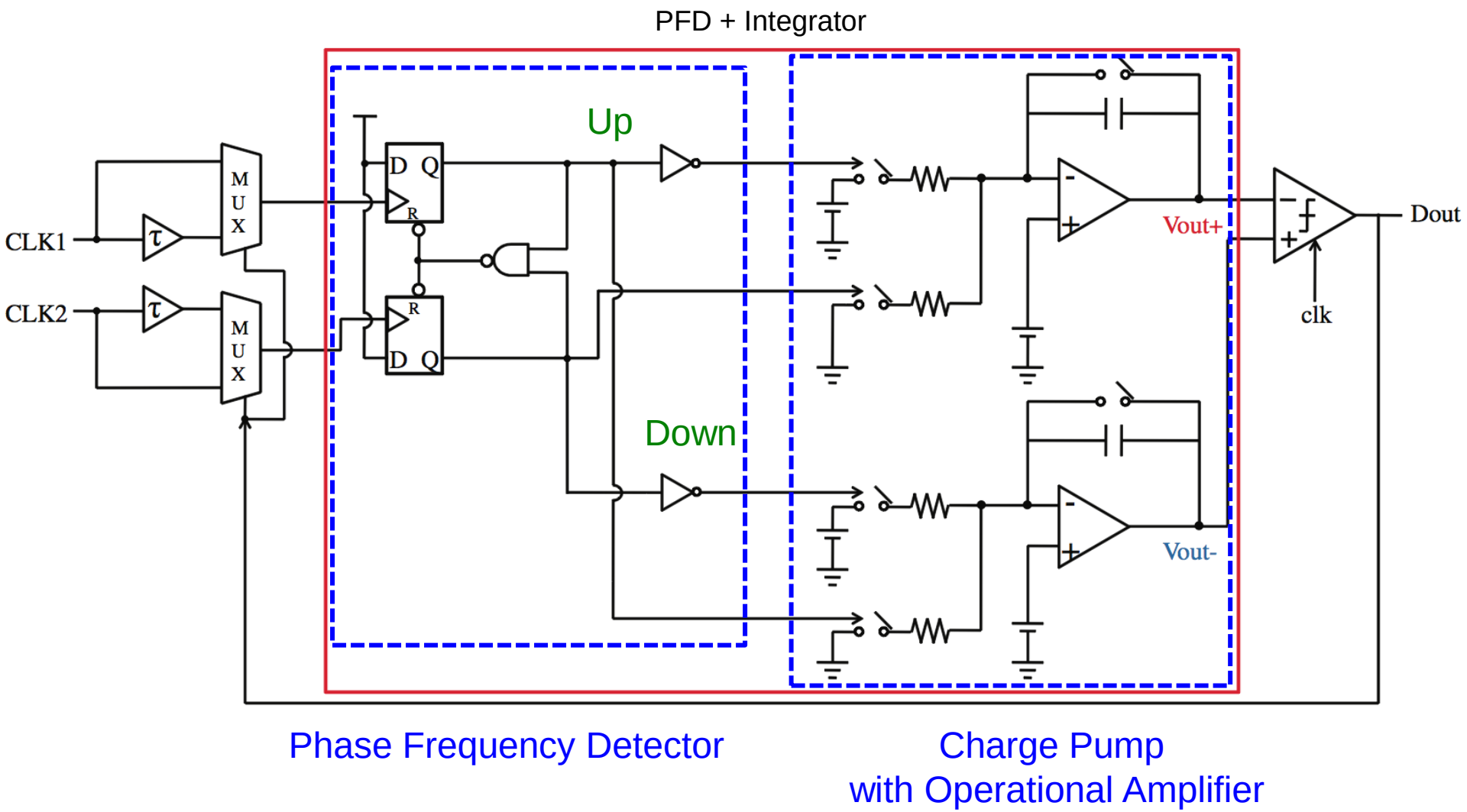
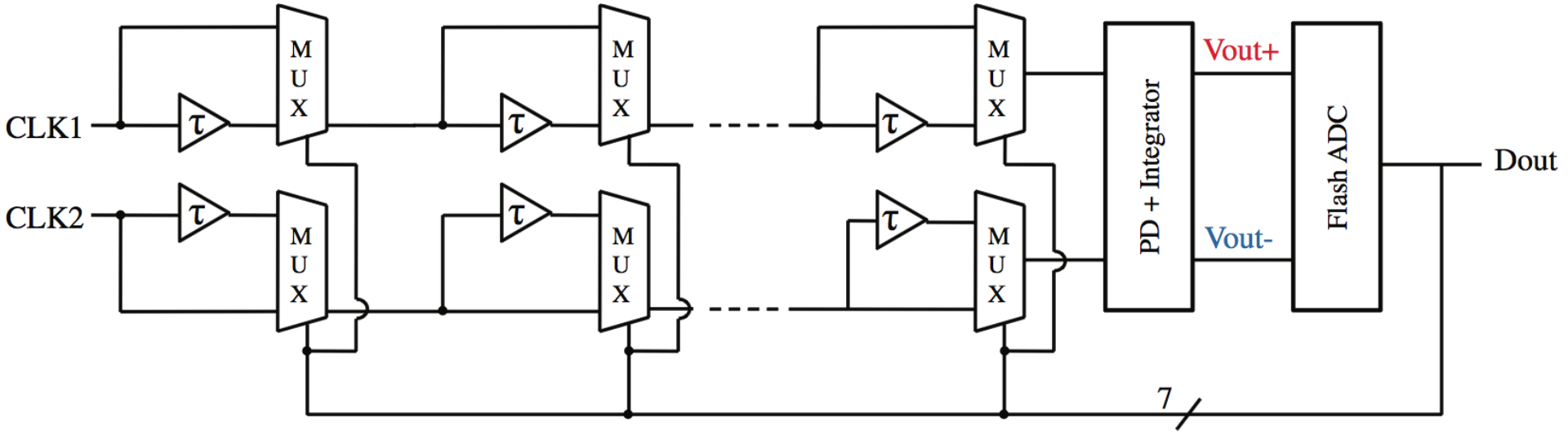
Single-Bit ΣΔ TDC

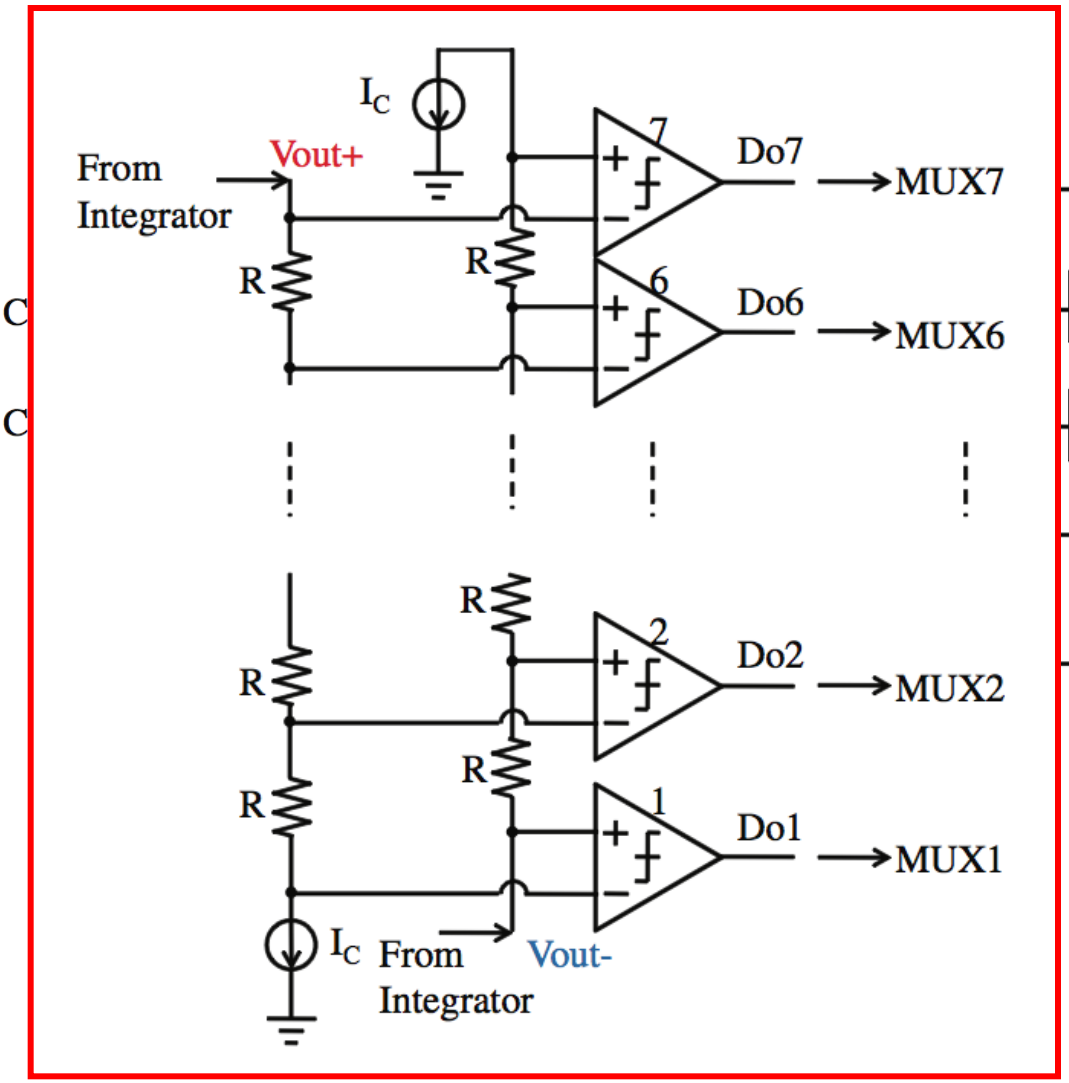


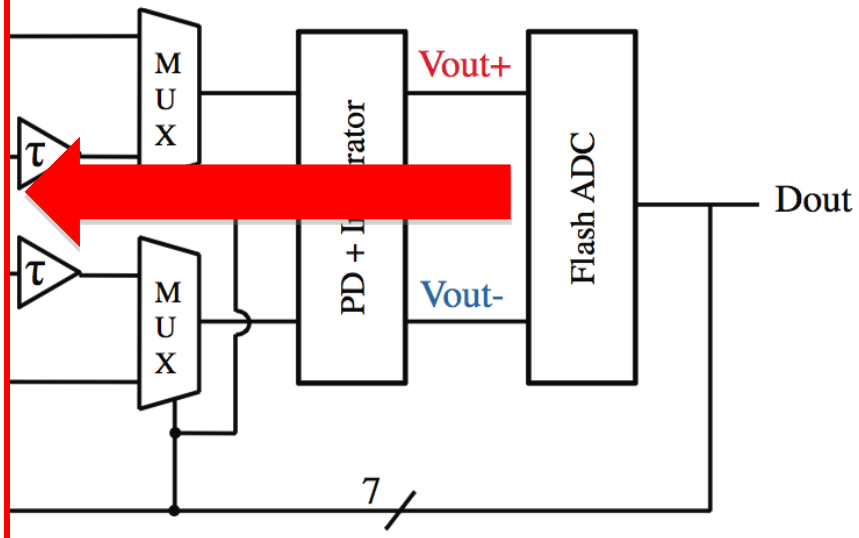
Multi-Bit ΣΔ TDC

Delay cell array



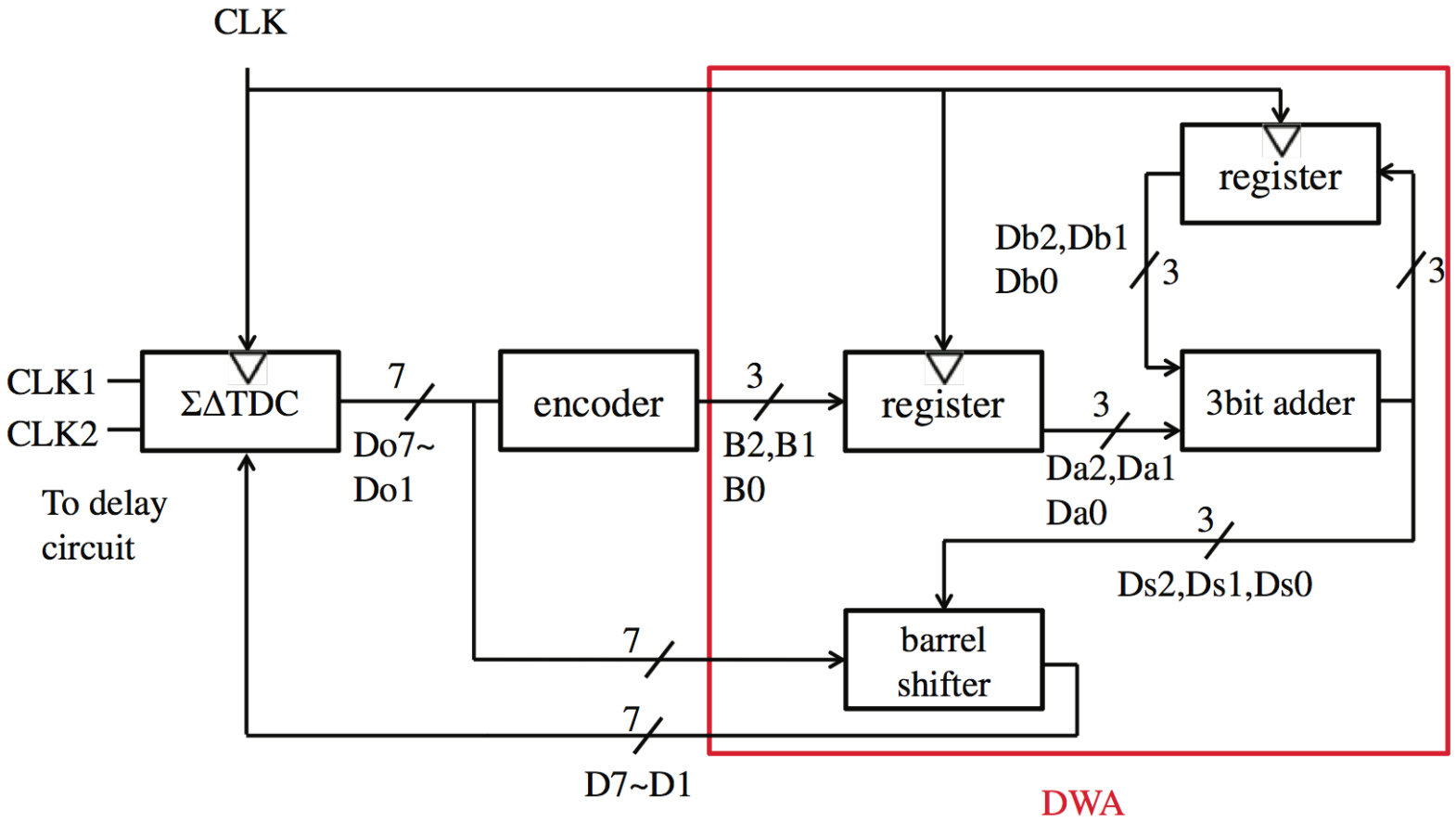
Circuit Design of Multi-Bit ΣΔ TDC





Array of comparators whose outputs are connected to MUX select signals.

DWA Logic



Simple digital circuit:

Two Registers, Encoder, Adder, Barrel Shifter

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Circuit Performance Comparison

	Flash TDC	1-bit ΣΔ TDC	Multi-Bit ΣΔ TDC (without correction)	Multi-Bit ΣΔ TDC (with correction)
Circuitry				
Resolution				
Accuracy				
Time				

Conclusion

- We propose to use ΣΔ TDC
  for digital signal timing measurement.
- Multi-bit ΣΔ TDC.
  - Short measurement time
  - Fine time resolution.
  - Non-linearity due to mismatches among delay cells.

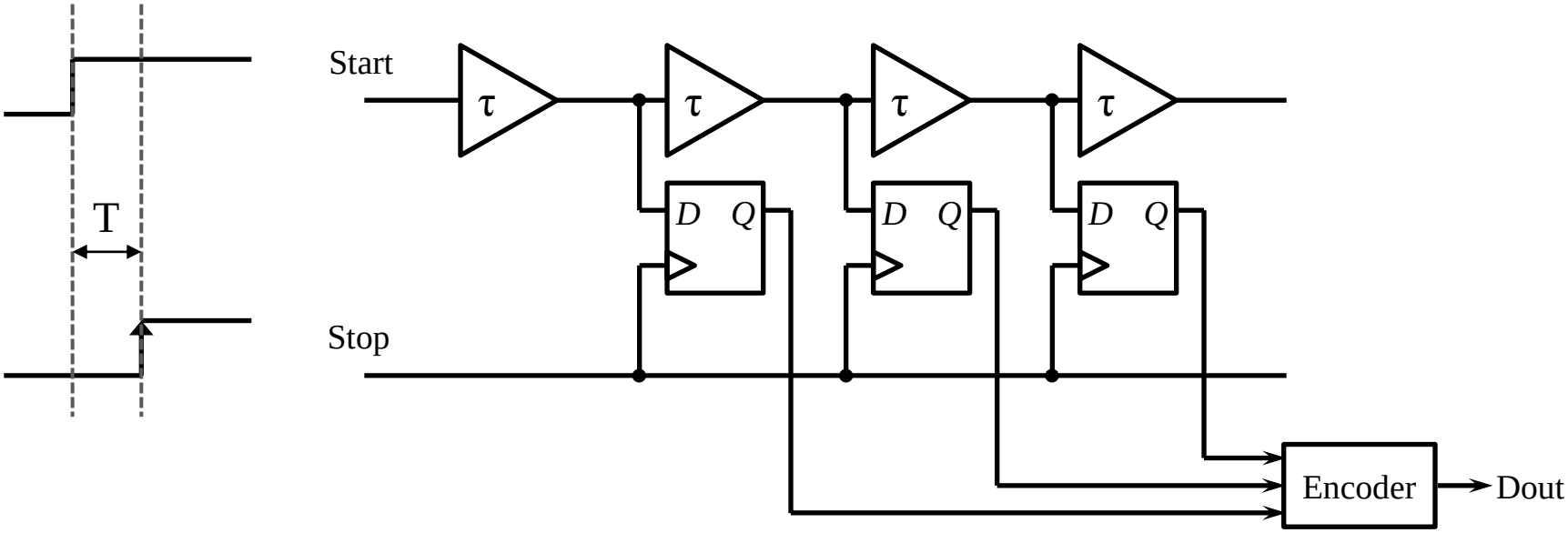
    ⇒ Two techniques to improve linearity
    - DWA
    - Self-Calibration (signal is "time")

Low cost, high quality digital timing test can be realized.

Appendix

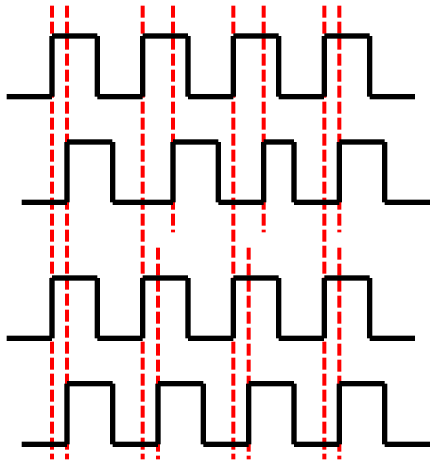
Flash TDC

•Flash TDC



- Arbitrary digital timing signals can be measured one input.
- Circuitry is large.
- Time resolution is τ.

- Measured repetitive digital signals.
  - ➢ High quality testing is required.



Arbitrary signals
- ➢ T is changed.

Repeatitive signals
- ➢ T is constant.

How to Calculate the Delay Time

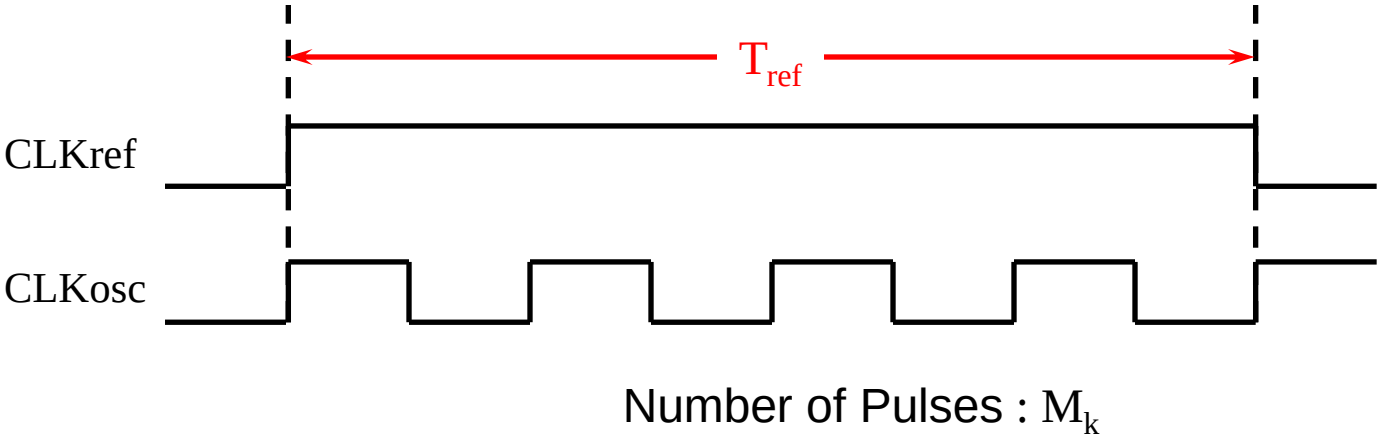
$$f_{OSC}^{k} \approx \frac{M_k}{T_{ref}} = \frac{1}{2(\tau' + \tau_k)}$$

$$\tau_k = \tau + \Delta\tau_k$$

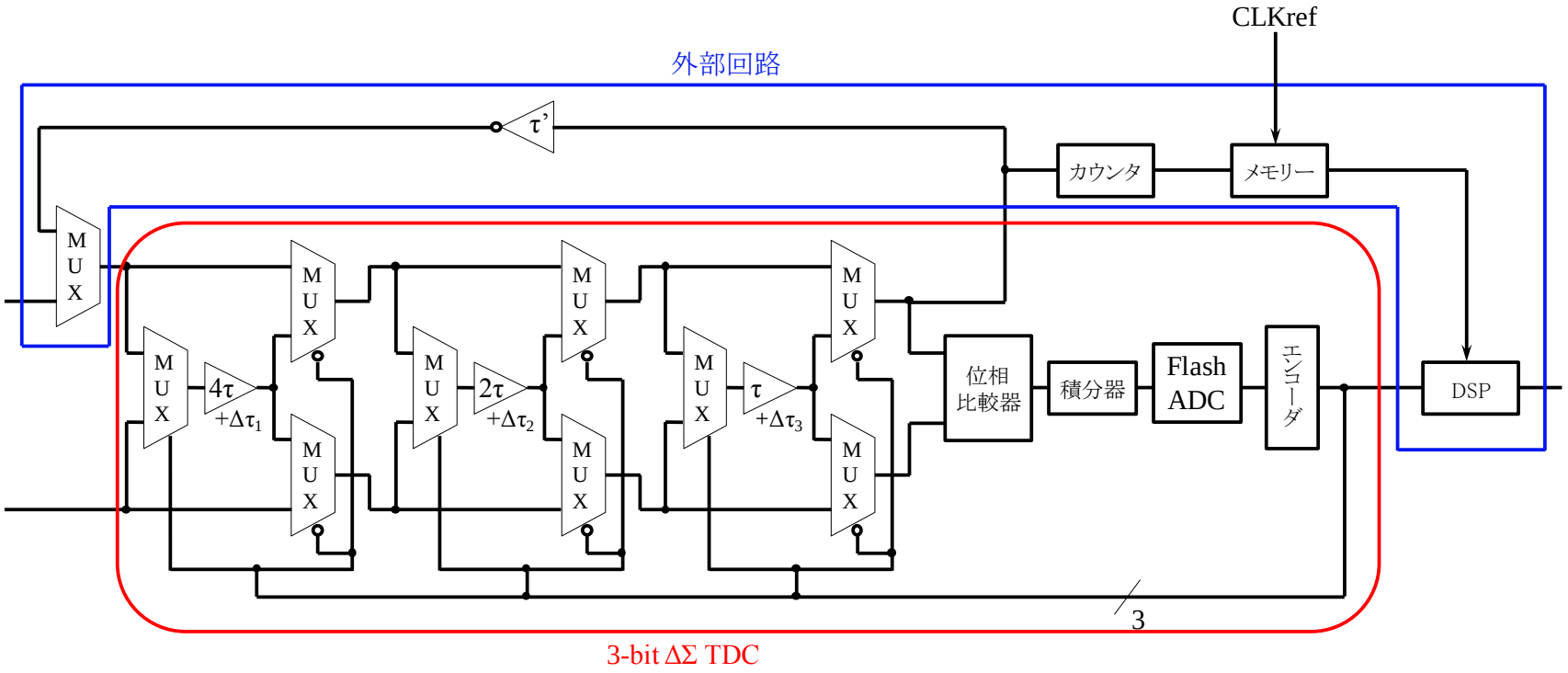
$$f_{OSC}^{0} \approx \frac{M_0}{T_{ref}} = \frac{1}{2\tau'}$$

$$\tau_k = \frac{1}{2}\left(\frac{1}{f_k} - \frac{1}{f_0}\right) \approx \frac{T_{ref}}{2}\left(\frac{1}{M_k} - \frac{1}{M_0}\right)$$

$k=1, 2, \ldots, 2^N-1$



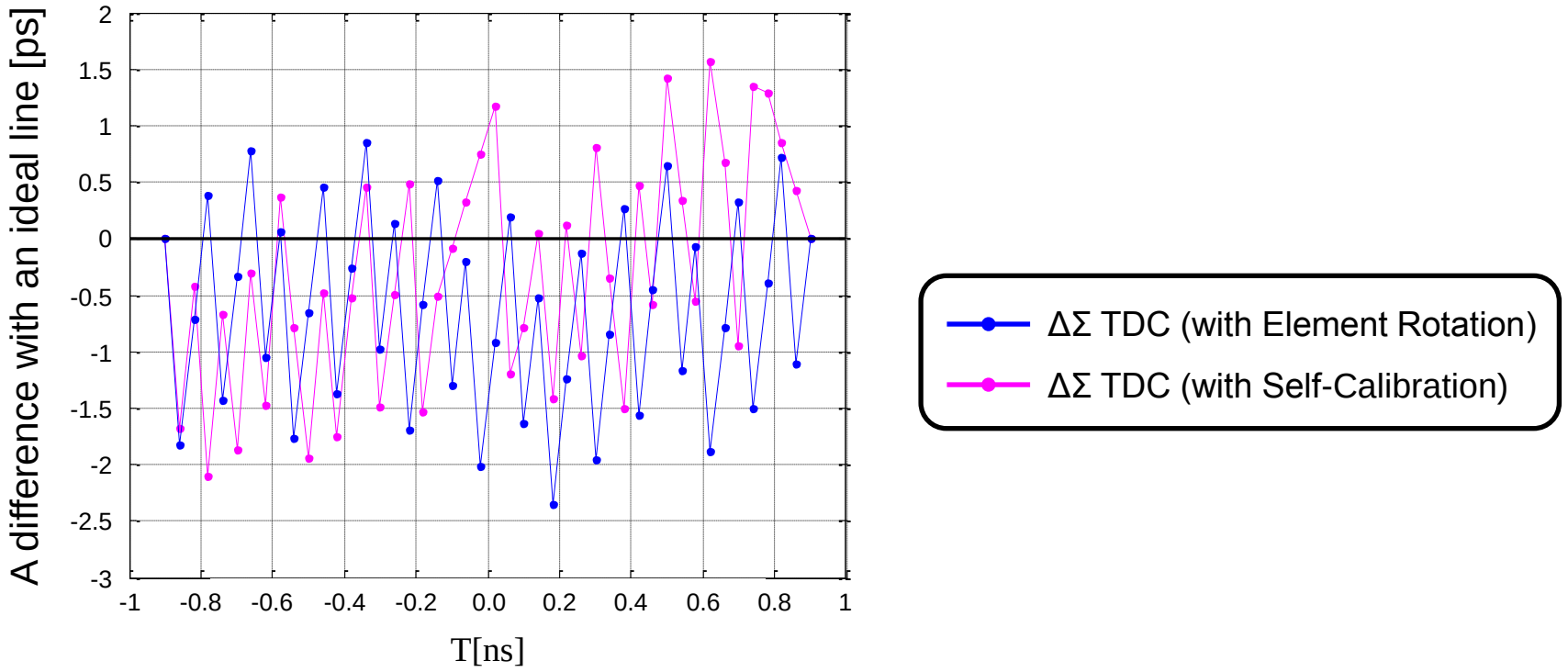
ΣΔ TDC with Self-Calibration



- 各遅延値に重みをもたせる
- 測定にはN-bit で Nステップかかる

Comparison of Linearity

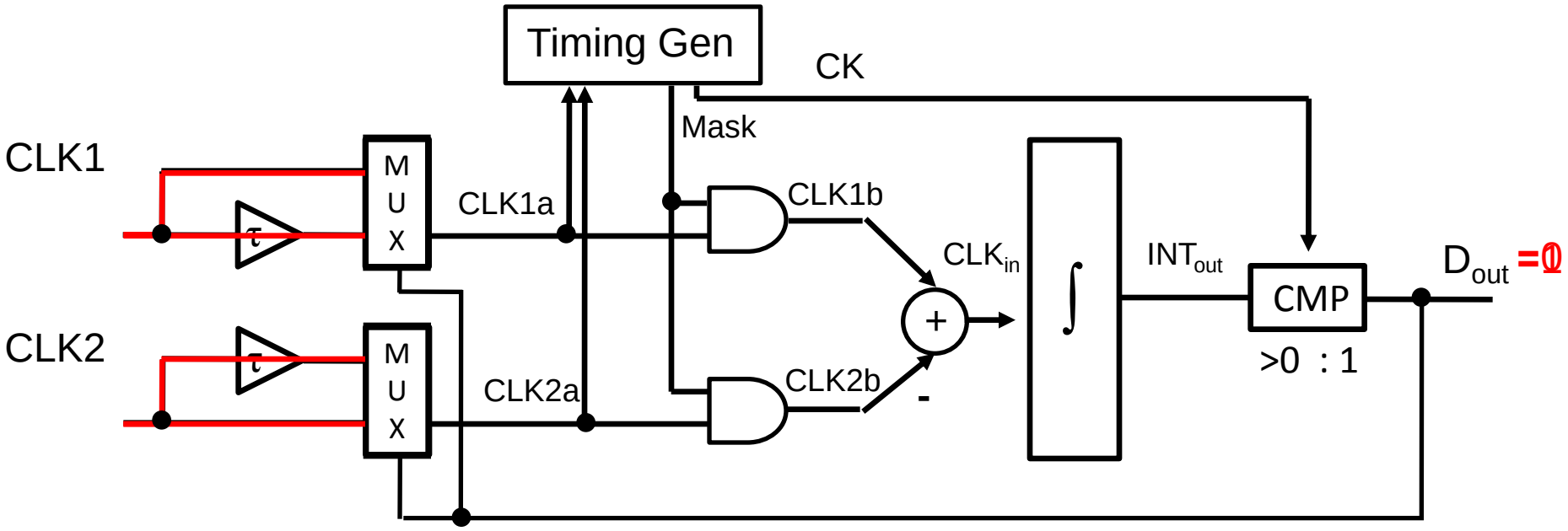
- 3-bit ΔΣ TDC (Delay Time(Ideal) : τ = 0.145ns)

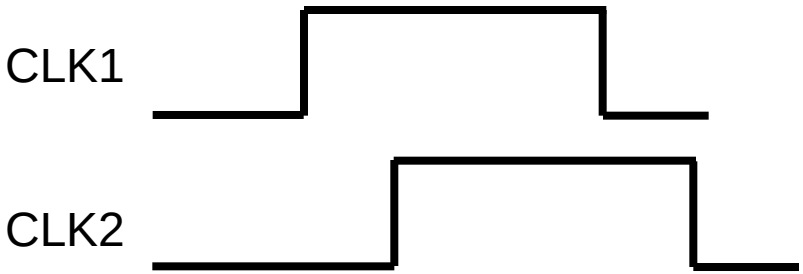


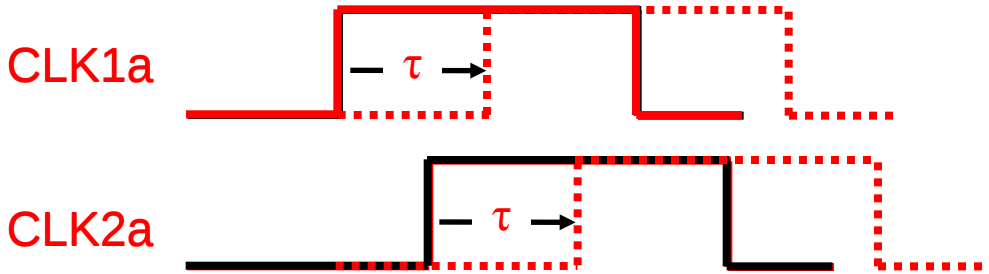
Output pulses : 99

- Ideal state : The error is from -2ps to +2ps.
- After calibration : The error is from -2.5ps to +2.5ps.
  - ➢ The linearity is improved.

シグマデルタ型TDC回路の動作①

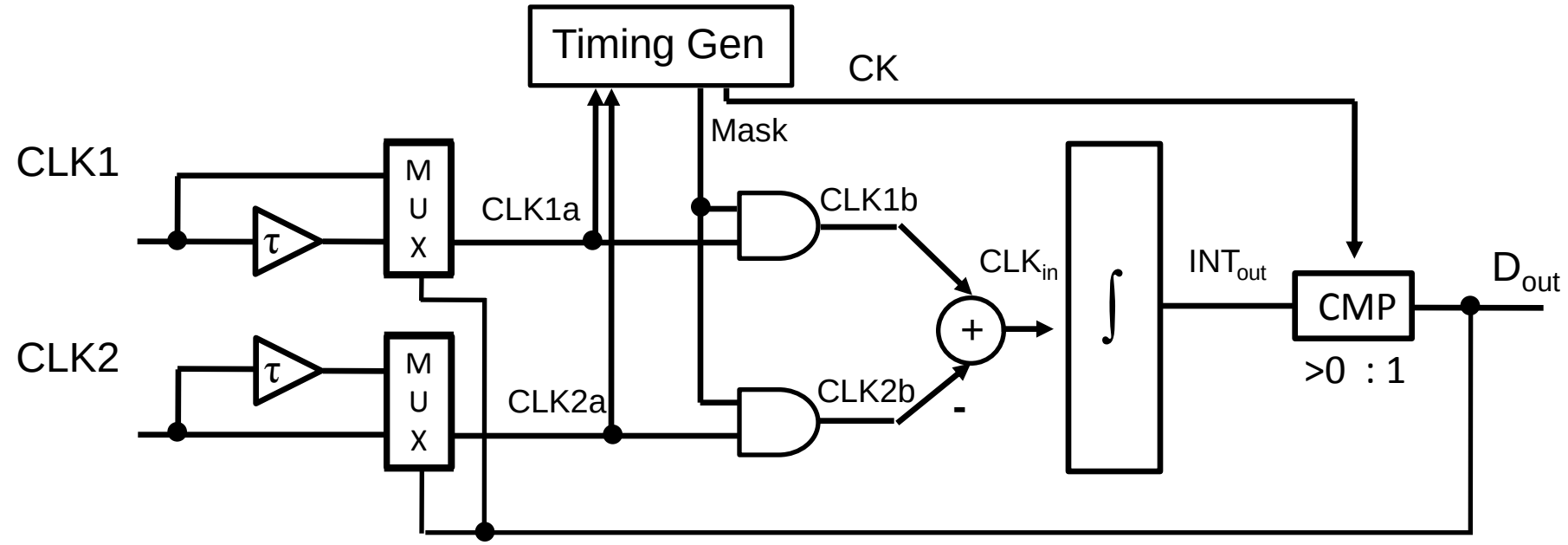


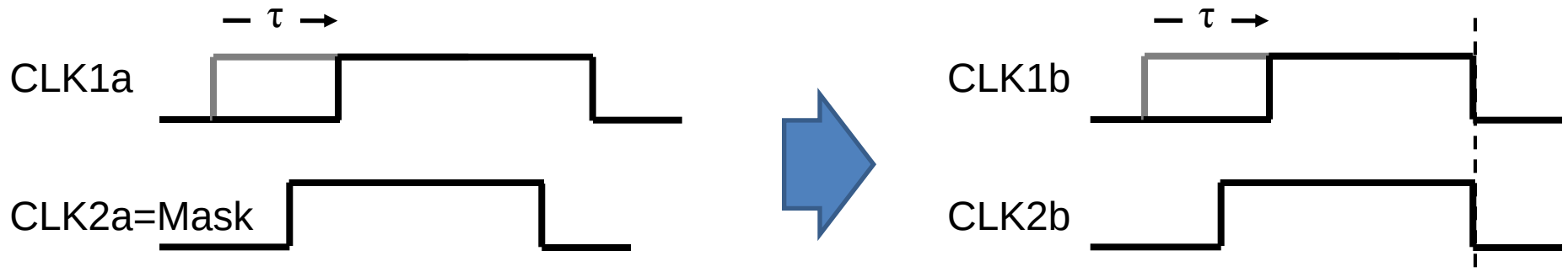




- CLK1とCLK2を入力
- 比較器出力により経路選択
  - CLK1a, CLK2aを得る

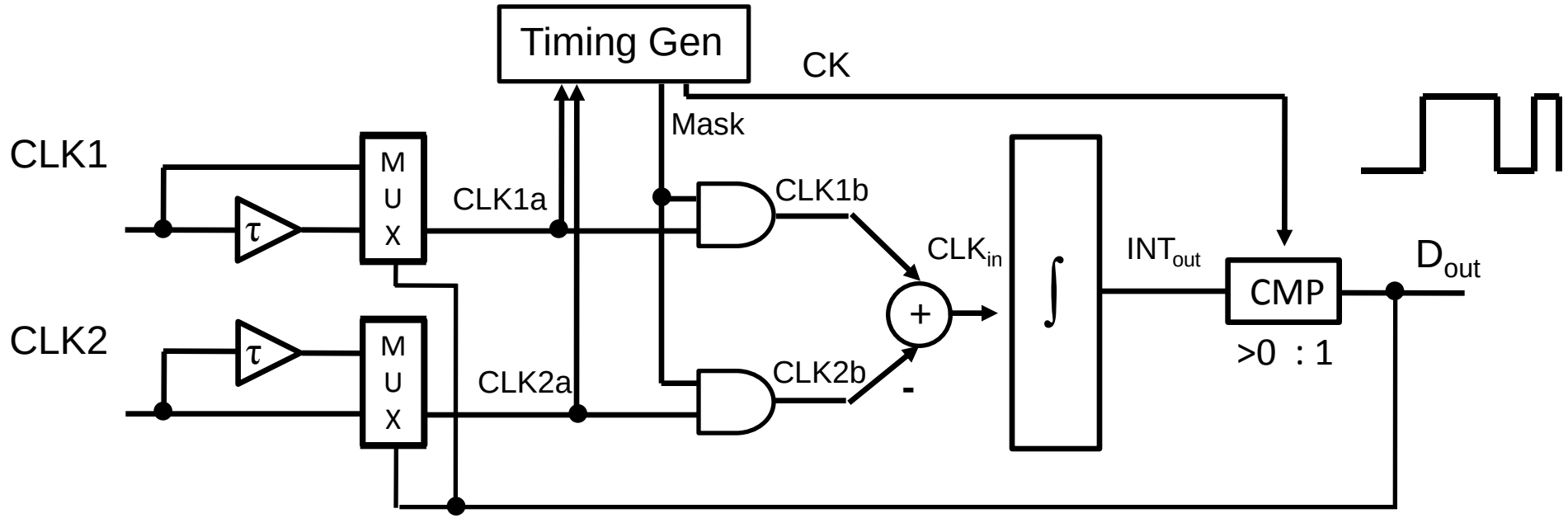
シグマデルタ型TDC回路の動作②

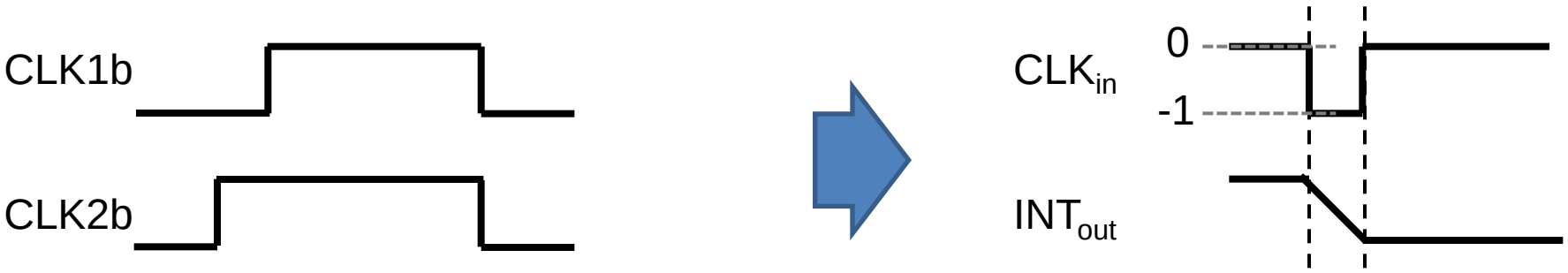




- タイミングジェネレータによりMask信号(=速い方の信号)を発生させる
  - Mask信号とCLK1a, CLK2aとの論理積をとり、立下りを合わせる
  - CLK1b, CLK2bを得る

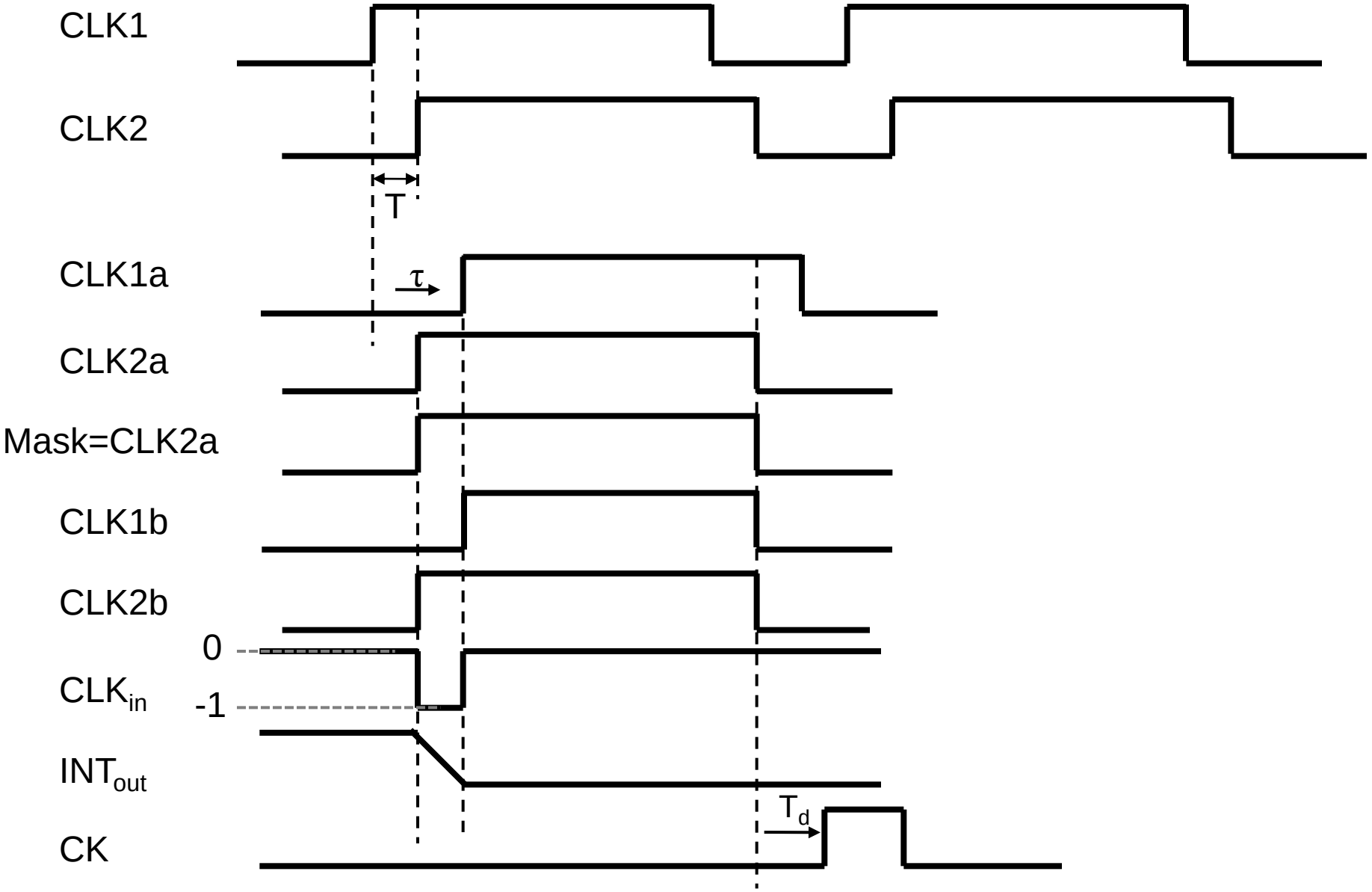
シグマデルタ型TDC回路の動作③





- CLK1bとCLK2bとの差をとり結果のCLK$_{in}$を積分
- 比較器でINT$_{out}$を0と比較し、出力D$_{out}$を得る
  - 次のクロックでの経路を制御

タイミングチャート(D_{out}=1のとき)



タイミングチャート(D_{out}=0のとき)