Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement

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***Abstract*— This paper describes the architecture (circuit design) and principles of operation of sigma-delta ($\Sigma\Delta$) time-to-digital converters (TDC) for high-speed I/O interface circuit test applications; they offer good accuracy with short test times. In particular, we describe multi-bit $\Sigma\Delta$ TDC architectures for fast testing. However, mismatches among delay cells in delay lines degrade the linearity there. Then we propose two methods to improve the overall TDC linearity: a data-weighted averaging algorithm, and a self-calibration method that measures delay values using a ring oscillator circuit. Our MATLAB and Spectre simulation results demonstrate the effectiveness of these approaches.**

Keywords: Time-to-Digital Converter, Time Measurement, Sigma-Delta Modulation, Multi-bit, High-Speed I/O Interface Circuit Testing

I. Introduction

High-speed I/O interfacing circuits such as for double-data-rate (DDR) memory interfaces are very important, and low-cost, high-quality testing of such circuits is challenging [1]. This paper describes simple test circuitry for measuring digital signal timing with high resolution and good accuracy.

We focus on Time-to-Digital Converter (TDC) applications of sigma-delta modulators (for fine-timing-resolution, digital output, and simple circuitry) and with multi-bit architecture (for short testing time).

Multi-bit $\Sigma\Delta$ TDC can suffer from delay mismatches among delay cells, but we propose two techniques to solve this problem and maintain good accuracy: data-weighted-averaging (DWA) and self-calibration.

We describe the principles of $\Sigma\Delta$ TDC in Section Ⅱ, and report the architecture for mismatch delay cell of DWA and calibration in multi-bit $\Sigma\Delta$ TDCs in Section Ⅲ, and Ⅳ. We present simple circuit designs in Section V, and conclusion in Section VI.

II. Sigma-Delta TDC

A. Flash TDC and Sigma-Delta TDC

TDC can be used to measure digital signal timing. The architecture of a basic flash-type TDC is shown in Fig.1 [2]. It consists of a delay-line using delay cells in the signal path and an array of flip-flops. The input **Start** signal passes along the delay cells, which are connected in series. And then each signal is connected to a D input terminal in the D flip-flop array. **Start** signal is delayed only by an integral multiple of the buffer delay τ. The state of each D flip-flop is latched by the rising edge of the **Stop** signal. This circuit converts the time delay between the signals to a certain number of steps of buffer delay. That is, the output from the D flip-flop is obtained as a thermometer code (unary code) output showing the time delay between **Start** signal and **Stop** signal, and this time delay is obtained as a digital output D_{out} using a thermometer-code-to-binary encoder.

The flash-type TDC has the advantage of being able to measure a single-event input, however its disadvantages are that the time resolution is determined by the delay value τ, and its circuitry is large.

We consider here how to measure the time delay between two repetitive digital signals (or clocks), and we use a $\Sigma\Delta$ TDC for the measurement. Although arbitrary digital timing signals cannot be measured with the $\Sigma\Delta$ TDC, it can measure the timing of two clocks where time resolution is inversely proportional to measurement time. The longer the measurement time, the finer the time resolution. We consider here the use of a multi-bit architecture for short testing time, and the use of DWA or self-calibration of the delay cell elements for good accuracy.

Note that the $\Sigma\Delta$ TDCs have been studied recently [3], [4], [5], [6] mainly for all-digital PLL circuits. In this research, we consider to use them for digital signal timing measurement and testing.

B. Single-bit Sigma-Delta TDC

Fig.2 shows a single-bit $\Sigma\Delta$ TDC architecture for our Matlab simulation. It consists of a delay element, three multiplexers, an analog integrator, and a comparator. Its inputs are two clock signals $CLK1$ and $CLK2$ with the same frequency, and it measures the time difference T of their clock timing edges.

In this design, the TDC output as the time difference is positive when the $CLK1$ rising edge is earlier than $CLK2$ and it is negative when the $CLK1$ edge is later. The number of 1's of the comparator output for a given time is proportional to the time difference between $CLK1$ and $CLK2$ when $CLK1$ is earlier. Similarly the number of 0's is proportional to their time difference when $CLK2$ is earlier.

Its operation is as follows:

1) When the comparator output is "1", $CLK1$ is delayed by τ while $CLK2$ is not delayed. When the comparator output is "0", $CLK1$ is not delayed, while $CLK2$ is delayed by τ.
2) The clock signals acquired as the result are defined as $CLK1a$ and $CLK2a$, respectively.
3) Mask signal (generated in "Timing Generator") is the same as $CLK1a$ when $CLK1a$ comes earlier than $CLK2a$; otherwise it is the same as $CLK2a$.
4) $CLK1a$ is logical AND of Mask signal and $CLK1b$, while $CLK2a$ is logical AND of Mask signal and $CLK2b$.
5) We produce the time delay signal CLK_{in} between $CLK1b$ and $CLK2b$ and convert it to the voltage signal by feeding it to the integrator whose output is INT_{out}.
6) The comparator examines whether the integrator output INT_{out} is larger than "0" or not. Its output D_{out} is that of the $\Sigma\Delta$ TDC and feedback to the multiplexers.

Fig.3 shows timing diagram of the signals.

C. Multi-bit Sigma-Delta TDC

Next we describe the multi-bit $\Sigma\Delta$ TDC, and Fig.4 shows its architecture. In the case of the multi-bit $\Sigma\Delta$ TDC, a flash-type A/D converter (precisely, an array of comparators) is used instead of a single comparator, and its digital output is in a thermometer code (unary code) format. The same number of delay elements as that of the comparators are used: in case of an N-bit $\Sigma\Delta$ TDC, $2^N - 1$ comparators and delay elements are used.

Since the integrator output INT_{out} is digitized with an array of comparators (a flash ADC without an encoder), its output D_{out} is in a thermometer code format. Then the digital output in a thermometer code is fed into select signals of an array of multiplexers.

Note that the integrator output INT_{out} is digitized with fine voltage resolution with an array of comparators, and hence the multi-bit $\Sigma\Delta$ TDC can obtain fine time resolution compared to the single-bit one for a given measurement time. (Fig.5 shows the simulation results which support this statement.) In other words, the multi-bit $\Sigma\Delta$ TDC takes shorter measurement time for a given time resolution than the single-bit one, which means lower testing cost.

However, the multi-bit $\Sigma\Delta$ TDC may suffer from mismatches among delay units, which degrades the TDC linearity (which is similar to the multi-bit $\Sigma\Delta$ ADC [7]).

III. Multi-bit Sigma-Delta TDC with DWA

This section shows our proposal of applying the DWA algorithm to the multi-bit $\Sigma\Delta$ TDC for its linearity improvement.

The boxed area in Fig.4 shows a digital-to-time converter (DTC) in a $\Sigma\Delta$ TDC, and the comparators outputs are feedback and select the corresponding delay cells in the DTC.

There is delay value variation among delay cells in actual circuits, and it causes the nonlinearity error of the overall TDC. Then, we propose to apply the DWA algorithm to the multi-bit $\Sigma\Delta$ TDC. Fig.6 shows a block diagram and operation of the DWA logic. It performs the right rotation shift of the $\Sigma\Delta$ TDC comparators outputs in a thermometer code as follows:

1) The first input starts at S_1.
2) Next input starts at the position of S_2 shifted by 1 (the previous input) from the previous position S_1.
3) Next input starts at S_5 that shifted by 3 (the previous input) from the previous position S_2.

This is the $\Sigma\Delta$ operation, and suppresses errors (caused by the delay cell mismatches) in DC component and pushes it in the high frequency side. (Fig.7).

Fig.8 shows a block diagram of the multi-bit $\Sigma\Delta$ TDC with DWA logic. The outputs of the comparator array are fed into DWA logic and their outputs are given to the multiplexers as select signals in the DTC.

We have performed Matlab simulation for a 3-bit $\Sigma\Delta$ TDC with DWA logic. Simulation conditions are given in Table I. The time difference between input clocks used for the simulation is from -0.9ns to 0.9ns.

Figs.9 (a) and (b) show the difference between an ideal line and the simulated result (i.e., the integral non-linearity: INL). Fig.9 (a) is the result in case that the number of comparison times (number of samplings) is 99, and Fig.9 (b) is when it is 599. We see that the INL is large without DWA, however when DWA is employed, it is small and the TDC linearity is improved.

IV. Multi-bit Sigma-Delta TDC with Self-Calibration

We describe here a self-calibration technique to improve the linearity of the multi-bit $\Sigma\Delta$ TDC, utilizing the fact that the input signals are "time" instead of "voltage". Our calibration consists of two steps:

1) Self-measurement of delay values of each delay cell is carried out with a ring oscillator configuration (Fig.10).
2) We improve the TDC linearity using the measured delay values output calculation (Fig.11).

In Fig.11, the vertical axis A_{out} indicates the rising timing edge difference between the input clocks, and the horizontal axis D_{out} shows a digital output of the $\Sigma\Delta$ TDC, and the error from the ideal value is caused by mismatches of the delay cells. We propose here to adjust the D_{out} values (based on the measured cell delays) using fraction as well as integer with the following DSP so that D_{out} and A_{out} are linear.

The following is the measuring method of the cell delays:

1) We add an inverter to have a ring oscillator configuration with each delay cell (Fig.10).
2) We also add a binary counter whose clock is the ring oscillator output and which is in the "enable" state when the reference clock CLK_{ref} is high.

Each cell delay value can be measured *digitally* using the ring oscillator, the counter and the reference clock. We assume here that the time duration is T_{ref} when the reference clock is high, and the number of the ring oscillator output pulses during T_{ref} is M_k. Then the ring oscillator frequency f_{osc}^k is approximated

by

$$f_{osc}^{k} \approx \frac{M_k}{T_{ref}}. \quad (1)$$

As $T_{ref} f_{osc}^{k}$ is larger, this approximation becomes more accurate. Let τ' is the delay time of the added inverter plus the multiplexers, and τ_1 is the measured delay of cell 1. Then we have the following:

$$f_{osc}^{1} = \frac{1}{2(\tau' + \tau_1)}. \quad (2)$$

Similarly we have the following for cell k:

$$f_{osc}^{k} = \frac{1}{2(\tau' + \tau_k)} \quad \text{for } k = 1, 2, .., 2^N - 1. \quad (3)$$

We also measure the ring oscillator frequency with the inverter and multiplexers and without the cell delay.

$$f_{osc}^{0} = \frac{1}{2\tau'}. \quad (4)$$

Then we can obtain the delay value τ_k of each cell based on the above equations:

$$\tau_k = \frac{1}{2}(\frac{1}{f_k} - \frac{1}{f_0}) \approx \frac{T_{ref}}{2}(\frac{1}{M_k} - \frac{1}{M_0}). \quad (5)$$

These measurements/calculations are performed in digital domain, and the measured delay values τ_k are stored in memory.

During measurement of the time difference between clocks with the multi-bit $\Sigma\Delta$ TDC, we carry out digital post-calculation from the TDC output. When $D_{out}(n) = m$, then we use the following corrected output $D_{out}^{correct}(n)$ for the post processing:

$$D_{out}^{correct}(n) = (2^N - 1) \sum_{k=1}^{m} (\frac{1}{M_k} - \frac{1}{M_0})/A. \quad (6)$$

Here

$$A = \sum_{k=1}^{2^N - 1} (\frac{1}{M_k} - \frac{1}{M_0}). \quad (7)$$

Note that $D_{out}(n)(= m)$ is an integer, but $D_{out}^{correct}(n)$ is a real number (integer + fraction). With the P comparison times (sampling times), we have the following time measurement output:

$$T_{measure} = \frac{T_{ref} \cdot A}{2P(2^N - 1)} \sum_{n=1}^{P} (D_{out}^{correct}(n) - \overline{D_{out}^{correct}}(n)). \quad (8)$$

Here

$$\overline{D_{out}^{correct}}(n) = (2^N - 1) \sum_{k=m+1}^{2^N - 1} (\frac{1}{M_k} - \frac{1}{M_0})/A. \quad (9)$$

Fig.12 shows the whole TDC circuit with the proposed self-calibration scheme.

Next we show the simulation results of the 3-bit $\Sigma\Delta$ TDC with self-calibration method. We assume that each delay value is known by self-measurement, and the post-calculation is performed. Simulation conditions are given in Table I.

Figs.13 (a) and (b) show the INL with and without the self-calibration. Fig.13 (a) shows the result in case that the number of comparison times is 99, while Fig.13 (b) is the case that it is 599. We see that our self-calibration improves the linearity.

We close this section by remarking that the similar self-calibration technique is used in $\Sigma\Delta$ ADC [8], [9], where the nonlinearity measurement of the multi-bit DAC inside the $\Sigma\Delta$ ADC modulator is difficult. However, in case of TDC, the nonlinearity self-measurement of the multi-bit DTC is relatively easy using the ring oscillation configuration. This is because the input signal of TDC is "time" while that of ADC is "voltage".

V. Circuit Design

We have designed our $\Sigma\Delta$ TDCs with TSMC 180nm CMOS process parameters.

Fig.14 shows the circuit design of a single-bit sigma-delta TDC, which is composed of a delay selection circuit, a phase-frequency detector (PFD), a charge pump, and a comparator.

- The delay selection circuit consists of a multiplexer, and two delay cells τ with cascaded inverters.
- The PFD consists of two D flip-flops with reset and NAND circuit. If the reset signal is 0, then it forces the DFF outputs to be 0. This circuit outputs the phase difference between $CLK1a$ and $CLK2a$. There are two outputs Vup and $Vdown$. Vup is 1 when $CLK1a$ is 1 and $CLK2a$ is 0, while $Vdown$ is 1 when $CLK1a$ is 0 and $CLK2a$ is 1.
- We have designed a charge pump using op amps for stable operation. Vup and $Vdown$ control appropriate switches. We use a pseudo-differential structure and the outputs are $Vout+$ and $Vout-$.
- The comparator examines which is bigger, $Vout+$ or $Vout-$ at the clock rising edge timing. Output of the comparator is connected to the multiplexer in the delay selection circuit.

Fig.15 shows the circuit design of a multi-bit $\Sigma\Delta$ TDC. We use an array of comparators (a flash ADC without an encoder) whose outputs are connected to the selection signals of the multiplexers.

Fig.16 shows a block diagram of DWA logic. The encoder converts the comparator outputs in a thermometer code into 3-bit binary signal (B2, B1, B0). We have two registers: one is to hold the 3-bit signals and delay them by 1 clock, and its outputs are (Da2, Da1, Da0). The other is for the output of 3-bit adder, and its outputs are (Db2, Db1, Db0). The output of 3-bit adder adds the output of two registers and its outputs are (Ds2, Ds1, Ds0). We have checked the operation of this circuit and verified that the DWA logic works correctly.

We have combined all the circuits and checked that the overall circuit works correctly with Spectre simulation.

VI. Conclusions

We have described multi-bit $\Sigma\Delta$ TDC architectures for fast and high accuracy testing of the timing between two clocks. We have proposed two techniques to reduce the effects of

delay mismatches among delay cells: one is a DWA algorithm, and the other is self-calibration for the delay cells. Our self-calibration can be done easily since the signal is "time" rather than "voltage". We have performed system design, circuit design as well as Matlab and Spectre simulation, which validate the effectiveness of our proposed approach. Our simulation results show that the correction techniques of DWA and self-calibration can improve linearity to near the ideal state.

Our proposed circuits are simple but enable fast and accurate testing, and hence we expect to use them as DFT, BIST or BOST for clock timing measurement and testing.

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We acknowledge Y. Yano, T. Gake, N. Takai, T. J. Yamaguchi, K. Wilkinson and STARC.

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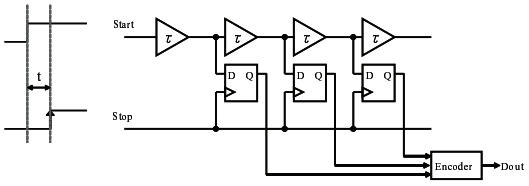


Fig. 1. Architecture of a flash-type TDC.

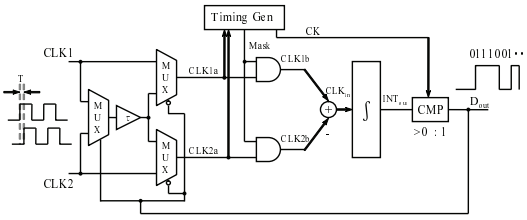
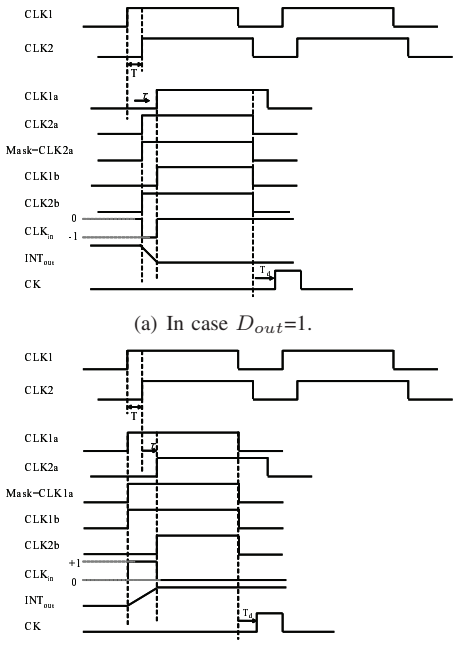


Fig. 2. A single-bit ΣΔ TDC.



(a) In case D_{out}=1.

(b) In case D_{out}=0.

Fig. 3. Timing diagram of a single-bit ΣΔ TDC.

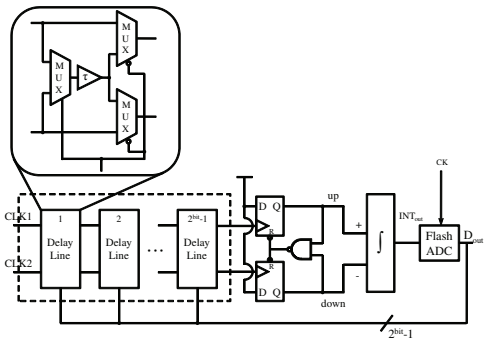
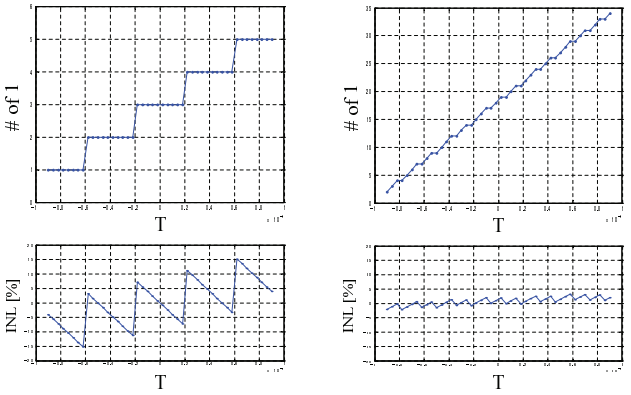


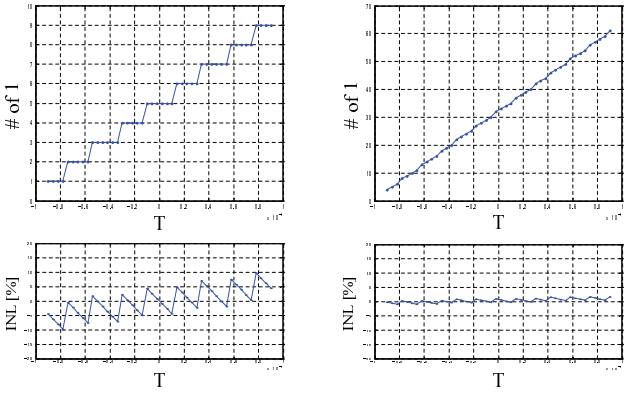
Fig. 4. Architecture of a multi-bit ΣΔ TDC.

TABLE I
PARAMETERS OF DELAY VALUES FOR SIMULATION

	$\tau 1$	$\tau 2$	$\tau 3$	$\tau 4$
Delay values(Ideal)	0.145	0.145	0.145	0.145
Delay values(Actual)	0.140	0.149	0.148	0.143
	$\tau 5$	$\tau 6$	$\tau 7$	Total of τ
Delay values(Ideal)	0.145	0.145	0.145	1.015
Delay values(Actual)	0.145	0.148	0.146	1.019



(a) In case of 1-bit, 5 samples. (b) In case of 3-bit , 5 samples.



(c) In case of 1-bit, 9 samples. (d) In case of 3-bit, 9 samples.

Fig. 5. Rising timing edge difference T of two input signals and accumulation of digital outputs (or INL) of 1-bit or 3-bit $\Sigma\Delta$ TDCs when the number of sampling times is 5 or 9.

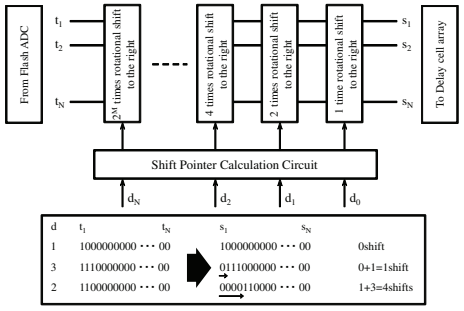


Fig. 6. Operation of DWA logic.

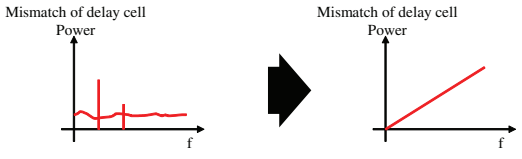


Fig. 7. Noise-shaping by DWA logic.

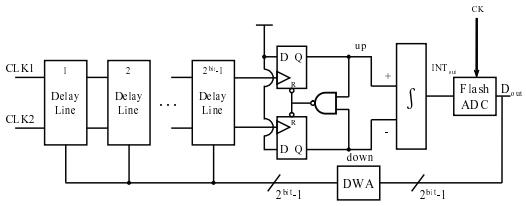
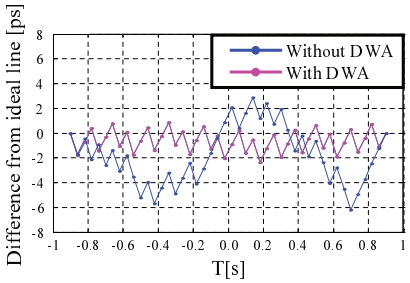
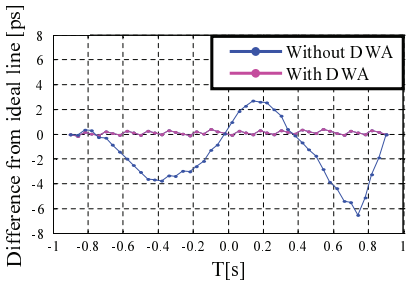


Fig. 8. Architecture of a multi-bit $\Sigma\Delta$ TDC with DWA logic.



(a) In case 99 times.



(b) In case 599 times.

Fig. 9. INL with and without DWA (simulation results).

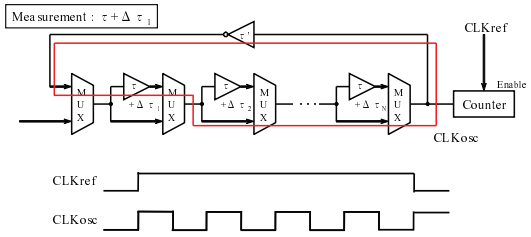


Fig. 10. Self-measurement of delay values with a ring oscillator configuration.

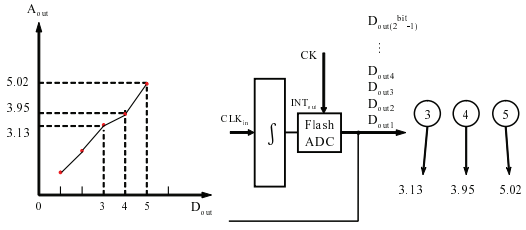


Fig. 11. Proposed error correction scheme.

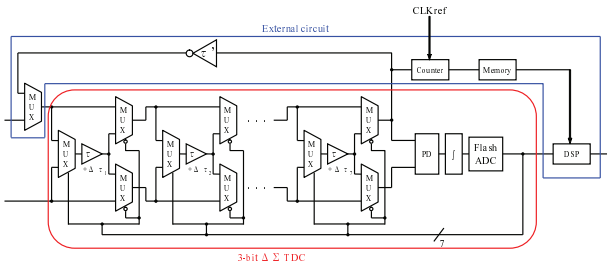
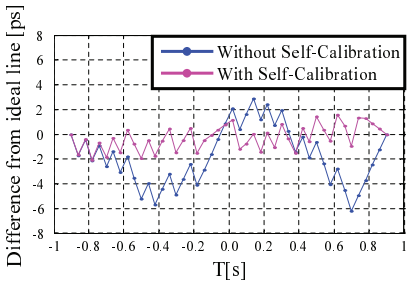
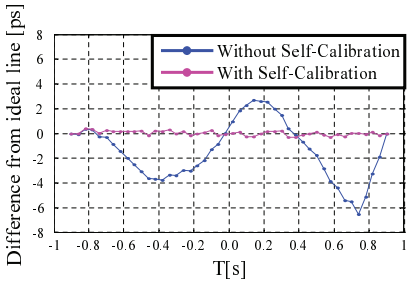


Fig. 12. TDC circuit with self-calibration.



(a) In case 99 times.



(b) In case 599 times.

Fig. 13. INL with and without self-calibration (simulation results).

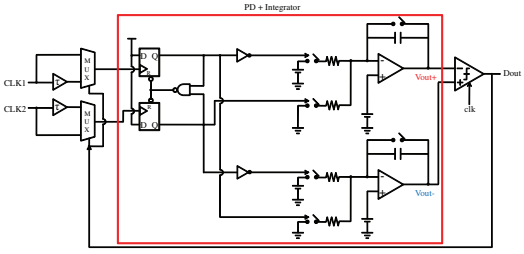
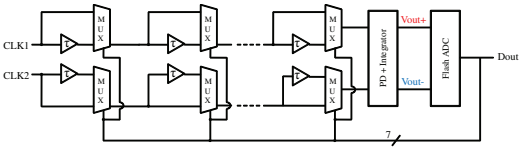
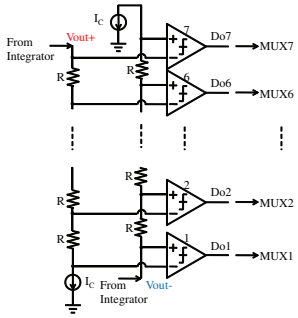


Fig. 14. Circuit design of a single-bit ΣΔ TDC.



(a)



(b)

Fig. 15. Circuit design of a multi-bit ΣΔ TDC. (a) The whole circuit. (b) Flash ADC part.

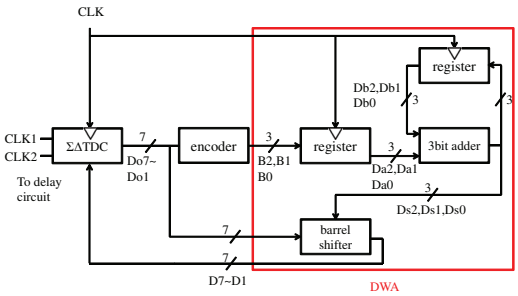


Fig. 16. Block diagram of DWA logic.