Multi-bit Sigma-Delta TDC Architecture with Self-Calibration

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***Abstract*— This paper describes the architecture and principles of operation of sigma-delta (ΣΔ) time-to-digital converters (TDC) for high-speed I/O interface circuit test applications; they offer good accuracy with short test times. In particular, we describe a multi-bit ΣΔ TDC architecture for fast testing. However, mismatches among delay cells in delay lines degrade the linearity there. Then we propose a self-calibration method that measures delay values using an improved ring oscillator circuit to improve the overall TDC linearity. Our MATLAB simulation results demonstrate the effectiveness of the proposed approach.**

Keywords: Time-to-Digital Converter, Time Measurement, Sigma-Delta Modulation, Multi-bit, Self-Calibration

I. Introduction

High-speed I/O interfacing circuits such as for double-data-rate (DDR) memory interfaces are very important, and low-cost, high-quality testing of such circuits is challenging [1]. This paper describes simple test circuitry for measuring digital signal timing (such as DDR memory interface timing) with high resolution and good accuracy.

We focus on Time-to-Digital Converter (TDC) applications of sigma-delta modulators (for fine-timing-resolution, digital output, and simple circuitry) and with multi-bit architecture (for short testing time).

Multi-bit ΣΔ TDC can suffer from delay mismatches among delay cells, but we propose a self-calibration technique to solve this problem and maintain good accuracy.

We describe the principles of ΣΔ TDC in Section II, and report the calibration in a multi-bit ΣΔ TDC in Section III We present its improved circuit in Section IV, and conclusion in Section V.

II. Sigma-Delta TDC

A. Flash TDC and Sigma-Delta TDC

TDC can be used to measure digital signal timing. The architecture of a basic flash-type TDC is shown in Fig.1 [2]. The flash-type TDC has the advantage of being able to measure a single-event input, however its disadvantages are that the time resolution is determined by the delay value τ, and its circuitry is large.

We consider here how to measure the time delay between two repetitive digital signals (or clocks), and we use a ΣΔ TDC for the measurement. Although arbitrary digital timing signals cannot be measured with the ΣΔ TDC, it can measure the timing of two clocks where time resolution is inversely proportional to measurement time. The longer the measurement time, the finer the time resolution. We consider here the use of a multi-bit architecture for short testing time, and the use of DWA or self-calibration of the delay cell elements for good accuracy.

Note that the ΣΔ TDCs have been studied recently [3], [4], [5], [6] mainly for all-digital PLL circuits. In this research, we consider to use them for digital signal timing measurement and testing.

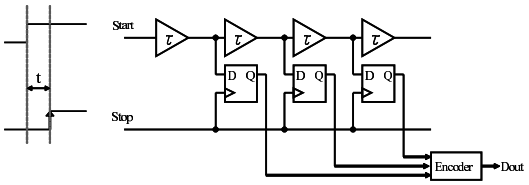


Fig. 1. Architecture of a flash-type TDC.

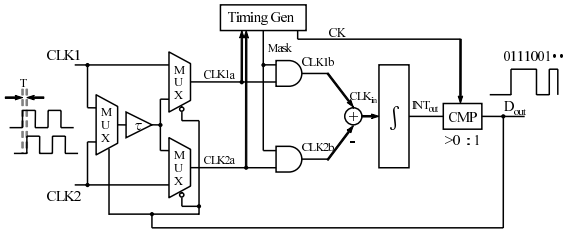
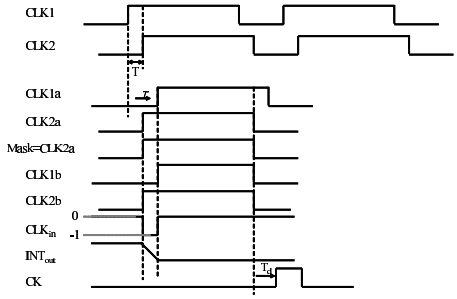


Fig. 2. A single-bit ΣΔ TDC.

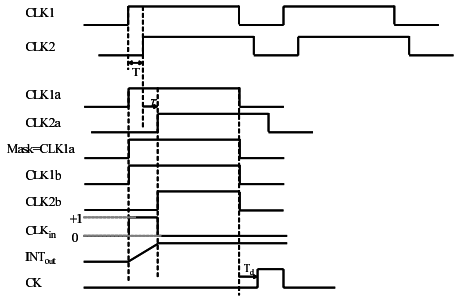
B. Single-bit Sigma-Delta TDC

Fig.2 shows a single-bit ΣΔ TDC architecture for our Matlab simulation. It consists of a delay element, three multiplexers, an analog integrator, and a comparator. Its inputs are two clock signals $CLK1$ and $CLK2$ with the same frequency, and it measures the time difference T of their clock timing edges.

In this design, the TDC output as the time difference is positive when the $CLK1$ rising edge is earlier than $CLK2$ and it is negative when the $CLK1$ edge is later. The number of 1's of the comparator output for a given time is proportional to the time difference between $CLK1$ and $CLK2$ when $CLK1$ is earlier. Similarly the number of 0's is proportional to their time difference when $CLK2$ is earlier. Its operation is as follows:



(a) In case D_{out}=1.



(b) In case D_{out}=0.

Fig. 3. Timing diagram of a single-bit $\Sigma\Delta$ TDC.

(i) When the comparator output is "1", $CLK1$ is delayed by τ while $CLK2$ is not delayed. When the comparator output is "0", $CLK1$ is not delayed, while $CLK2$ is delayed by τ.
(ii) The clock signals acquired as the result are defined as $CLK1a$ and $CLK2a$, respectively.
(iii) Mask signal (generated in "Timing Generator") is the same as $CLK1a$ when $CLK1a$ comes earlier than $CLK2a$; otherwise it is the same as $CLK2a$.
(iv) $CLK1b$ is logical AND of Mask signal and $CLK1a$, while $CLK2b$ is logical AND of Mask signal and $CLK2a$.
(v) We produce the time delay signal CLK_{in} between $CLK1b$ and $CLK2b$ and convert it to the voltage signal by feeding it to the integrator whose output is INT_{out}.
(vi) The comparator examines whether the integrator output INT_{out} is larger than "0" or not. Its output D_{out} is that of the $\Sigma\Delta$ TDC and feedback to the multiplexers.

Fig.3 shows timing diagram of the signals.

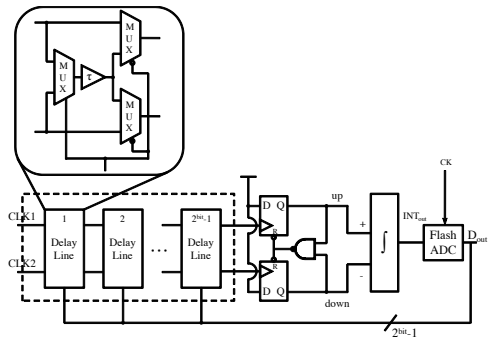


Fig. 4. Architecture of a multi-bit $\Sigma\Delta$ TDC.

C. Multi-bit Sigma-Delta TDC

Next we describe the multi-bit $\Sigma\Delta$ TDC, and Fig.4 shows its architecture. In the case of the multi-bit $\Sigma\Delta$ TDC, a flash-type A/D converter (precisely, an array of comparators) is used instead of a single comparator, and its digital output is in a thermometer code format. The same number of delay elements as that of the comparators are used: in case of an N-bit $\Sigma\Delta$ TDC, $2^N - 1$ comparators and delay elements are used.

Since the integrator output INT_{out} is digitized with an array of comparators, its output D_{out} is in a thermometer code format. Then the digital output in a thermometer code is fed into select signals of an array of multiplexers.

Note that the integrator output INT_{out} is digitized with fine voltage resolution with an array of comparators, and hence the multi-bit $\Sigma\Delta$ TDC can obtain fine time resolution compared to the single-bit one for a given measurement time [7]. In other words, the multi-bit $\Sigma\Delta$ TDC takes shorter measurement time for a given time resolution than the single-bit one, which means lower testing cost.

However, the multi-bit $\Sigma\Delta$ TDC may suffer from mismatches among delay units, which degrades the TDC linearity (which is similar to the multi-bit $\Sigma\Delta$ ADC [8]).

Remark (i) The delay τ determines the input range of the $\Sigma\Delta$ TDC; the time resolution of the $\Sigma\Delta$ TDC is determined not only by τ but also by the measurement time length (the number of the comparisons of the ADC inside the modulator).
(ii) The input range of a single-bit $\Sigma\Delta$ TDC is from -τ to τ. But for example, a 3-bit $\Sigma\Delta$ TDC is from -8τ to 8τ; the delay value of the 3-bit $\Sigma\Delta$ TDC should be designed to one-eighth of that of the single-bit $\Sigma\Delta$ TDC. (if necessarily, a vernia delay line can be used to realize effectively fine τ.)

III. Multi-bit Sigma-Delta TDC with Self-Calibration

We describe here a self-calibration technique to improve the linearity of the multi-bit $\Sigma\Delta$ TDC, utilizing the fact that the input signals are "time" instead of "voltage". Our calibration consists of two steps:
(i) Self-measurement of delay values of each delay cell is carried out with a ring oscillator configuration (Fig.5).
(ii) We improve the TDC linearity using the measured delay values output calculation (Fig.6).

In Fig.6, the vertical axis A_{out} indicates the rising timing edge difference between the input clocks, and the horizontal axis D_{out} shows a digital output of the $\Sigma\Delta$ TDC, and the error from the ideal value is caused by mismatches of the delay cells. We propose here to adjust the D_{out} values (based on the measured cell delays) using fraction as well as integer with the following DSP so that D_{out} and A_{out} are linear: in other words, the DSP has to calculate in a floating-point number format instead of in a fixed-point number format. For example, suppose that $(3\tau + \Delta\tau_1 + \Delta\tau_2 + \Delta\tau_3)/\tau = 3.13$ in Fig.6. Then the DSP uses 3.13 for the following digital lowpass filter calculation in case that the 3-bit ADC output is 3. Similarly, if $(4\tau + \Delta\tau_1 + \Delta\tau_2 + \Delta\tau_3 + \Delta\tau_4)/4 = 3.95$, then the DSP uses 3.95 in case that the ADC output is 4 [9], [10].

The following is the measuring method of the cell delays:
(i) We add an inverter to have a ring oscillator configuration with each delay cell (Fig.5).
(ii) We also add a binary counter whose clock is the ring oscillator output and which is in the "enable" state when the reference clock CLK_{ref} is high.

Each cell delay value can be measured *digitally* using the ring oscillator, the counter and the reference clock. We assume here that the time duration is T_{ref} when the reference clock is high, and the number of the ring oscillator output pulses during T_{ref} is M_k. Then the ring oscillator frequency f_{osc}^k is approximated by

$$f_{osc}^k \approx \frac{M_k}{T_{ref}}. \tag{1}$$

As $T_{ref} f_{osc}^k$ is larger, this approximation becomes more accurate. Let τ' is the delay time of the added inverter plus the multiplexers, and τ_1 is the measured delay of cell 1. Then we have the following:

$$f_{osc}^1 = \frac{1}{2(\tau' + \tau_1)}. \tag{2}$$

Similarly we have the following for cell k:

$$f_{osc}^k = \frac{1}{2(\tau' + \tau_k)} \quad \text{for } k = 1, 2, .., 2^N - 1. \tag{3}$$

We also measure the ring oscillator frequency with the inverter and multiplexers and without the cell delay.

$$f_{osc}^0 = \frac{1}{2\tau'}. \tag{4}$$

Then we can obtain the delay value τ_k of each cell based on the above equations:

$$\tau_k = \frac{1}{2}\left(\frac{1}{f_{osc}^k} - \frac{1}{f_{osc}^0}\right) \approx \frac{T_{ref}}{2}\left(\frac{1}{M_k} - \frac{1}{M_0}\right). \tag{5}$$

These measurements/calculations are performed in digital domain, and the measured delay values τ_k are stored in memory.

During measurement of the time difference between clocks with the multi-bit $\Sigma\Delta$ TDC, we carry out digital post-calculation from the TDC output. When $D_{out}(n) = m$, then we use the following corrected output $D_{out}^{correct}(n)$ for the post processing:

$$D_{out}^{correct}(n) = (2^N - 1)\sum_{k=1}^{m}\left(\frac{1}{M_k} - \frac{1}{M_0}\right)/A. \tag{6}$$

$$\text{Here} \qquad A = \sum_{k=1}^{2^N-1}\left(\frac{1}{M_k} - \frac{1}{M_0}\right). \tag{7}$$

Note that $D_{out}(n)(= m)$ is an integer, but $D_{out}^{correct}(n)$ is a real number (integer + fraction). With the P comparison times (sampling times), we have the following time measurement output:

$$T_{measure} = \frac{T_{ref} \cdot A}{2P(2^N - 1)} \sum_{n=1}^{P}\left(D_{out}^{correct}(n) - \overline{D_{out}^{correct}}(n)\right). \tag{8}$$

$$\text{Here} \quad \overline{D_{out}^{correct}}(n) = (2^N - 1)\sum_{k=m+1}^{2^N-1}\left(\frac{1}{M_k} - \frac{1}{M_0}\right)/A. \tag{9}$$

Fig.7 shows the whole TDC circuit with the proposed self-calibration scheme.

Next we show the simulation results of the 3-bit $\Sigma\Delta$ TDC with self-calibration method. We assume that each delay value is known by self-measurement, and the post-calculation is performed. Simulation conditions are given in Table I. Figs.8 (a) and (b) show the INL with and without the self-calibration. Fig.8 (a) shows the result in case that the number of comparison times is 99, while Fig.8 (b) is the case that it is 599. We see that our self-calibration improves the linearity.

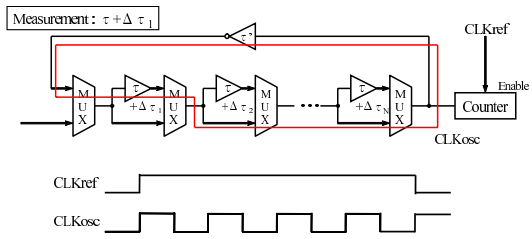


Fig. 5. Self-measurement of delay values with a ring oscillator configuration.

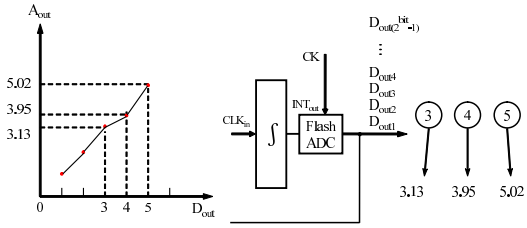


Fig. 6. Proposed error correction scheme.

We close this section by remarking that the similar self-calibration technique is used in $\Sigma\Delta$ ADC [9], [10], where the nonlinearity measurement of the multi-bit DAC inside the $\Sigma\Delta$ ADC modulator is difficult. However, in case of TDC, the nonlinearity self-measurement of the multi-bit DTC is relatively easy using the ring oscillation configuration. This is because the input signal of TDC is "time" while that of ADC is "voltage".

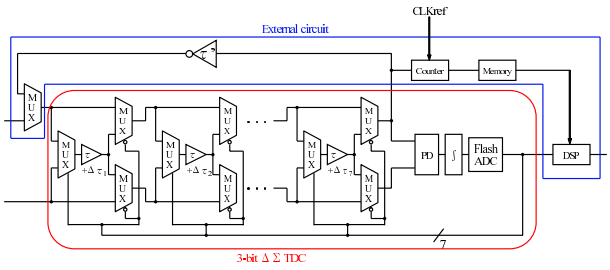
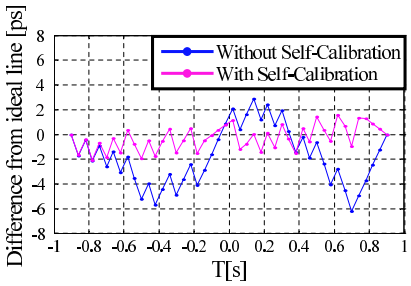
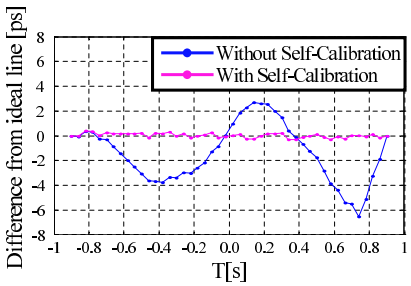


Fig. 7. TDC circuit with self-calibration.



(a) In case 99 times.



(b) In case 599 times.

Fig. 8. INL with and without self-calibration (simulation results).

TABLE I

PARAMETERS OF DELAY VALUES FOR SIMULATION

	$\tau 1$	$\tau 2$	$\tau 3$	$\tau 4$
Delay values(Ideal)	0.145	0.145	0.145	0.145
Delay values(Actual)	0.140	0.149	0.148	0.143
	$\tau 5$	$\tau 6$	$\tau 7$	Total of τ
Delay values(Ideal)	0.145	0.145	0.145	1.015
Delay values(Actual)	0.145	0.148	0.146	1.019

IV. IMPROVED DELAY MEASUREMENT CIRCUIT

This section shows an improved delay-value self-measurement circuit in Fig.9, compared to our previously disclosed one in Figs.5, 7 [7]. The oscillation frequency f_{osc} of the basic ring-oscillator configuration in Fig.5 is a function of the buffer delay τ. Note that τ is the average of τ_r and τ_f (i.e., $\tau = (\tau_r + \tau_f)/2$), where τ_r is the delay when the buffer output rises from low to high level, and τ_f is the one when it falls from high to low level. However, we need the value of τ_r and we cannot measure it accurately with the ring oscillator in Fig.5 when τ_r and τ_f are quite different.

The oscillation frequency of the improved circuit in Fig.9 (a) is only a function of τ_r but is not a function of τ_f. Fig.9 (b) shows the timing chart of its signals for $\tau_r < \tau_f$. We have checked its operation with Spectre simulation. (Notice that we need to design the buffer delay in Fig.4 intentionally to satisfy $\tau_r < \tau_f$ to use the circuit in Fig.9 for self-calibration.)

By replacing one of the five buffers from node "a" to node "b" in Fig.9 (a) with the buffer in Fig.4 whose rise delay $\tau_{r(measure)}$ should be measured, we can obtain the accurate value of $\tau_{r(measure)}$ with measuring the oscillation frequency.

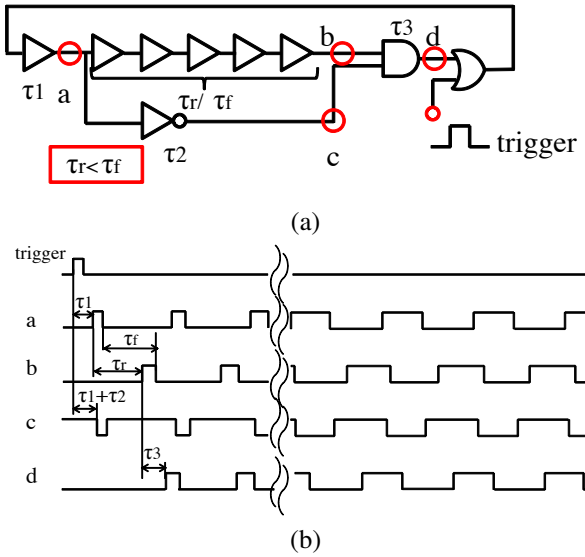


Fig. 9. (a) Oscillator circuit to measure the rise delay of the buffer. (b) Timing chart.

V. CONCLUSIONS

We have described multi-bit $\Sigma\Delta$ TDC architecture for fast and high accuracy testing of the timing between two clocks. We have proposed a self-calibration technique with an improved circuit to reduce the effects of delay mismatches among delay cells. Our self-calibration can be done easily since the signal is gtimeh rather than gvoltageh, and our Matlab simulation validates the effectiveness.

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