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Multi-bit Sigma-Delta TDC Architecture with Self-Calibration

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Presented by Yuta Arakawa (荒川雄太）

Outline

- ► Research Objective
- ► Single-Bit & Multi-bit ΣΔ TDCs
- ► Multi-Bit ΣΔ TDC with DWA
- ► Multi-Bit ΣΔ TDC with Self-Calibration
- ► Conclusion

Outline

- ► **Research Objective**
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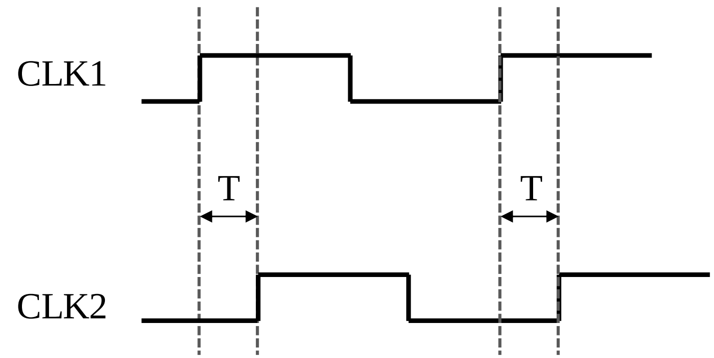
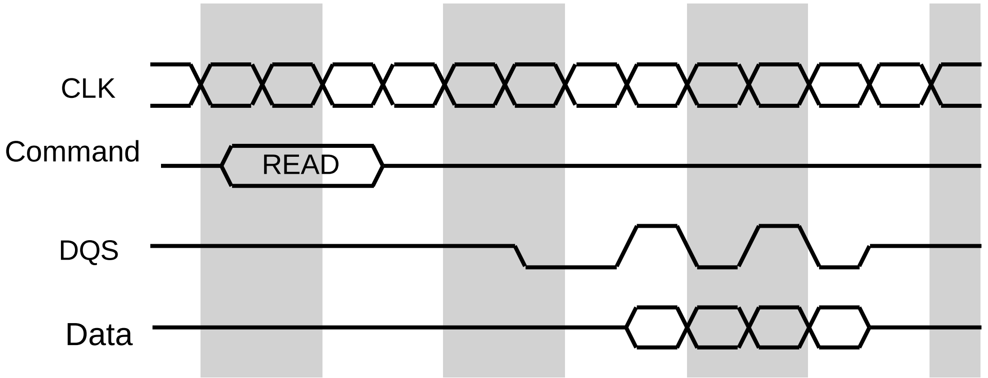
Research Purpose

- Testing timing difference
  between two repetitive digital signals
  Ex.
  Data and clock
  in Double Data Rate (DDR) memory



- Short testing time
- Good accuracy

Implement with small circuitry



Our Work

Focus on Multi-bit ΔΣ Time-to-Digital Converter (TDC)

- Repetitive digital signals

  ⇨ ΣΔ TDC can be used
- Simple circuit
- Fine resolution
- Testing time

  Single-bit ΣΔ TDC Long

  Multi-bit ΣΔ TDC Short
- Linearity

  Single-bit ΣΔ TDC Good

  Multi-bit ΣΔ TDC Bad due to delay elements mismatches

⇩

Two methods for their compensation

↳ DWA & Self-calibration

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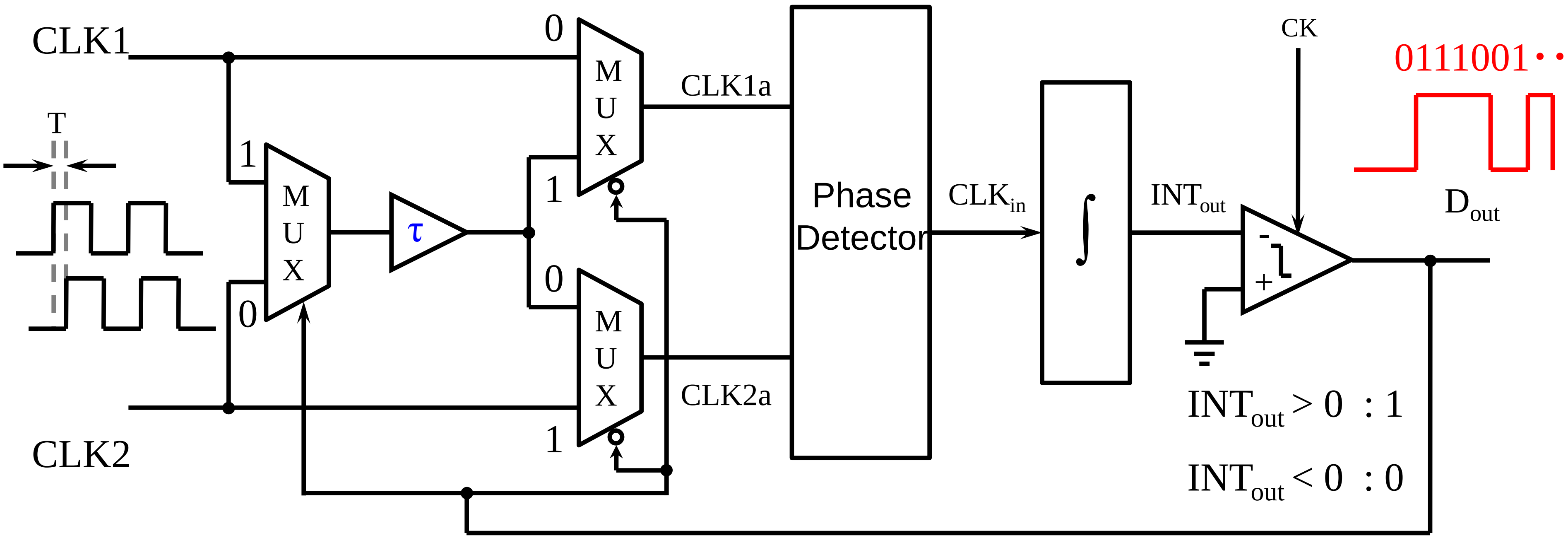
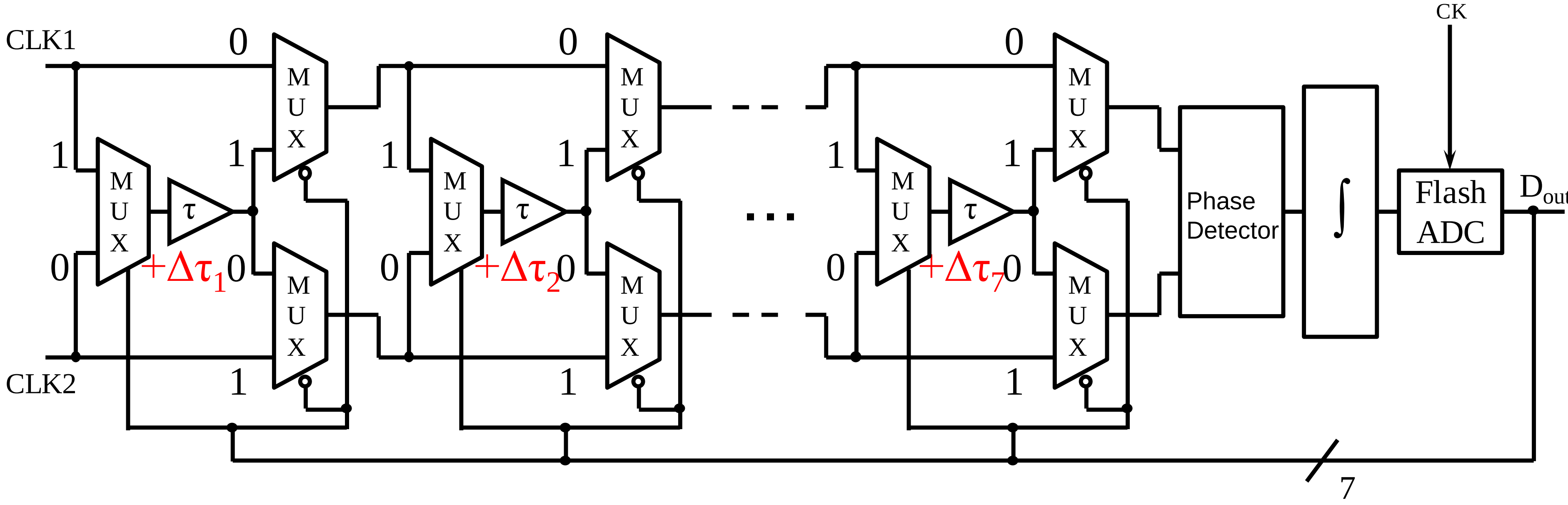
Single-Bit ΣΔ TDC



- Measurement of timing *T* between repetitive CLK1 and CLK2
- Number of 1's at *Dout* is proportional to *T*
- Time resolution becomes finer as measurement time becomes longer

Note: τ is not time resolution, but time measurement full range

Multi-Bit ΣΔ TDC



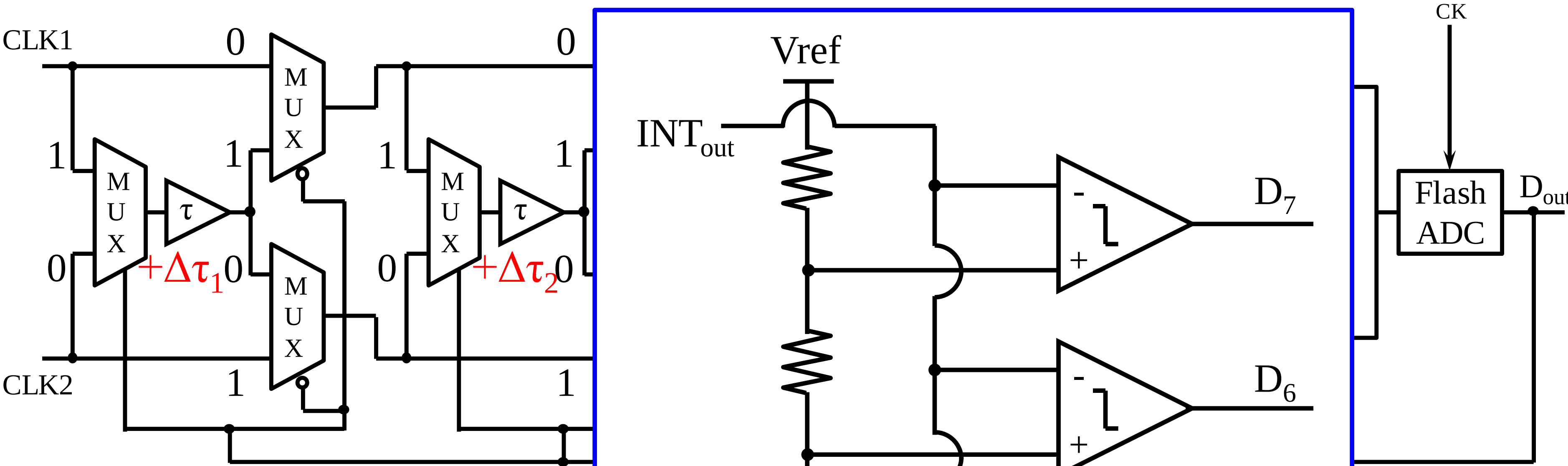
- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

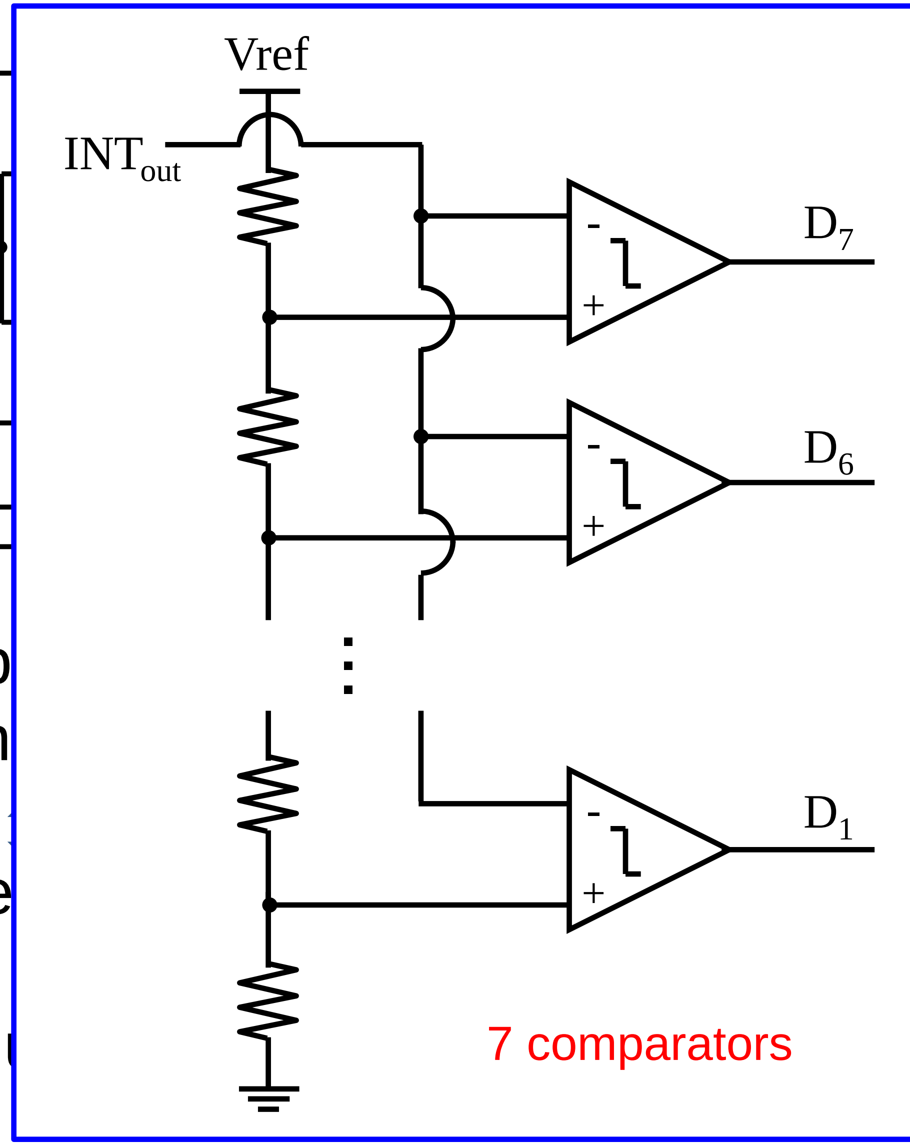
⇕

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.

Multi-Bit ΣΔ TDC



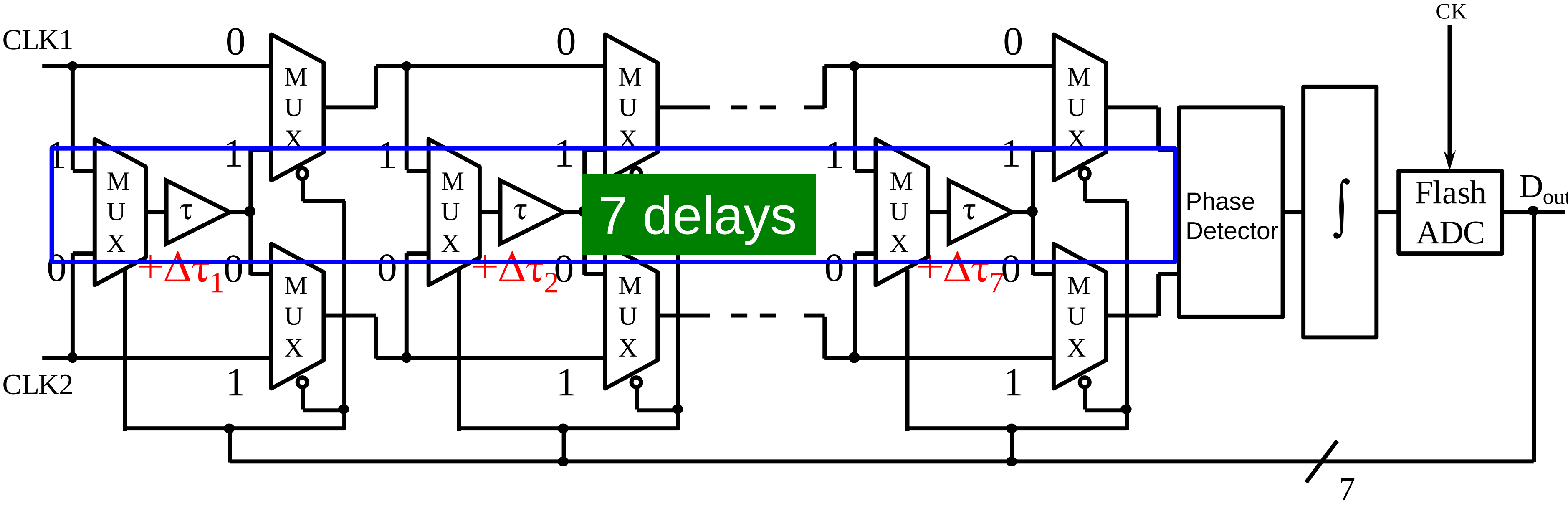


- 3-bit : 2^3-1 =7 comp
- Fine time resolution

  Shorter measureme … on

- TDC non-linearity d … cells

Multi-Bit ΣΔ TDC



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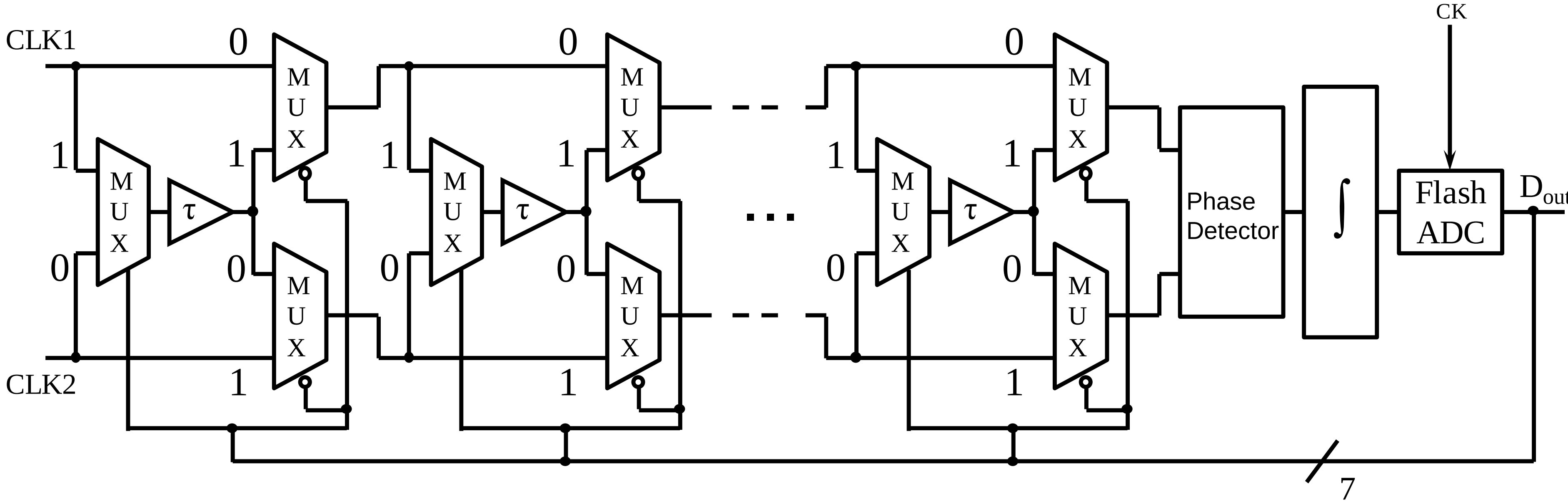
Multi-Bit ΣΔ TDC



- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

⇕

Shorter measurement time with a given time resolution

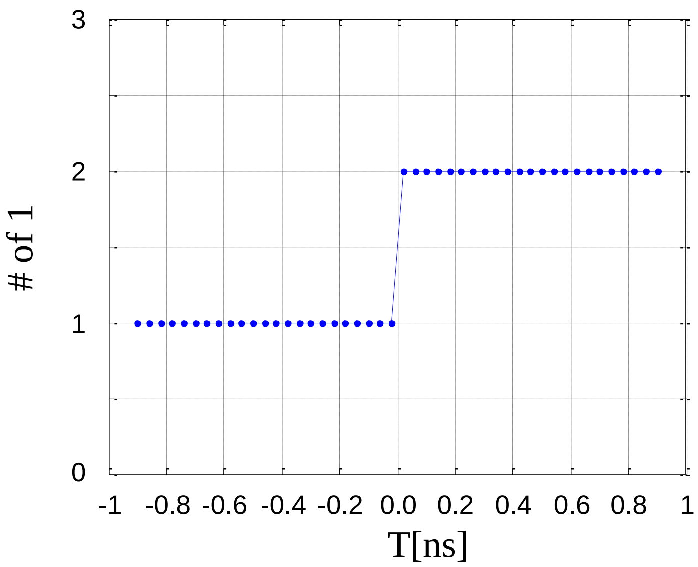
- TDC non-linearity due to mismatches among delay cells

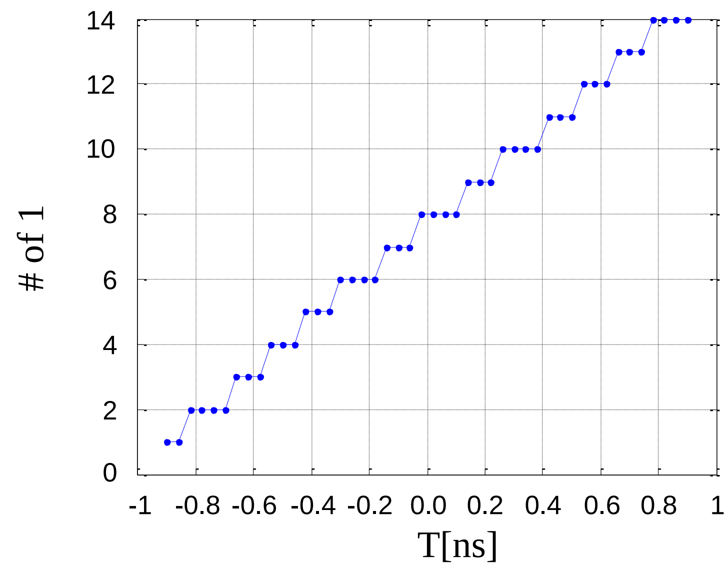
Difference in Measurement Time

- Simulation conditions

	1-bit ΣΔ TDC	3-bit ΣΔ TDC
Rising timing edge difference (T)	-0.9 ～ 0.9[ns] (Resolution : 0.04[ns])	-0.9 ～ 0.9[ns] (Resolution : 0.04[ns])
Delay time (τ)	1[ns]	0.145[ns]
The number of digital outputs	2	2

■ A rising number of outputs for the interval T



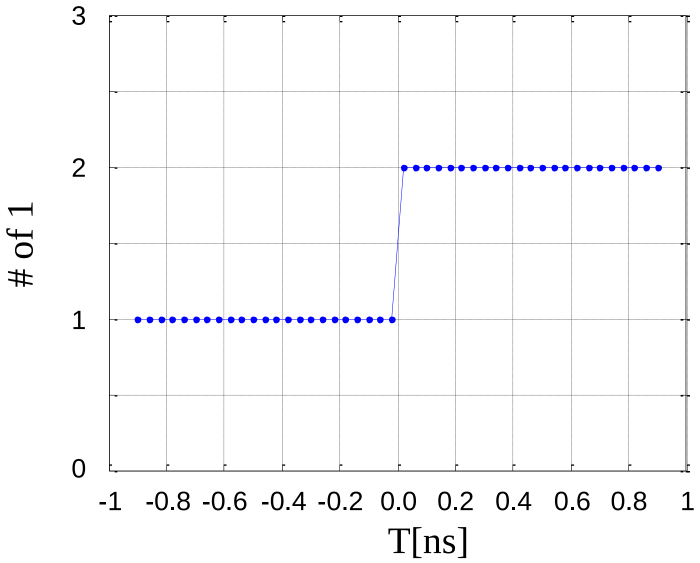


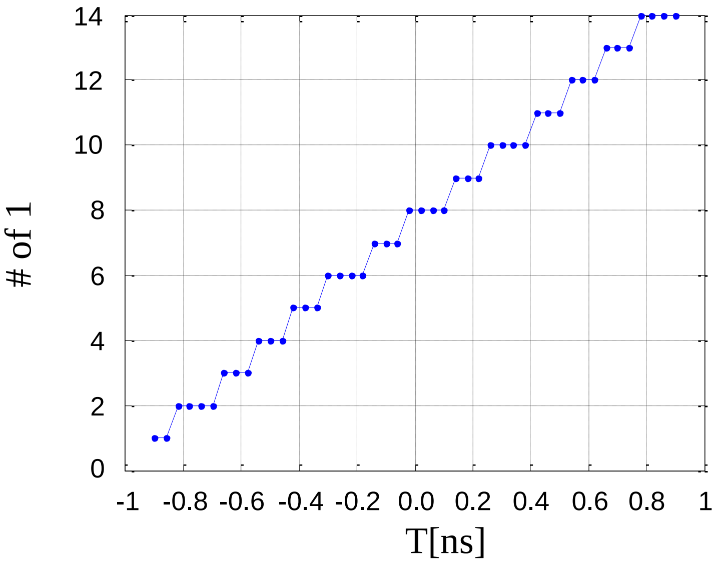
Difference in Measurement Time

✓Multi-bit takes short measurement time for a given time resolution

 **Low cost testing** 

■ A rising number of outputs for the interval T





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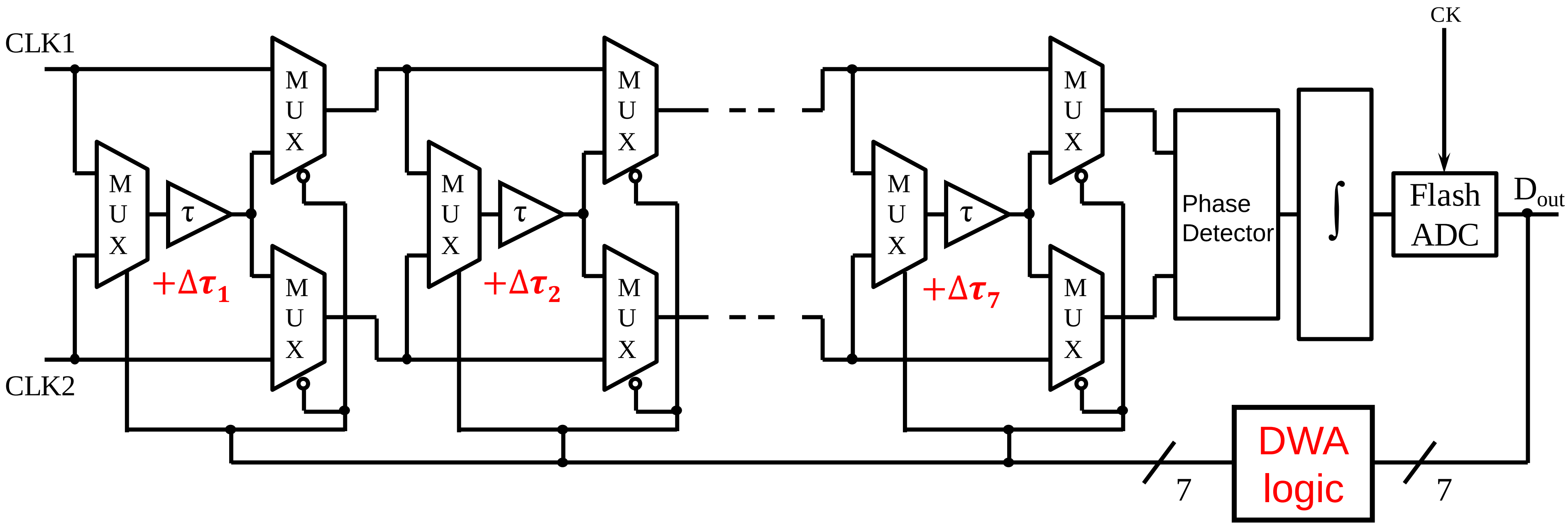
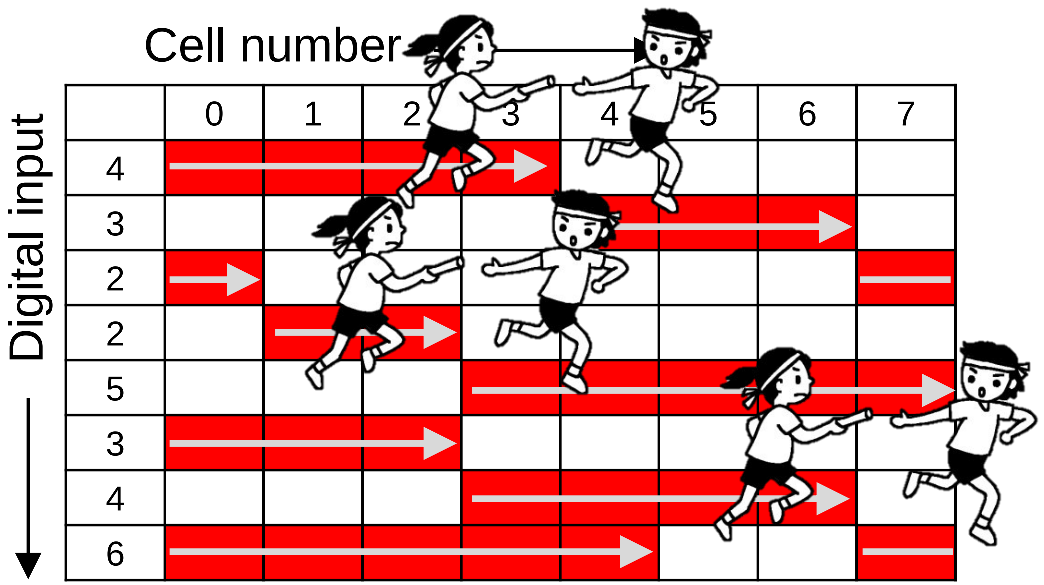
DWA (Data Weighted Averaging)



- Flash ADC outputs
  → shuffled by DWA logic,
  fed into MUXs as select signals

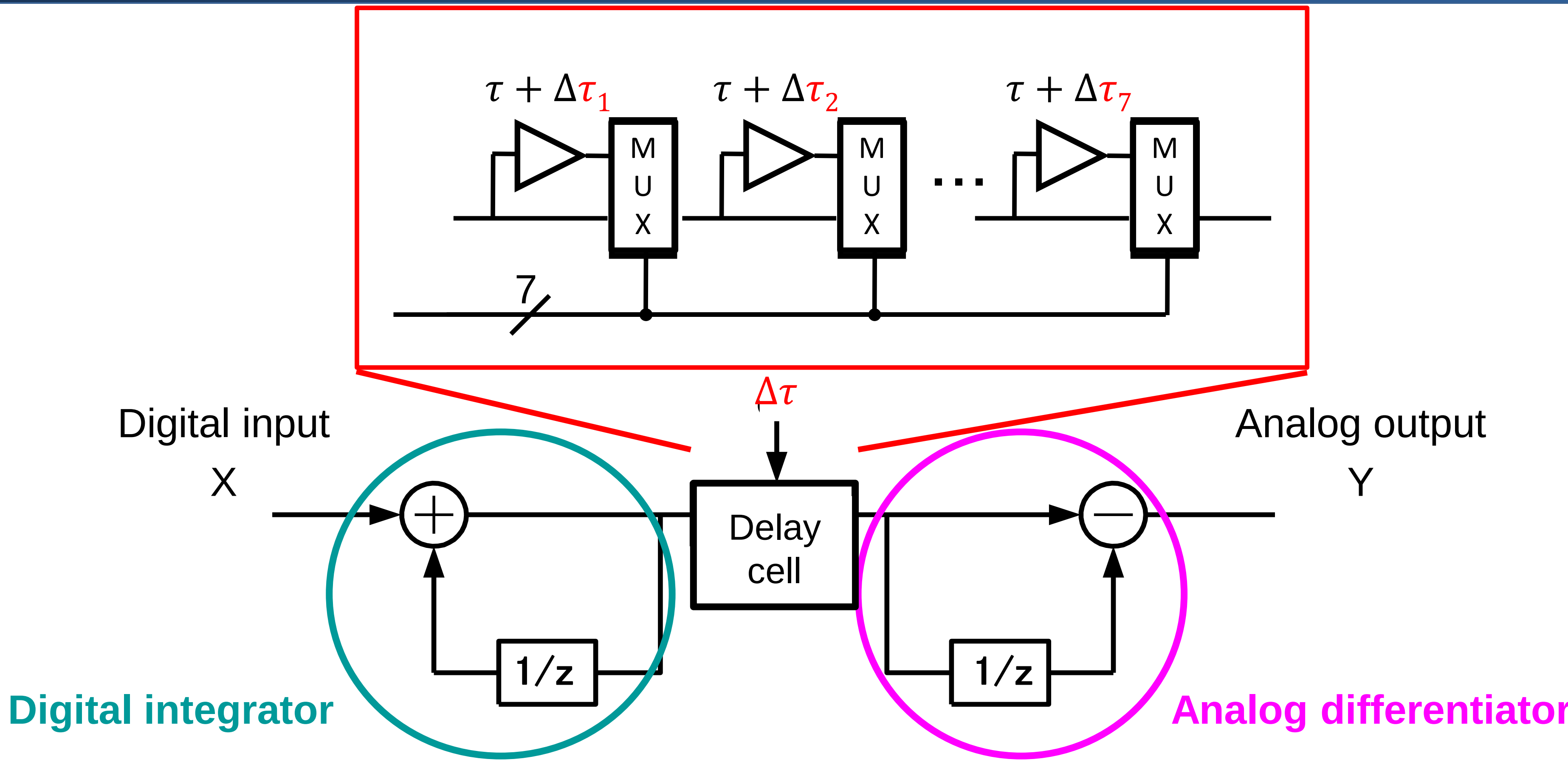
- Delay mismatch effects
  → moved to high-frequency (noise-shaping)

DWA Operation



Pass a baton in relay race !

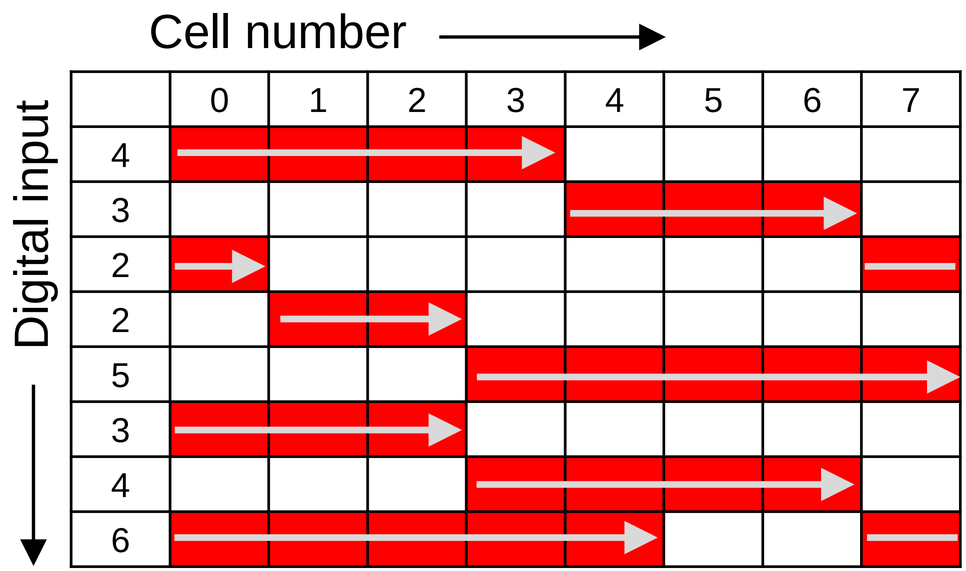
Noise-Shaping



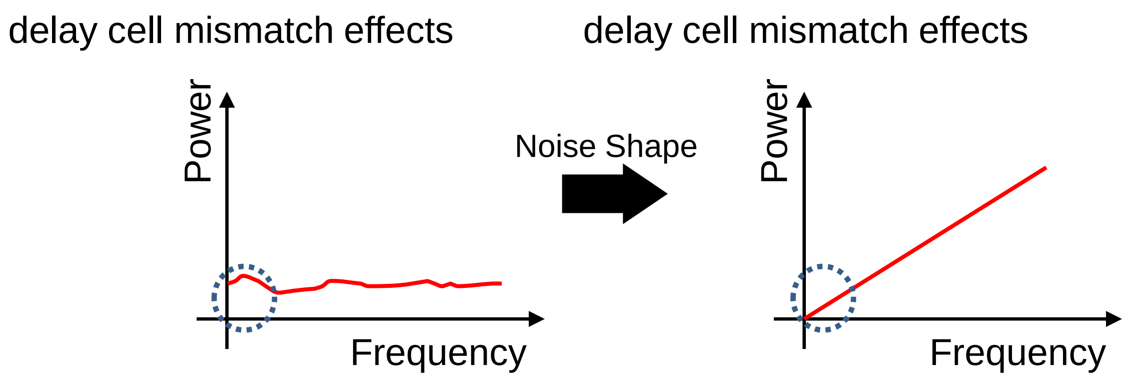
$$Y(z) = X(z) + (1 - 1/Z)\Delta\tau(z)$$

Delay mismatch $\Delta\tau$ is fist-order noise-shaping

DWA & Noise Shaping

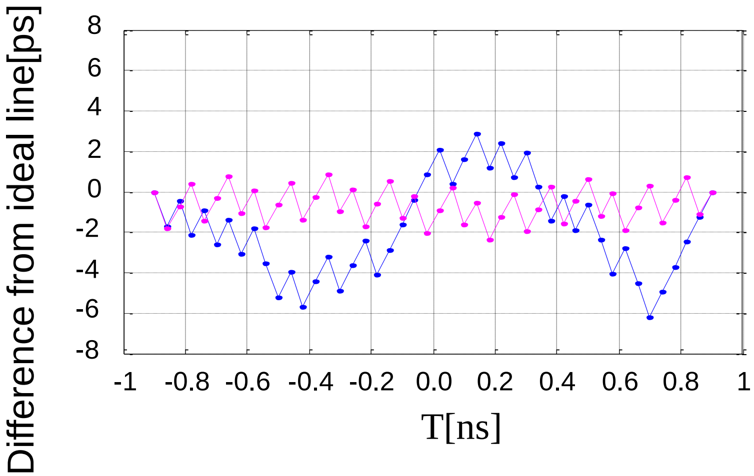


- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

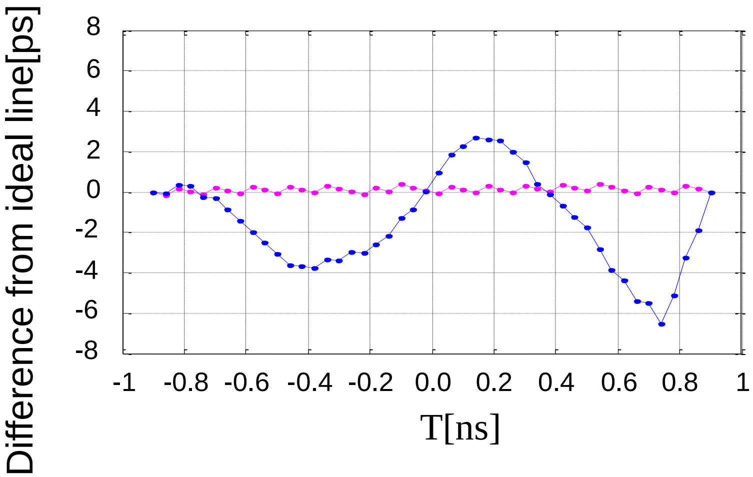


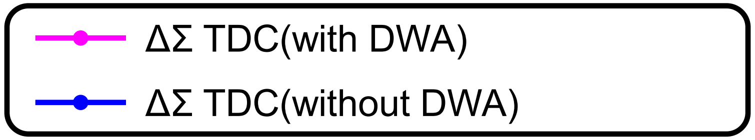
Simulation of ΔΣ TDC with DWA

- Output : 99 points



- Output : 599 points

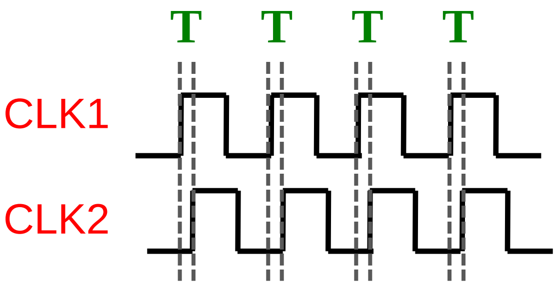




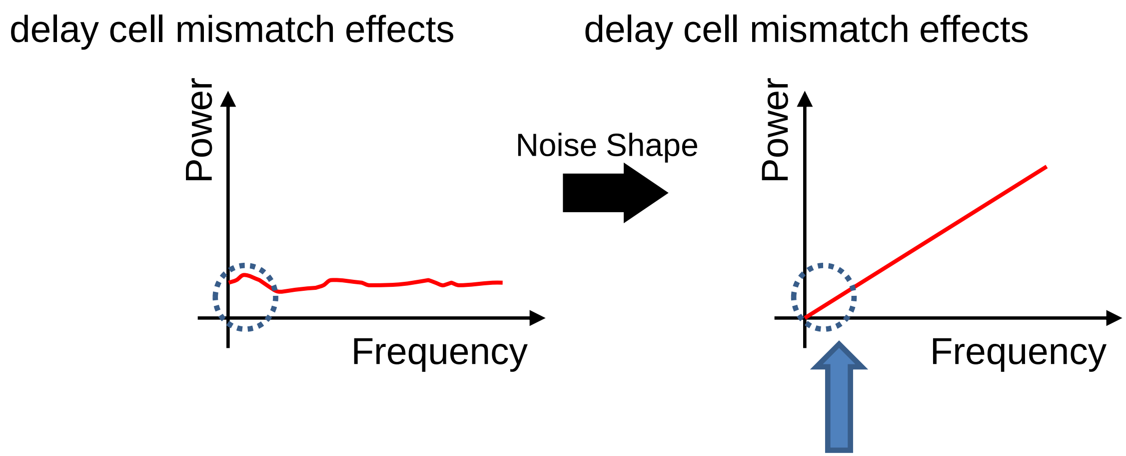
✓Reduce the effect of delay mismatches

ΣΔ TDC linearity is improved

DWA Effect



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation



Measure T

T is DC signal.

Mismatch effects
reduction at DC

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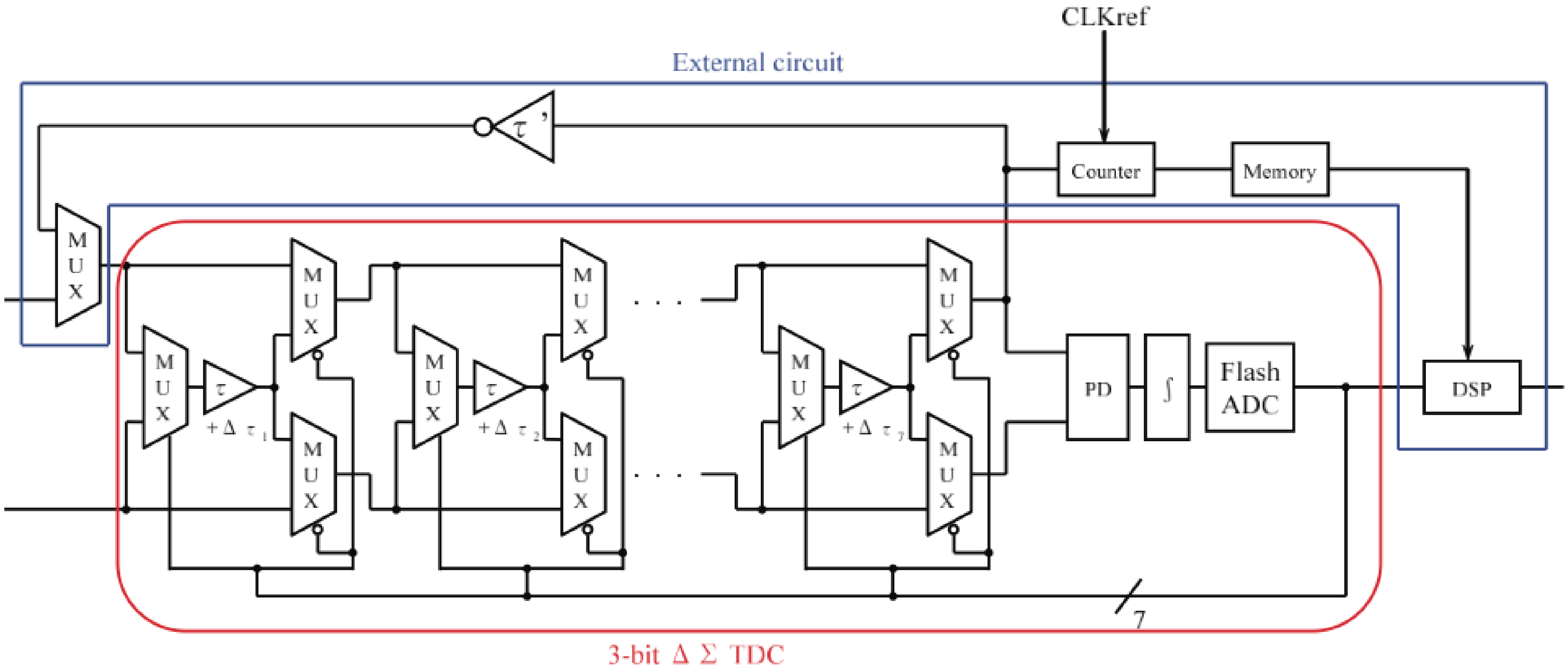
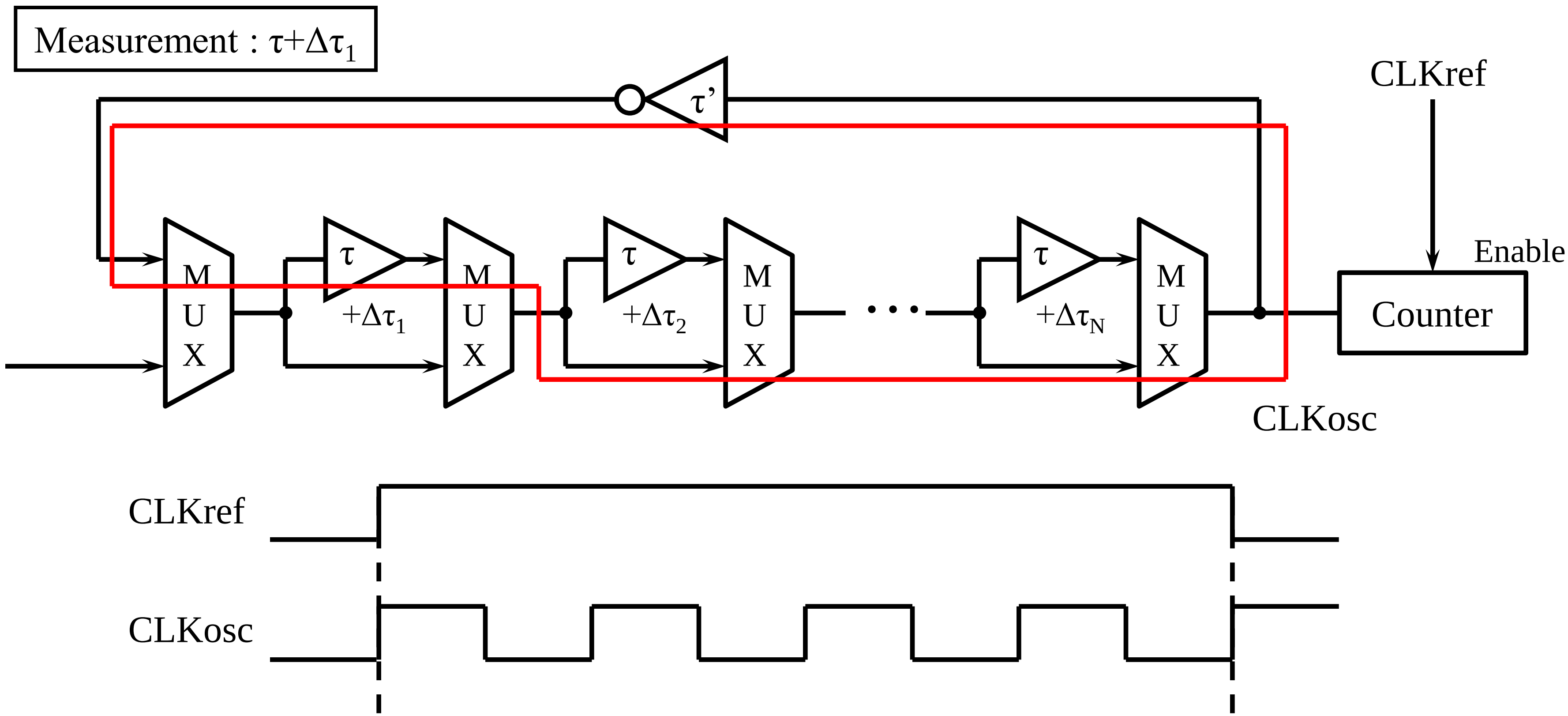
ΣΔ TDC with Self-Calibration



- Self-calibration circuit: inverter, MUX, counter, memory
- Measure delay values and store them in memory

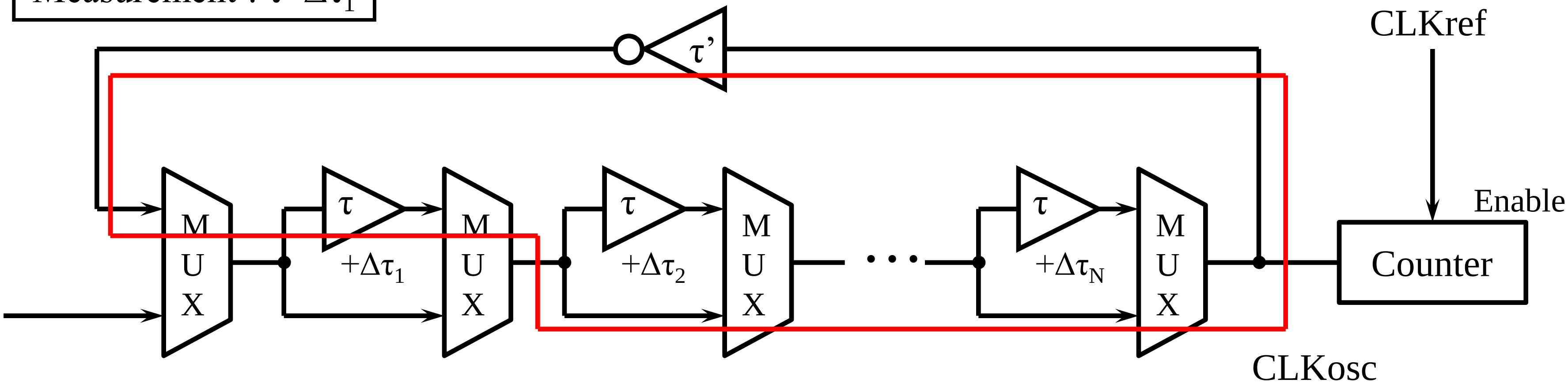
Self-Measurement of Delay



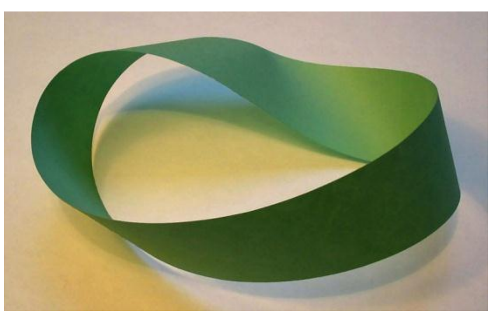
- Ring oscillator with a delay cell to be measured
- Counter measure the number of the pulses
- $\Delta\tau$ can be calculated
- Measured delay values are stored in memory

Time Signal & Ring Oscillator

Measurement : $\tau+\Delta\tau_1$

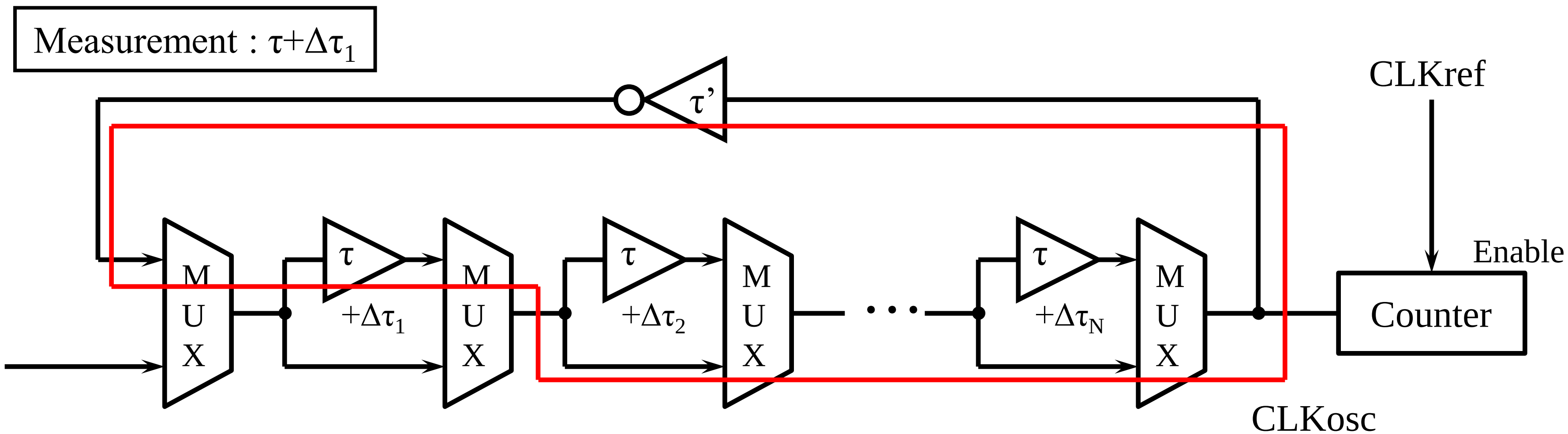


Ring oscillator



Möbius strip

Self-Measurement of Delay



Oscillation frequency

$$f = \frac{1}{2(\tau' + \tau + \Delta\tau_1)}$$

Measure

$\Delta\tau_2$、$\Delta\tau_3$, $\Delta\tau_4$、....$\Delta\tau_N$

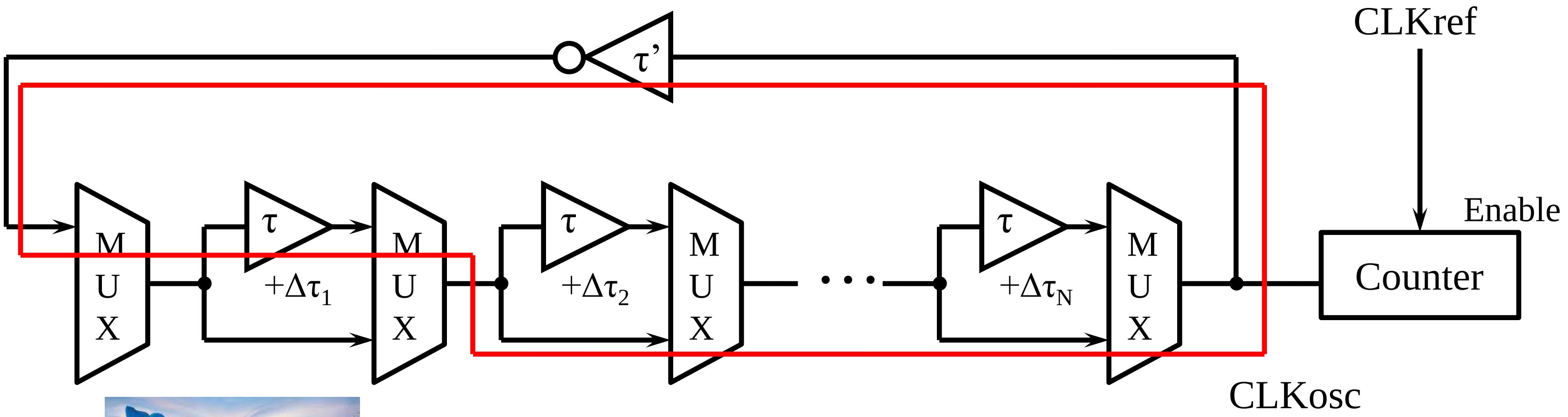
one by one.

$\Delta\tau_1$ can be calculated from the oscillation frequency

Essence of Proposed Method

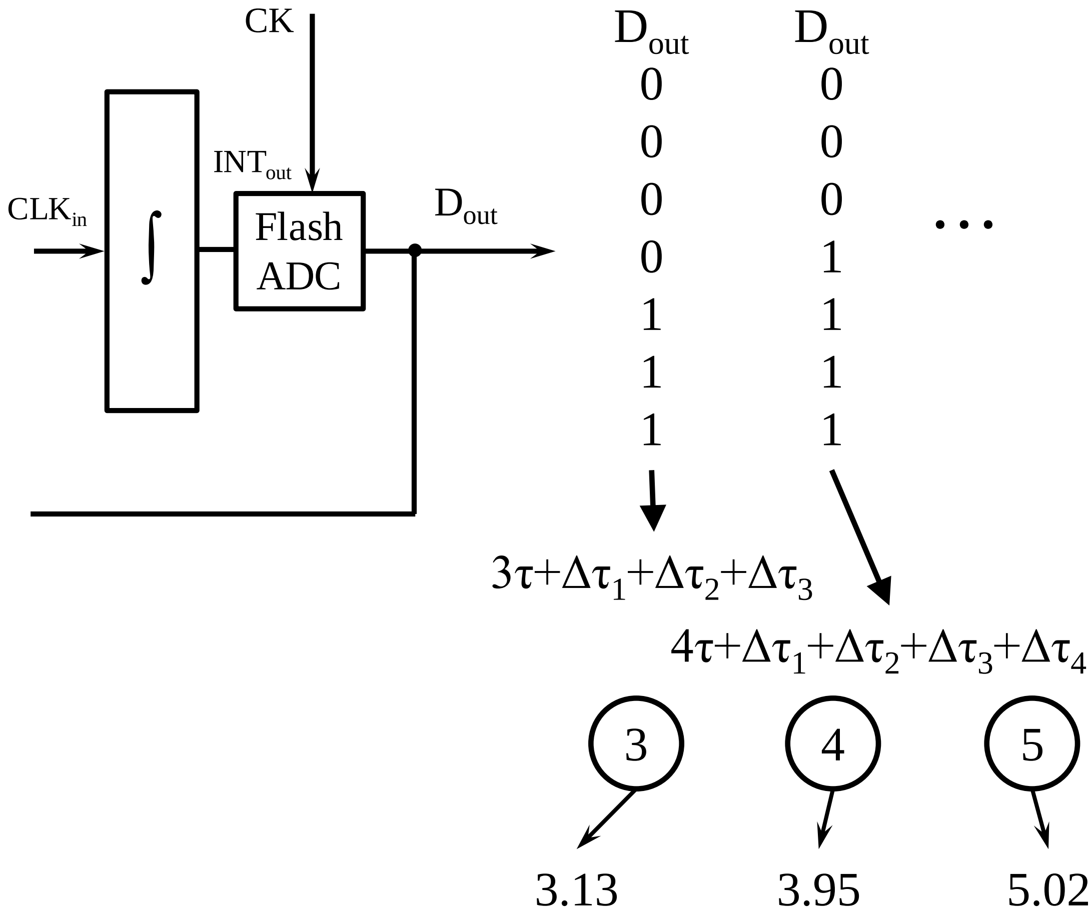
- All operations are done in digital domain
- Signal is Time instead of Voltage.

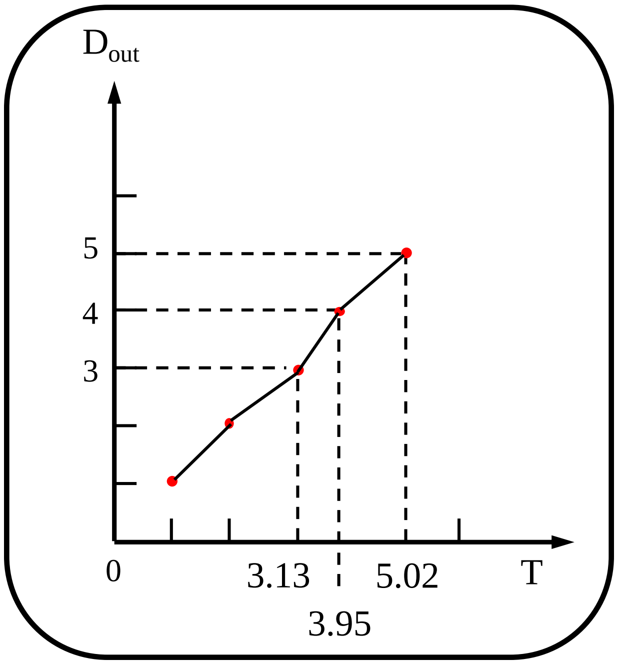
⇒ Easy, accurate measurement of $\Delta\tau$



Time flies like an arrow!

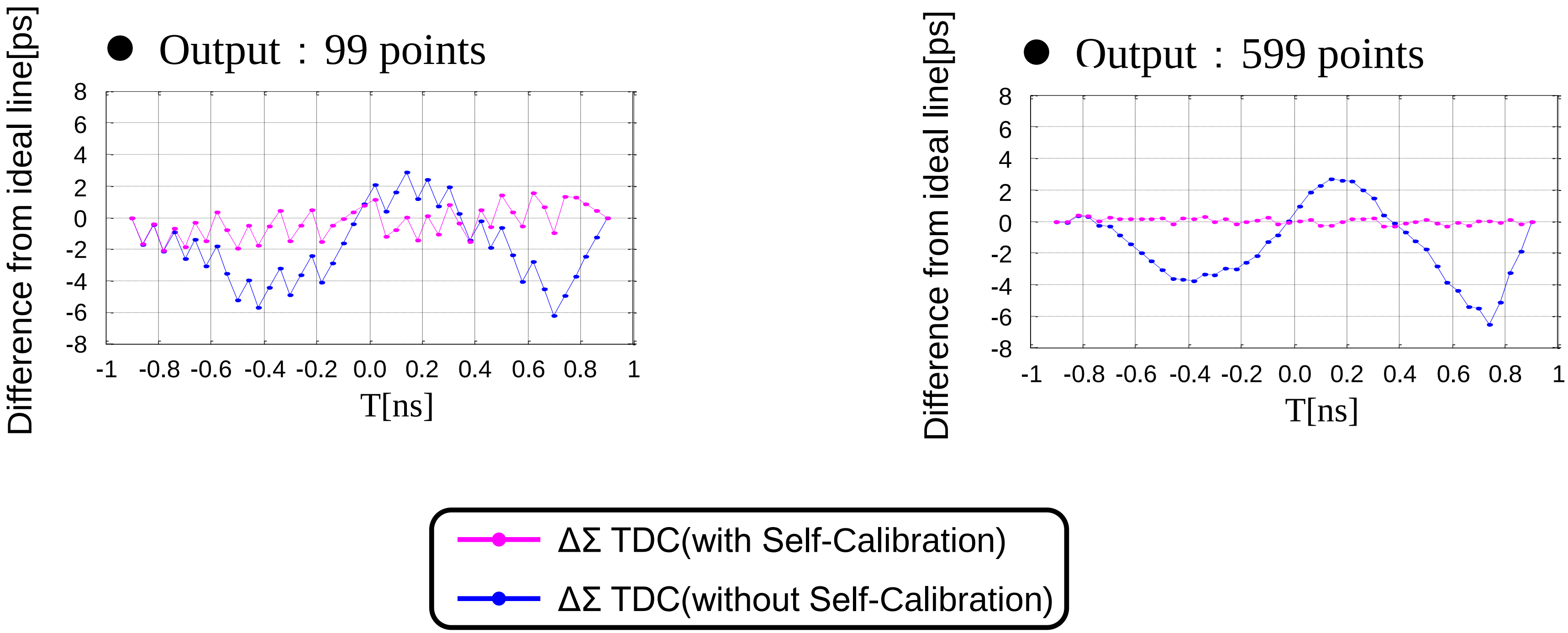
Proposed Error Correction Scheme





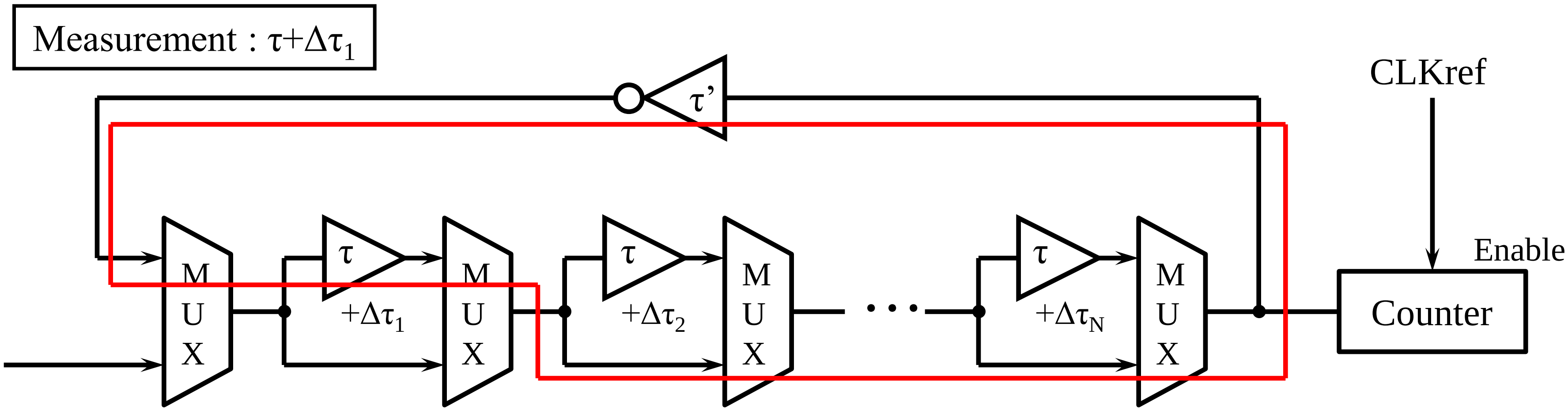
- Obtain TDC raw output (Dout) for two input clocks
- Read delay values from memory, and compensate for the output based on them

Simulation of Self-Calibration

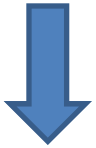


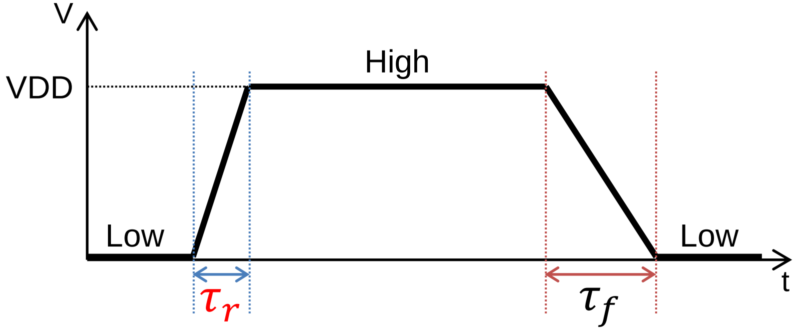
ΣΔ TDC linearity is improved

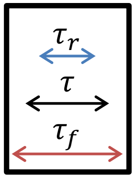
Problem of Ring Oscillator



$$f = \frac{1}{2(\tau' + \tau + \Delta\tau_1)}$$



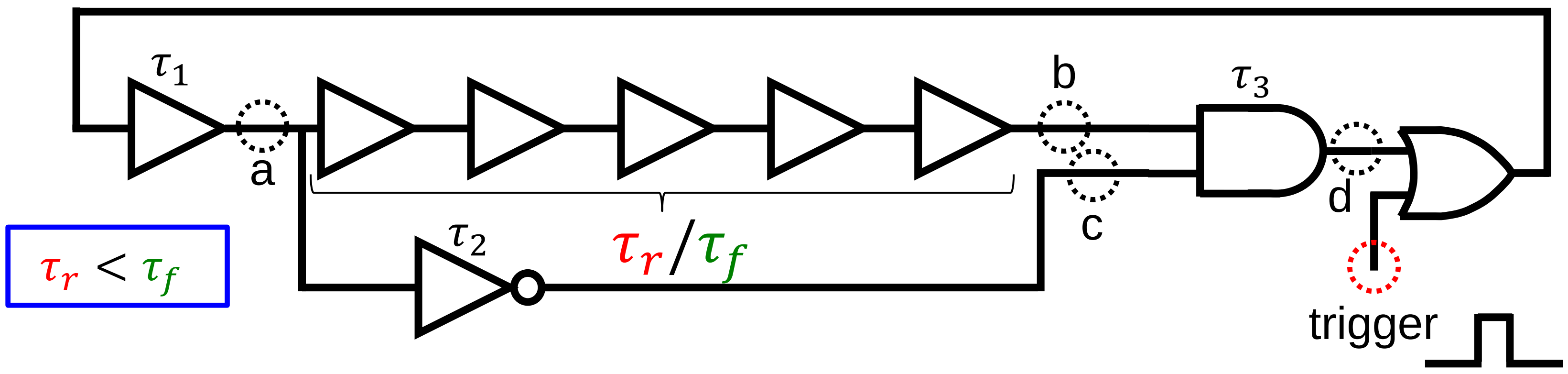




Measured delay $\tau = \frac{\tau_r + \tau_f}{2}$

However, we need the rise delay τr

Improved Delay Measurement Circuit

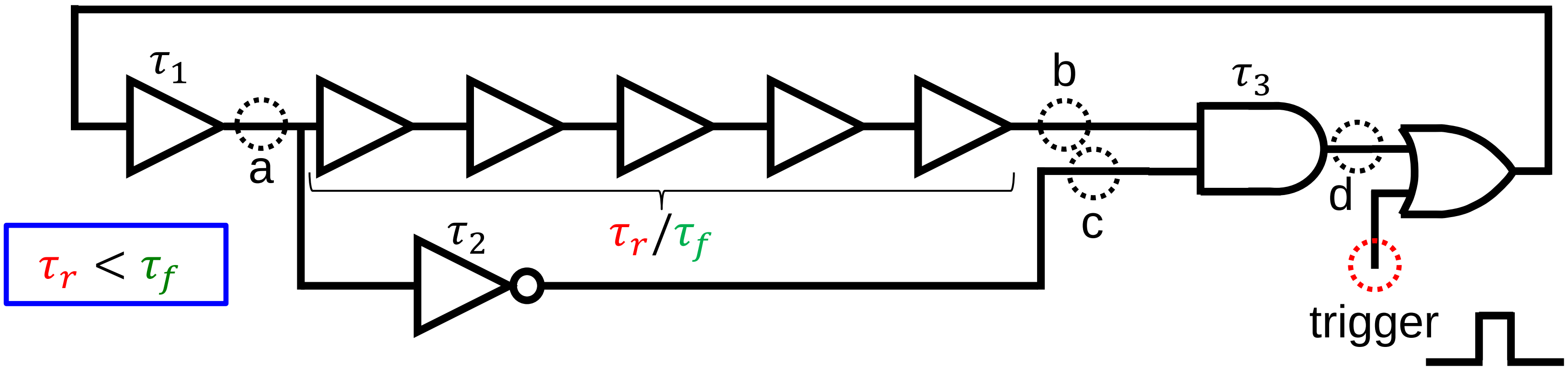


Oscillator circuit to measure

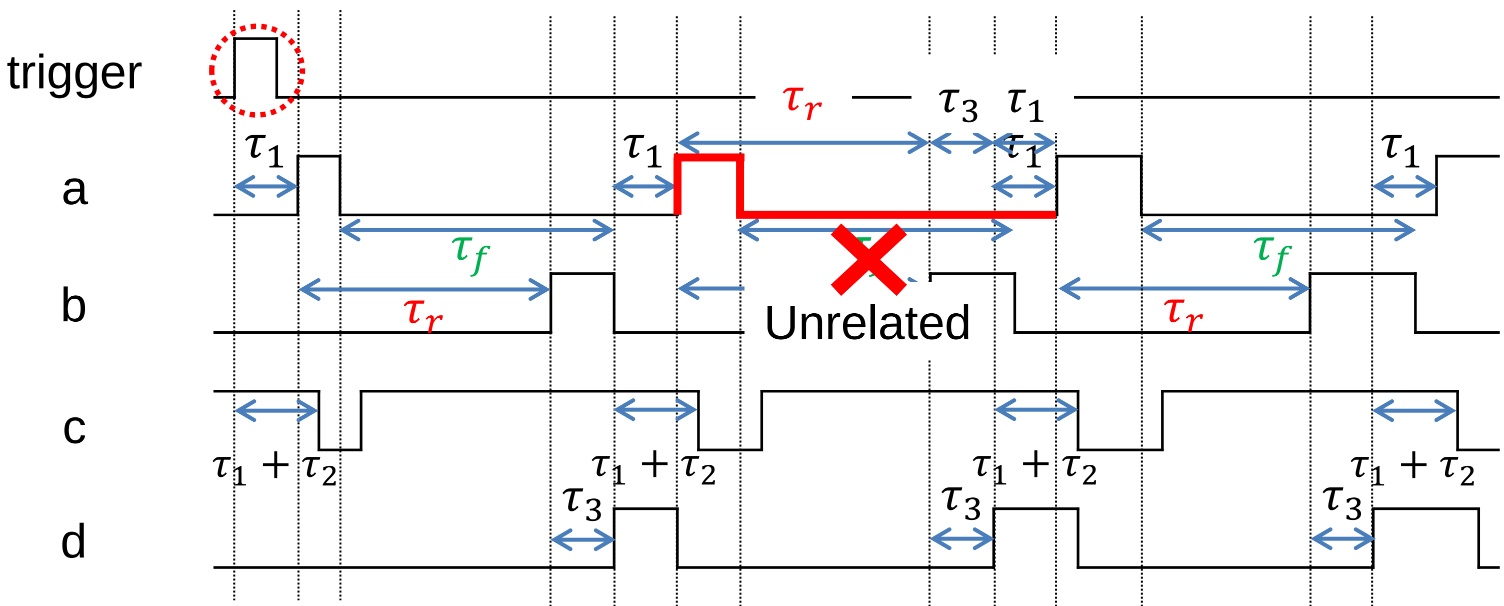
the rise delay τr of the buffer

Oscillation period is a function of τr , but NOT τf

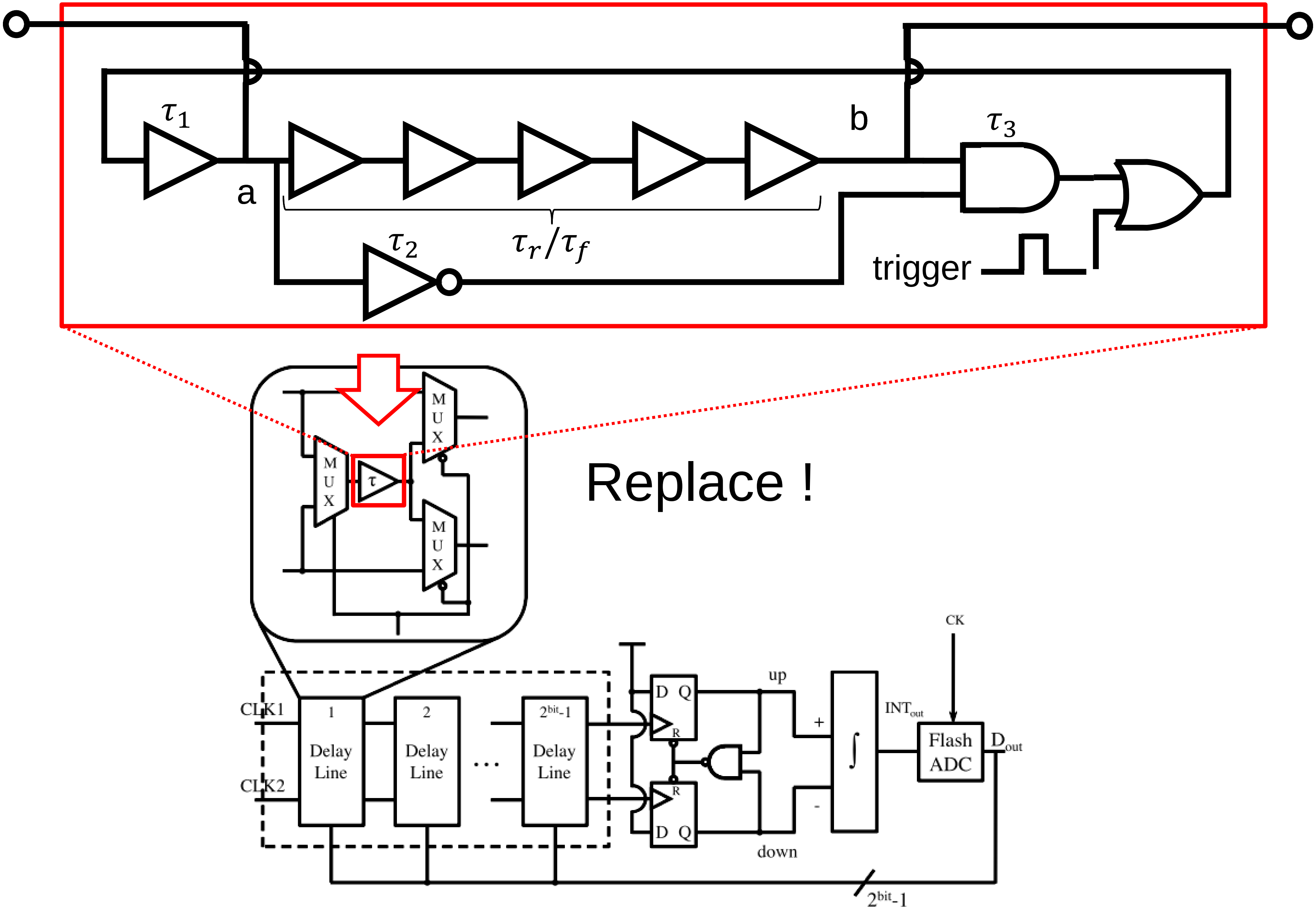
Oscillation Timing Chart



Period: $\tau 1 + \tau 3 + \tau r$



Delay with Several Buffers



Replace !

Circuit Performance Comparison

	Flash TDC	1-bit ΣΔ TDC	Multi-Bit ΣΔ TDC (without correction)	Multi-Bit ΣΔ TDC (with correction)
Area	×	◎	○	○
Resolution	×	◎	◎	◎
Accuracy	△	◎	×	◎
Time	◎	×	○	○

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Conclusion

- We propose to use ΣΔ TDC
  for digital signal timing measurement

- Multi-bit ΣΔ TDC
  - ➢ Short measurement time
  - ➢ Fine time resolution
  - ➢ Non-linearity due to mismatches among delay cells

  ⇨ Two techniques to improve linearity
  - – DWA
  - – Self-Calibration (signal is “time”)

Low cost, high quality digital timing test can be realized

Kobayashi Laboratory

Time makes GOLD !!

Appendix

How to Calculate the Delay Time

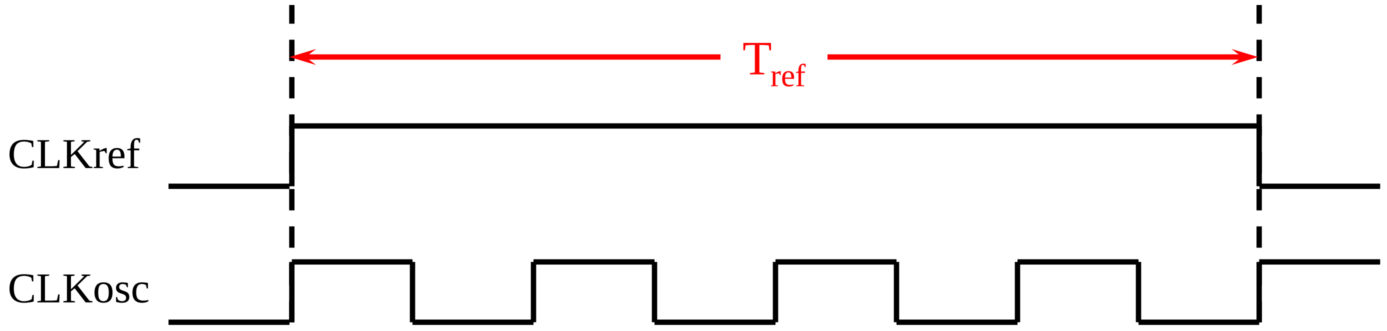
$$f_{OSC}^{k} \approx \frac{M_k}{T_{ref}} = \frac{1}{2(\tau' + \tau_k)}$$

$$\tau_k = \tau + \Delta\tau_k$$

$$f_{OSC}^{0} \approx \frac{M_0}{T_{ref}} = \frac{1}{2\tau'}$$

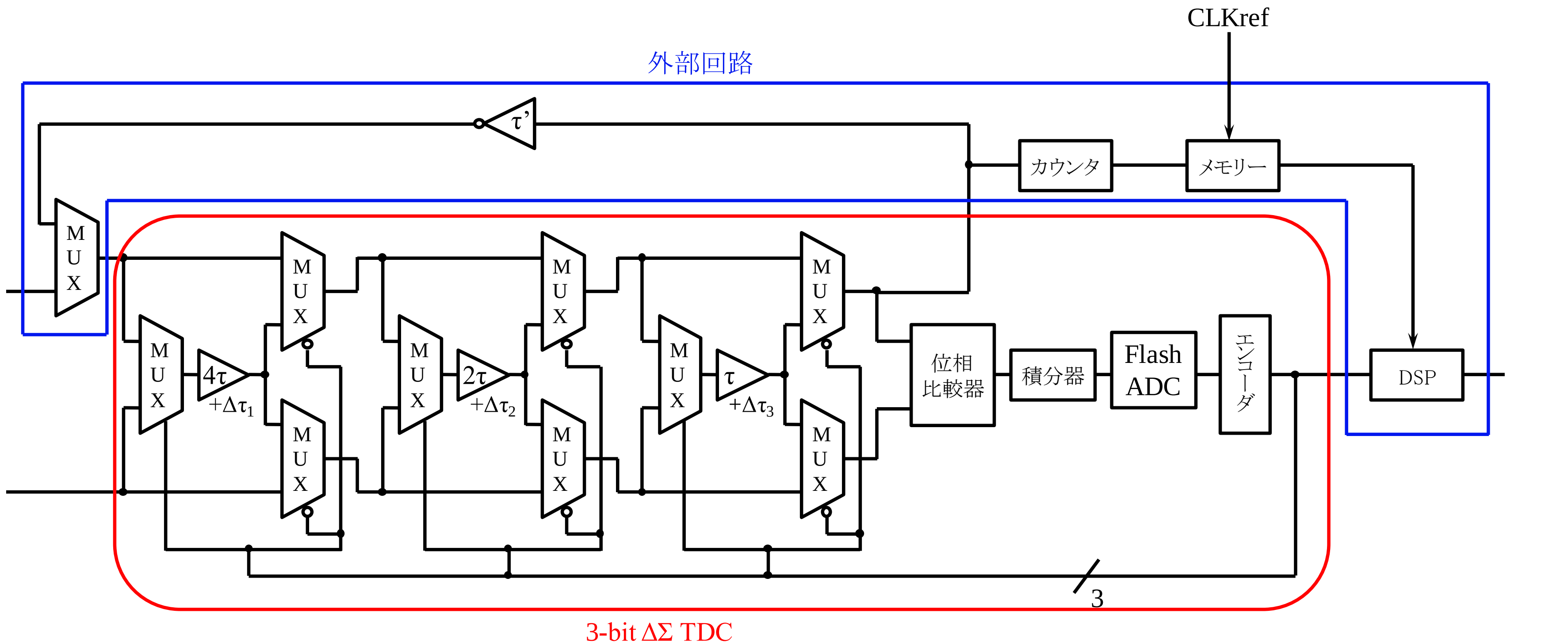
$$\tau_k = \frac{1}{2}\left(\frac{1}{f_k} - \frac{1}{f_0}\right) \approx \frac{T_{ref}}{2}\left(\frac{1}{M_k} - \frac{1}{M_0}\right)$$

k=1, 2, …, 2^N-1



Number of Pulses : M_k

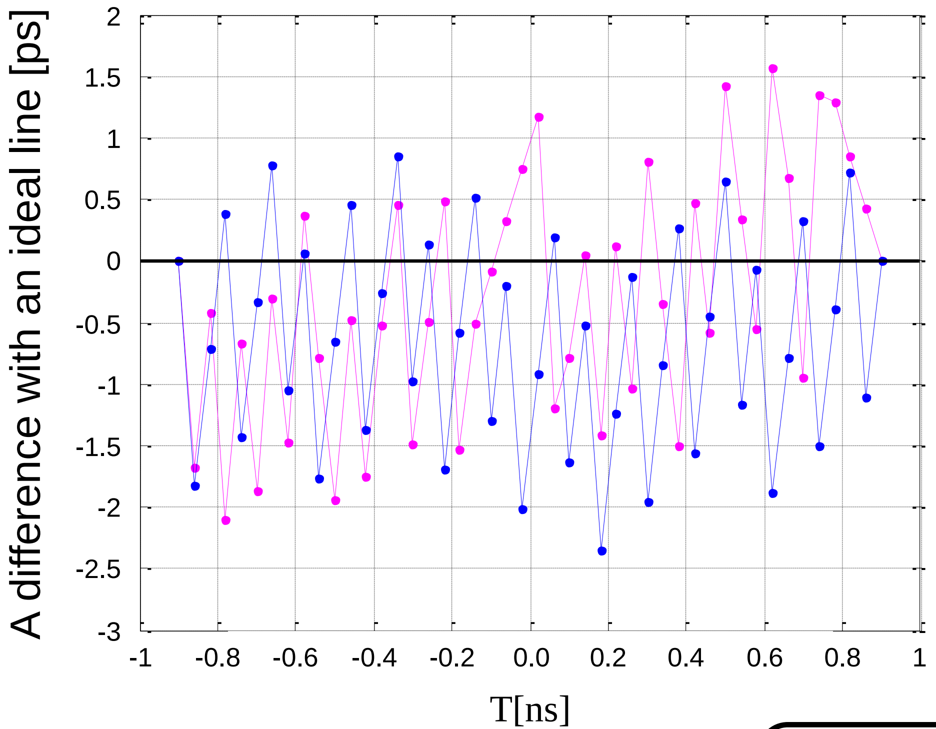
TDC Circuit with Self-Calibration



- 各遅延値に重みをもたせる
- 測定にはN-bit で Nステップかかる

Comparison of Linearity

▪3-bit ΔΣ TDC (Delay Time(Ideal) : |=0.145ns)



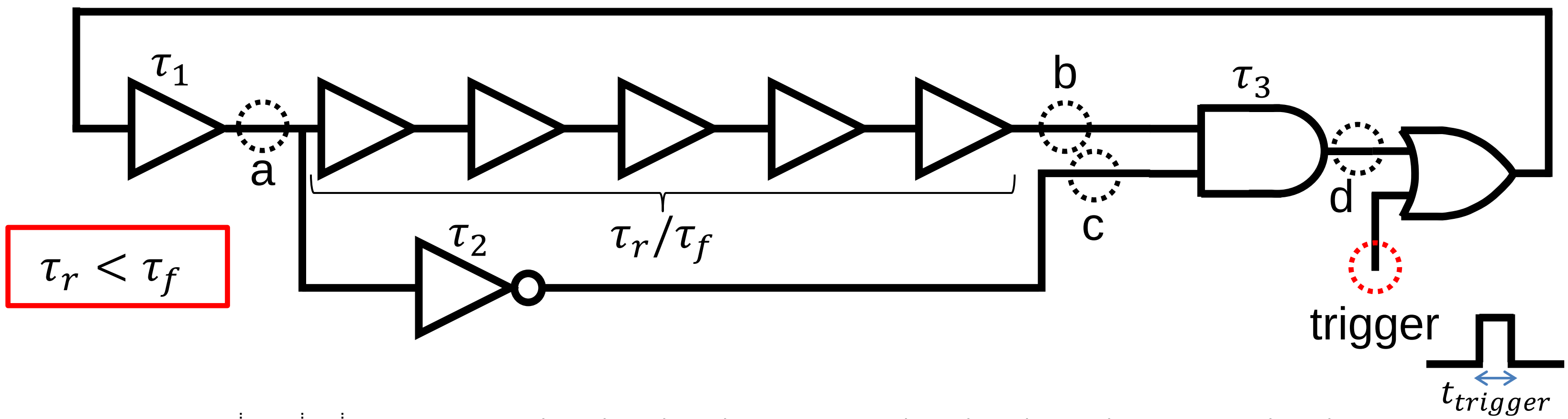
出力数99点において

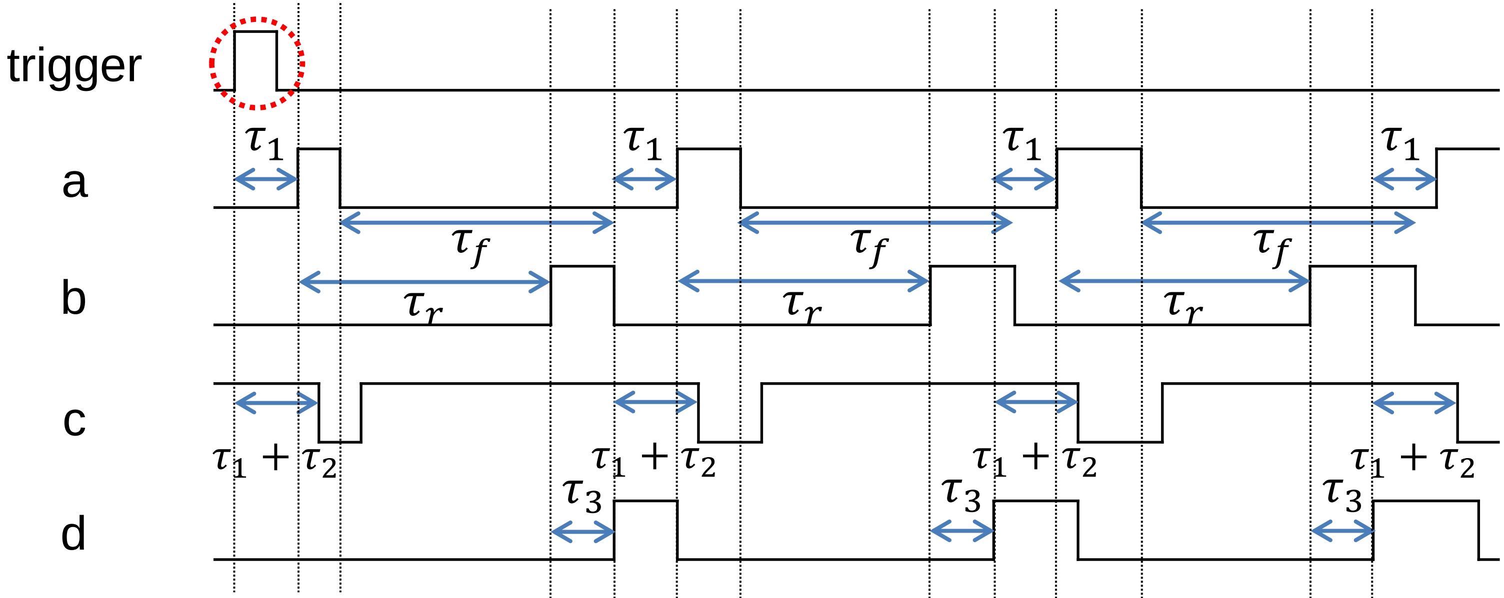
- 理想状態 ：±2 ps 以内の差
- 補正後　 ：±2.5 ps 以内の差
  - ➢ 線形性がほぼ理想状態まで改善

Detail of Oscillation timing chart

Timing chart

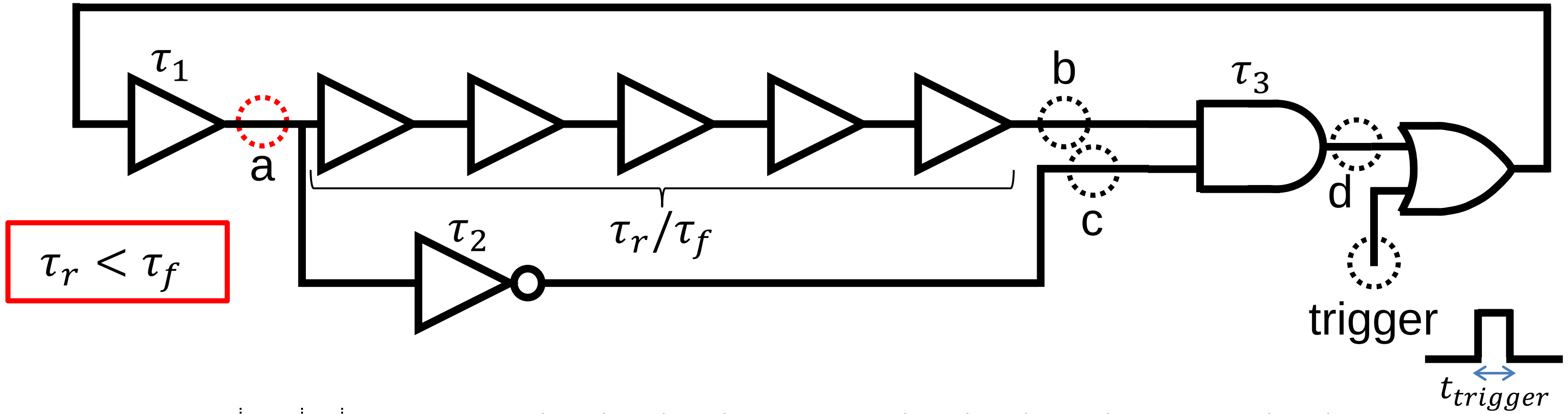
Input trigger

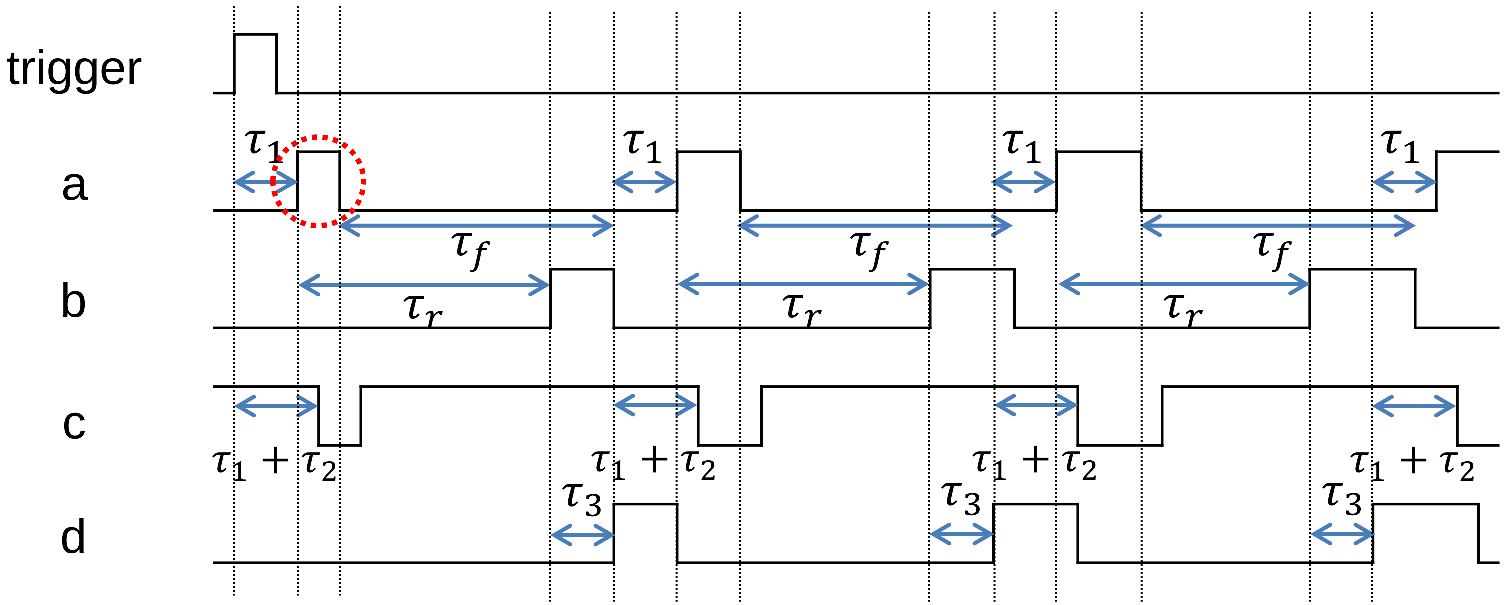




Timing chart

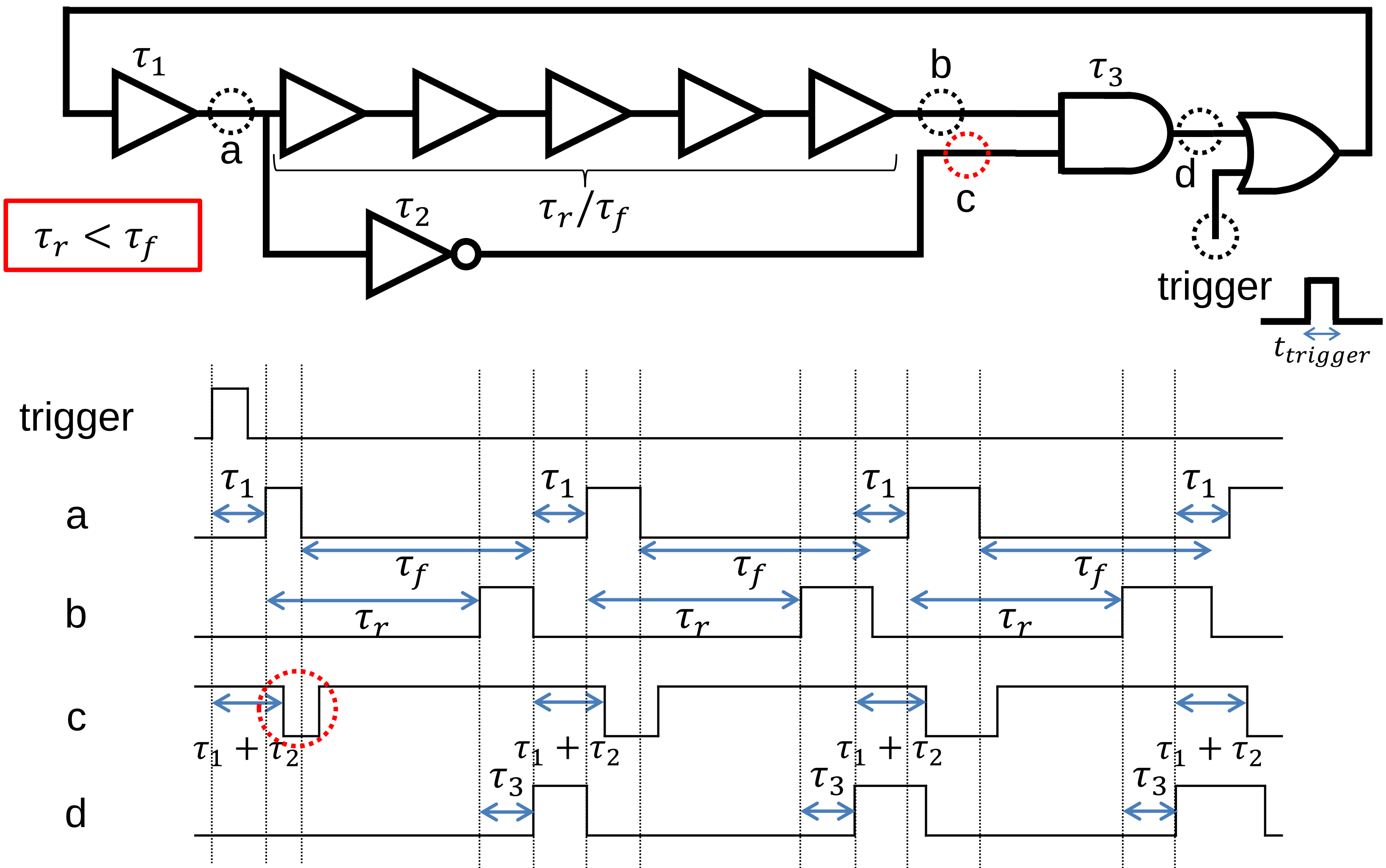
Buffer out put “a” is rises from low to high level after τ_1





Timing chart

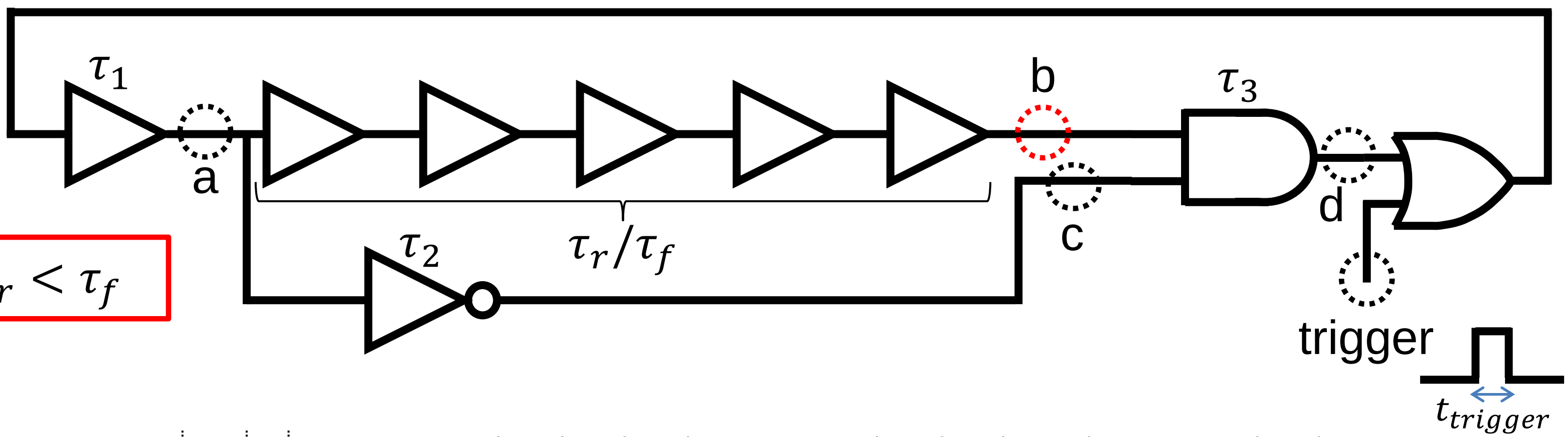
Inverter out put “c” is falls from high to low level after τ_2

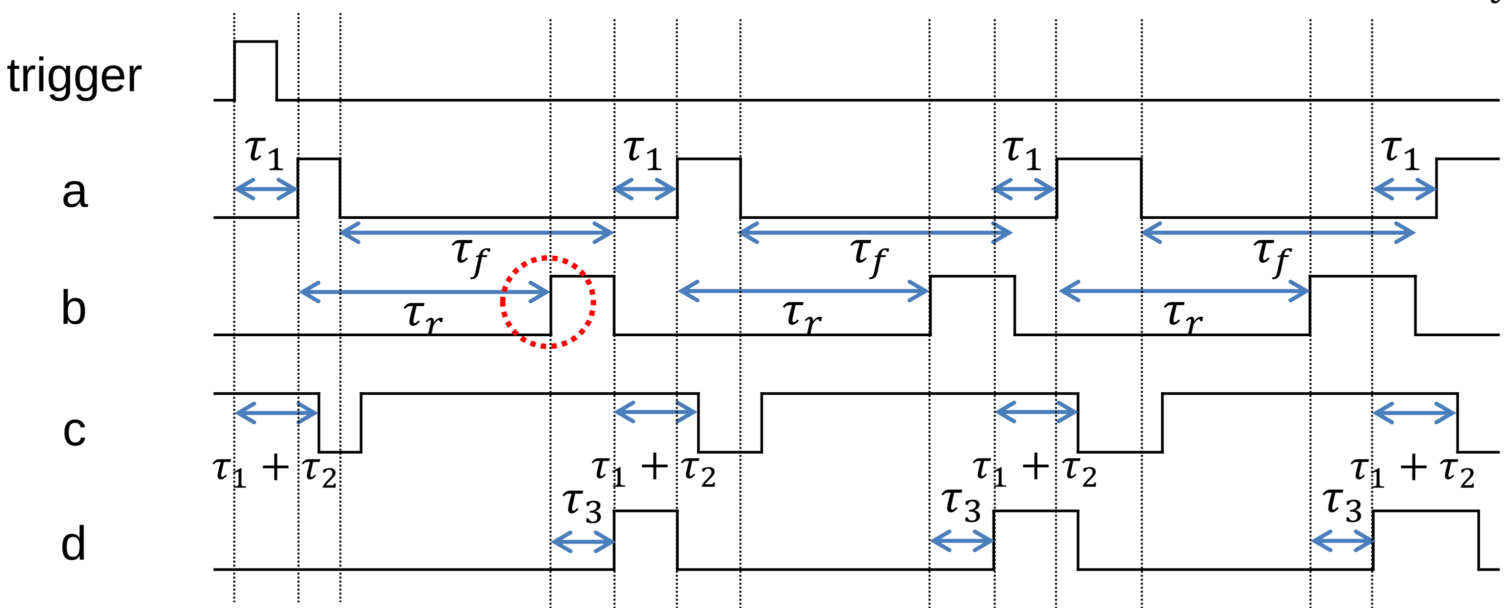


Timing chart

5 buffers out put "b" is rises from low to high level after τ_r

$\tau_r < \tau_f$

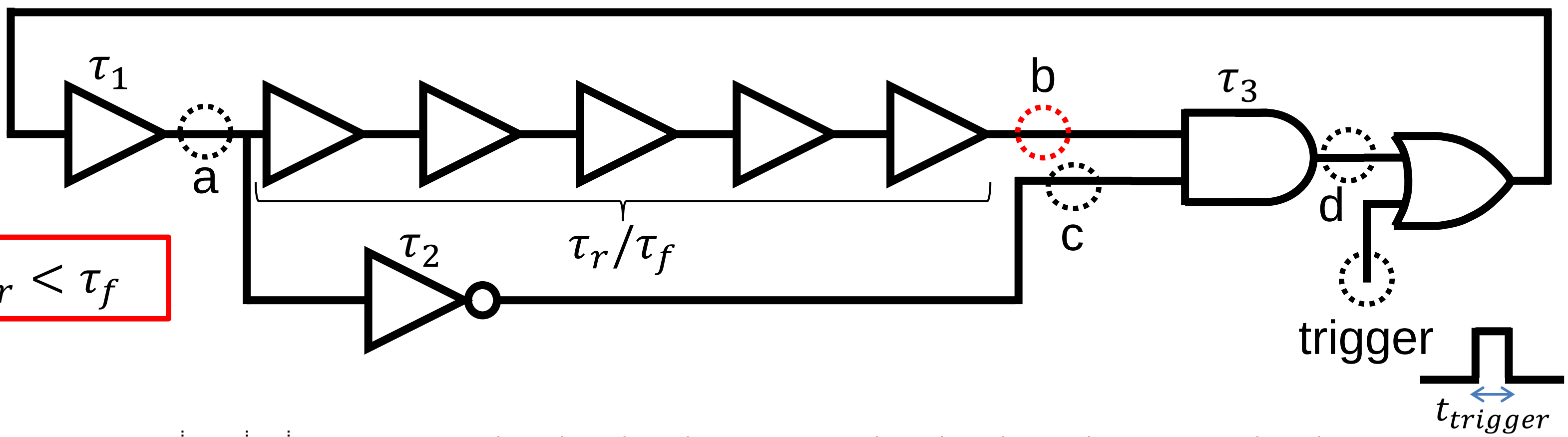


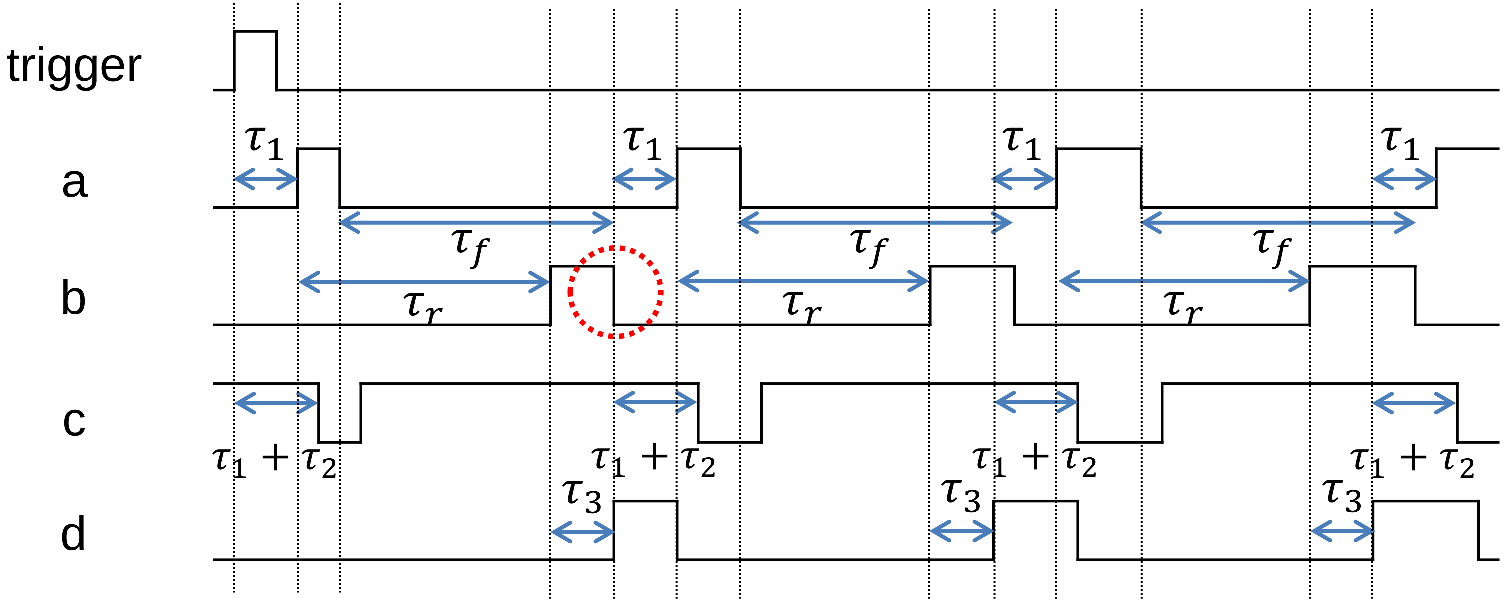


Timing chart

5 buffers out put “b” is falls from high to low level after τ_f

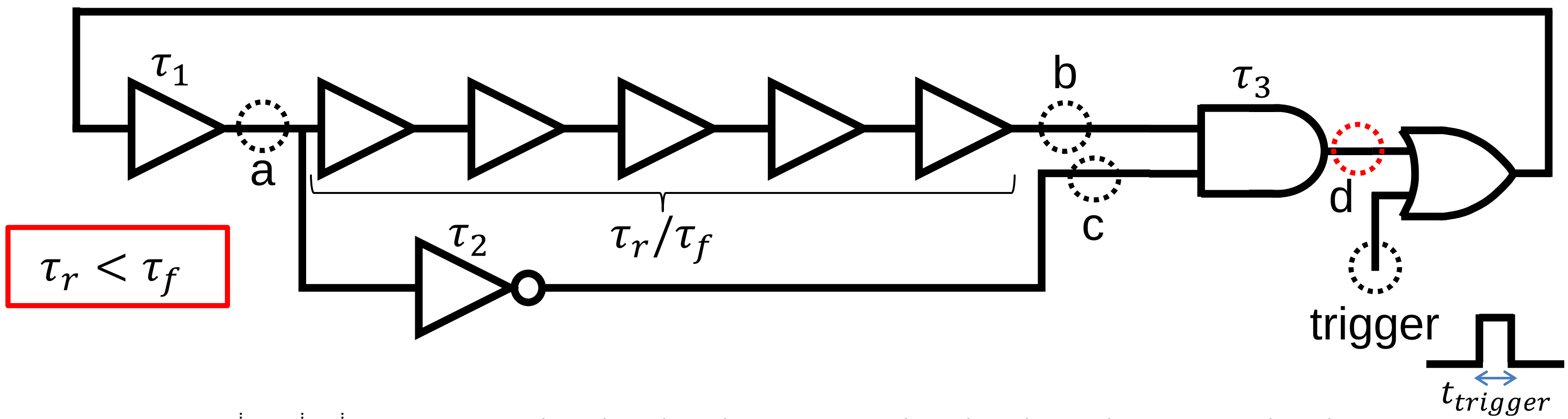
$\tau_r < \tau_f$

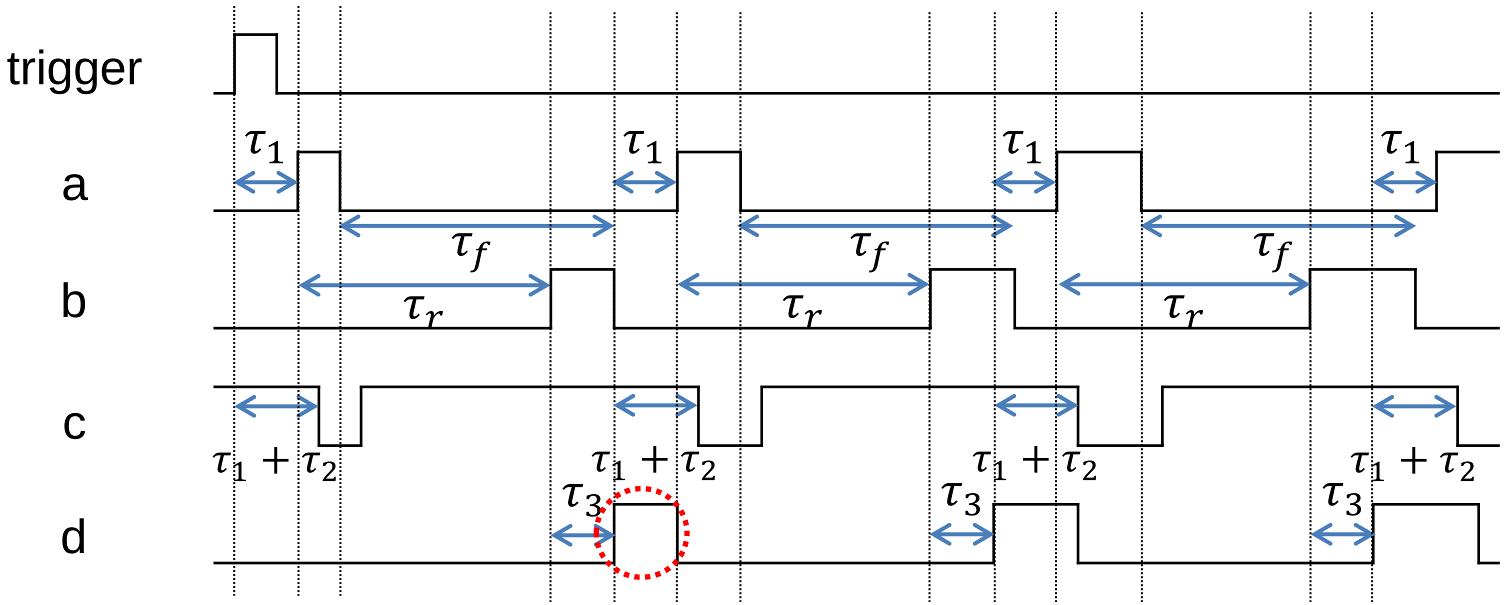




Timing chart

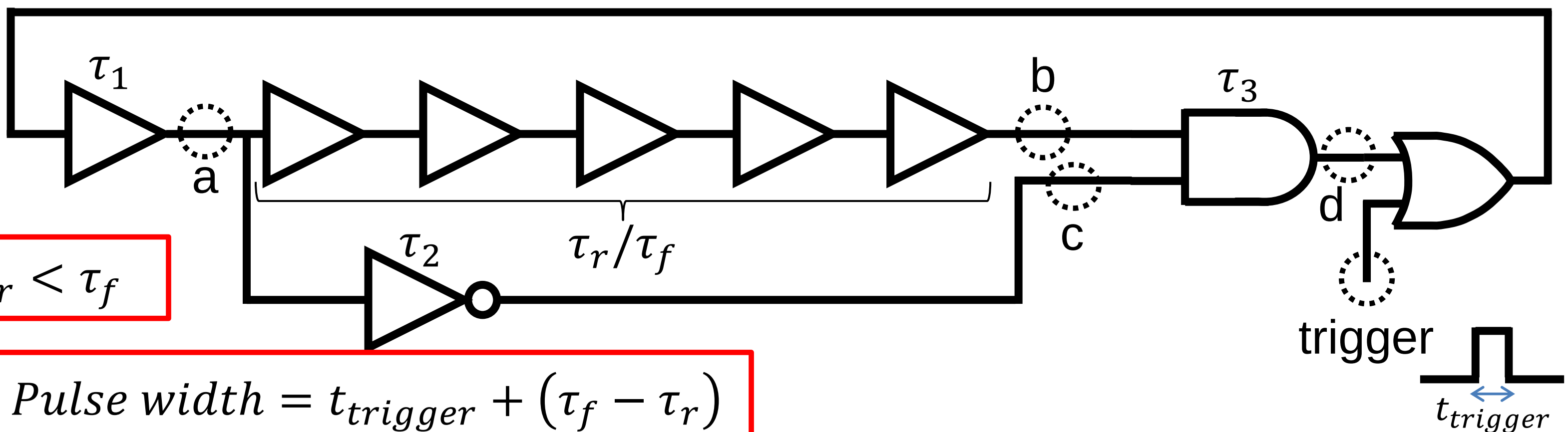
AND out put "d" is rises from low to high level after τ_3





Timing chart

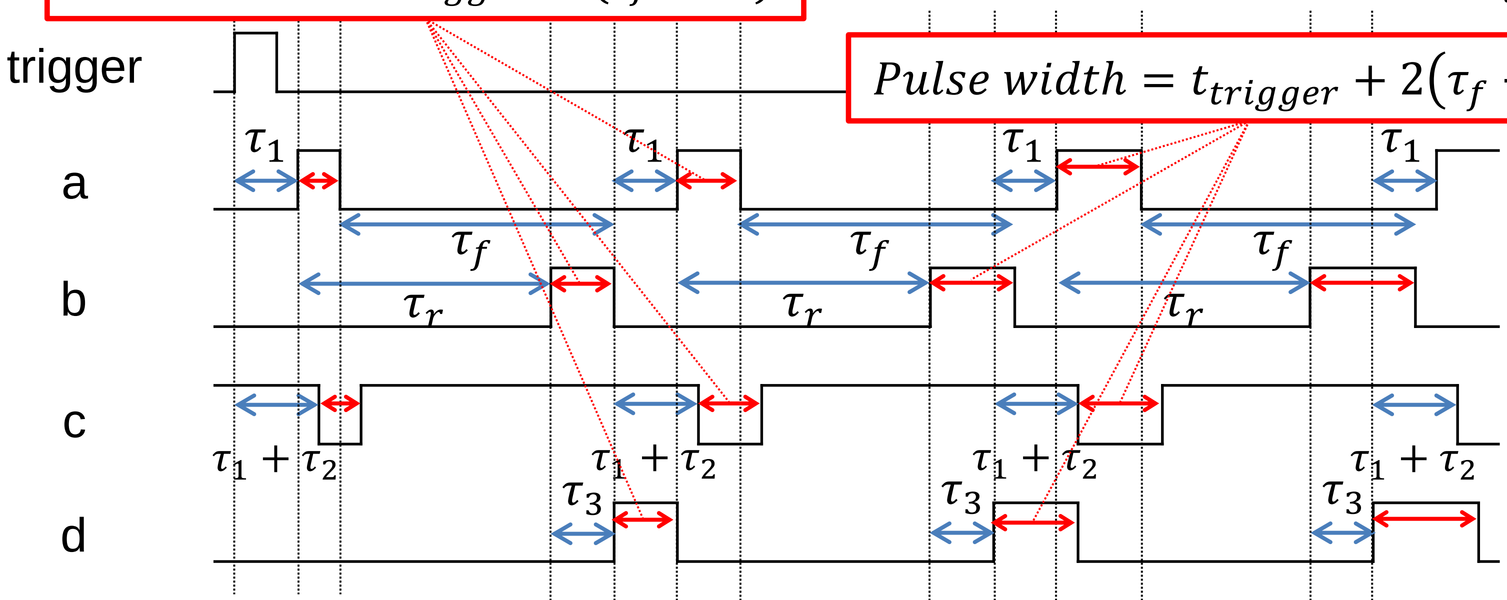
Over time, Pulse width of each node is increasing by $(\tau_f - \tau_r)$



$\tau_r < \tau_f$

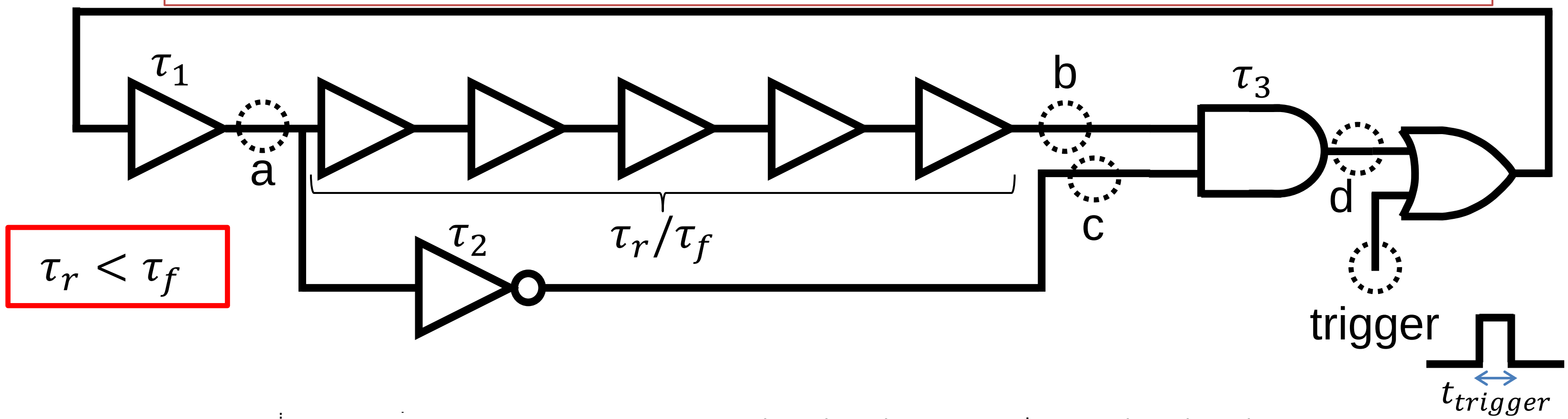
$Pulse\ width = t_{trigger} + (\tau_f - \tau_r)$

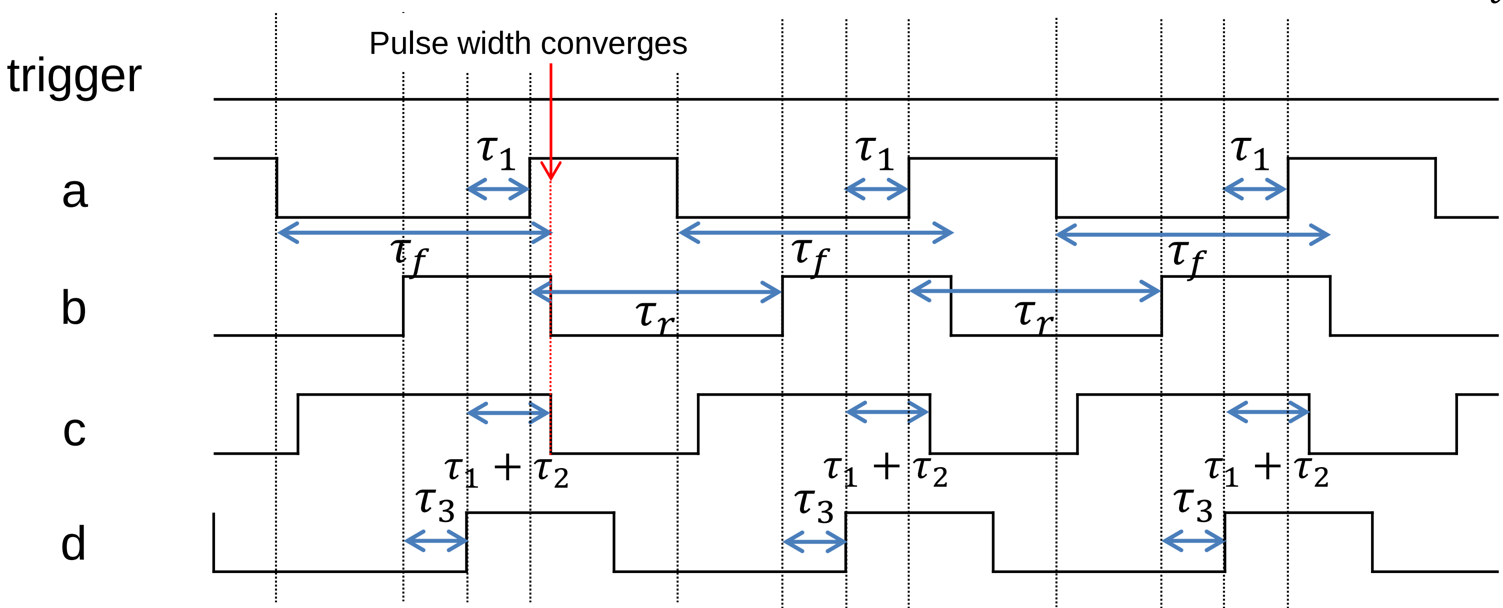
$Pulse\ width = t_{trigger} + 2(\tau_f - \tau_r)$



Timing chart

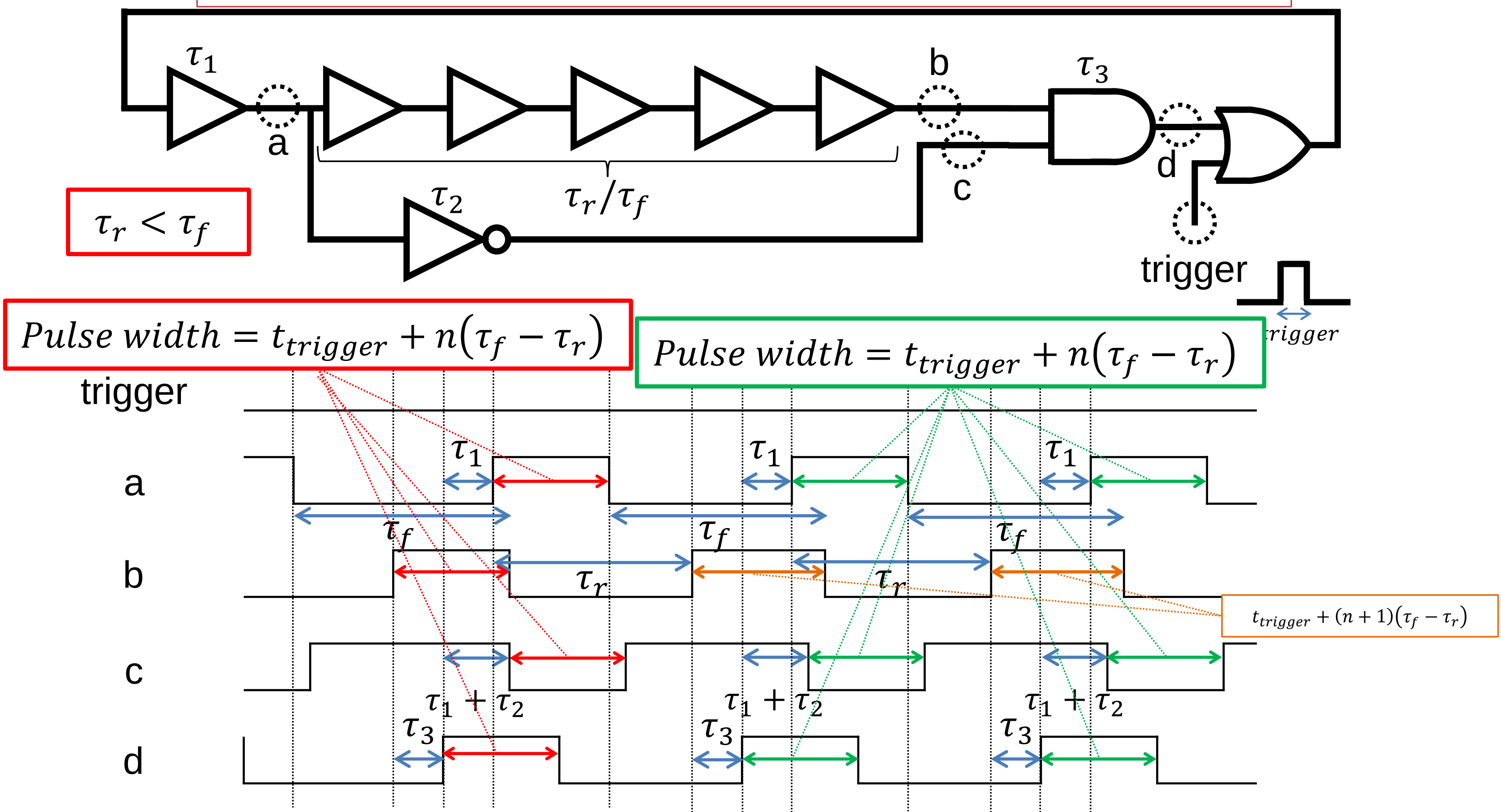
The timing of the falling edge of node B and C becomes the same, a pulse width converges





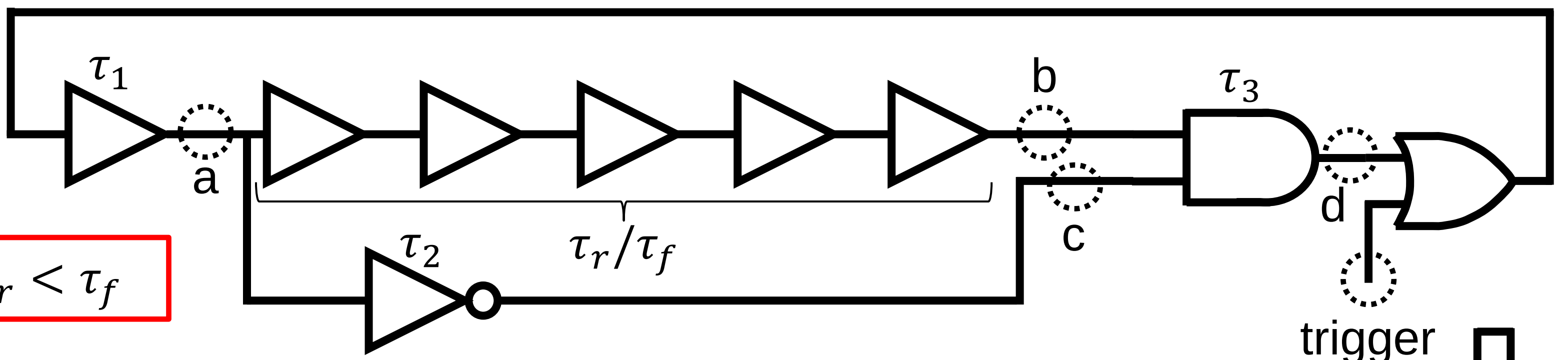
Timing chart

The timing of the falling edge of node B and C becomes the same, a pulse width converges



Timing chart

After convergence, period T of node "d" is $\tau_1 + \tau_r + \tau_3$



$\tau_r < \tau_f$

$$f_{osc} = \frac{1}{\tau_r + (\tau_1 + \tau_3)}$$

Obtain the accurate value of τ_r with measuring the oscillation frequency !!