# Post-Silicon Jitter Measurements

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## Abstract

This paper reviews the theory and introduces the architecture for a clock source with low phase noise and for measuring timing jitter. This approach utilizes a sample mean and sum of two random variables, and can be implemented in CMOS or SiGe BiCMOS circuits.

## 1. Introduction

Two noisy signal edges can interact with each other in an analog phase-locked loop (PLL) circuit, a voltage-controlled oscillator (VCO) circuit, and in source-synchronous systems. Several significant noise sources which contaminate the signal edges are specifically addressed in this paper;
(a) The phase frequency detector (PFD) of a PLL is the dominant noise source, where a reference clock edge and a noisy VCO output are compared to control the phase or frequency of oscillation. Reducing the noise in the PFD output is required for high-performance applications.
(b) The 1/*f* phase-noise corner frequencies of minimum size transistors in newer CMOS processes tend to increase and are present around several MHz. Since minimizing the phase noise due to VCO instabilities requires a wide loop bandwidth, reducing the VCO noise is critical for mm-wave transceivers.
(c) Since source-synchronous systems have simplicity of clock distribution, the ability to rapidly transition between power modes and require no synch training is important. However, when scaling such systems, the inherent clock/data fan-out mismatch can cause path length mismatches and resultant jitter [1]. It is very important to realize systems that can preserve the correlation between the jittery data and the received jittery clock.

It is extremely difficult to measure on-chip jitter using external instruments because this measurement requires both a high-frequency pin and an on-chip high-performance driver to deliver on-chip jittery signals to the external instrument without distortion. Alternatively, current on-chip *timing-jitter* measurement circuits require both a jitter-free reference clock and a fail counter in order to measure a jitter probability density function (PDF) [2]. Thus, it is extremely difficult to measure timing jitter in fs-resolution using current on-chip instrument. A new architecture is introduced here which requires no reference clock and can directly measure timing jitter even in the presence of a noisy edge of the clock under test.

This paper reviews the theory and introduces the architecture for a clock source with low phase noise and circuits for measuring timing jitter.

In Section 2 of this paper, the PLL, phase noise, and statistical mean and variance are revisited. In Section 3, use of correlated edges to reduce random skew is discussed. In Section 4, use of uncorrelated edges to reduce phase noise is discussed. In Section 5, timing jitter measurement which uses the clock under test as a referenced clock to directly measure timing jitter is presented.

## 2. PLL, Phase Noise, Mean and Variance

In this section, the two basic parameters of a random variable (mean and variance) are defined in conjunction with their use to characterize the phase noise.

### 2.1 Terminology and Definition

**Phase-Locked Loop (PLL).** The elements of an analog PLL circuit are a phase frequency detector (PFD), a charge pump, a lowpass filter, and a single-phase VCO (**Fig. 1**). The PFD is the dominant noise source in a PLL. The VCO strongly influences the operating frequency range, center frequency drift, and the center frequency supply voltage sensitivity [3].

Moreover, phase noise in the VCO output due to internal noise sources, is *inversely proportional* to the PLL loop bandwidth. Therefore, in order to minimize the phase noise due to VCO instabilities, the loop width must be made *as wide as possible* [4]. This makes the transient phase error contribution small. On the other hand, the phase noise due to the additive noise of the PLL received signal is *proportional* to the PLL loop bandwidth. Hence, the loop bandwidth should be made *as narrow as possible* [4]. This will cause a large transient phase error.

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**Phase noise** [5]. Phase noise $L(f_{offset})$ is defined as the ratio of power in one phase modulation sideband per Hertz of bandwidth to the total power in the carrier (Fig. 2).

$$L(f_{offset}) = \frac{noise\ power\ density}{total\ carrier\ power} \quad (1)$$

The mean-square value of phase noise is related to the area under the phase noise spectrum curve [6]. The rms value of phase noise is given by the positive square root of the mean-square value.

As shown in Fig. 2, at phase-noise corner frequency $f_c$, the $1/f$ phase-noise spectrum, which has a correlation coefficient of $\rho \neq 0$, intersects the thermal white noise spectrum, which has a correlation coefficient of $\rho = 0$.

The $1/f$ phase-noise corner frequency $f_c$ of minimum size transistors in newer CMOS processes tends to increase. Thus VCO implementations at mm-waves use core devices of small dimensions, and the phase noise corner frequencies occur at several MHz [7]. In VCOs, AM-to-PM conversion mechanisms up-convert the flicker noise, which is associated with the bias current, into high-frequency phase noise [8].

**Correlation coefficient.** The correlation coefficient $\rho$ is one of the similarity measures between two signals [9]. It is a function of similarity and alignment. The value of $\rho$ always falls between -1.0 and +1.0. If the two signals are aligned, their similarity is maximum, and $\rho$ = 1.0 indicating perfect positive correlation. Two signals aligned in opposite directions have maximum dissimilarity, and $\rho$ = -1.0 indicating perfect negative correlation. If the two signals are *orthogonal*, their similarity is zero, and $\rho$ = 0.0 indicating no correlation.

It is important to note that the total *power* of two orthogonal signals is equal to the *sum* of the power in each signal.

The rms value of the random clock skew is given as the statistical *sum* of the two random timing jitters [10].

$$\sigma^2_{Skew} = \Delta\phi^2_{j,RMS} + \Delta\phi^2_{k,RMS} - 2\rho\Delta\phi_{j,RMS}\Delta\phi_{k,RMS} \quad (2)$$

where $\phi_{j,RMS}$ and $\phi_{k,RMS}$ are the rms values and $\rho$ is the cross-correlation coefficient between the two timing jitters of $CLK_j$ and $CLK_k$.

**Statistical Mean and Variance** [11]. The *mean* of a random variable (RV) $x$ depends only on its distribution of $\mathbf{x}$. Therefore, if its PDF $f(x)$ is known, its mean $E[\mathbf{x}]$ can be expressed as integral function:

$$E[\mathbf{x}] = \int_{-\infty}^{+\infty} x f(x) dx$$

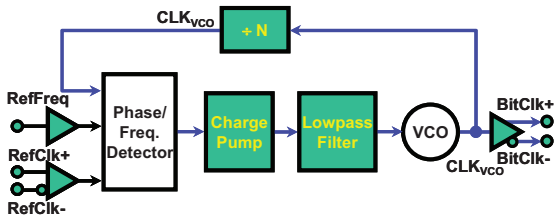



**Fig. 1. Analog Phase-Locked Loop.**

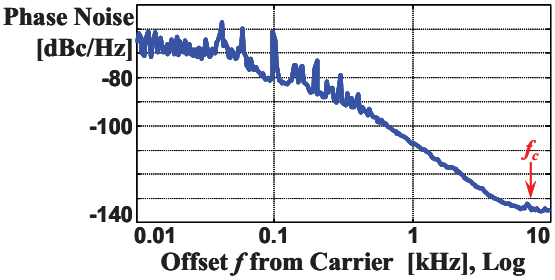



**Fig. 2. Typical phase noise and the phase-noise corner frequency $f_c$.**

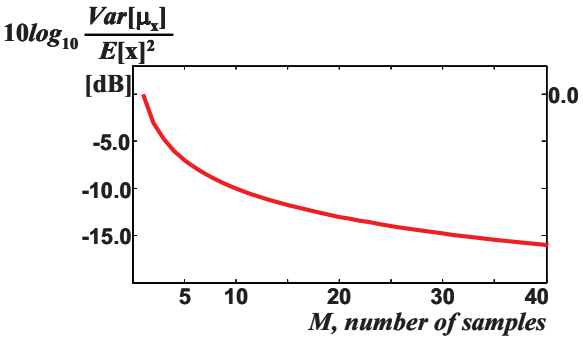



**Fig. 3. Normalized random error as a function of number of samples.**

The *variance* of a random variable $\mathbf{x}$ also depends only on its distribution. $Var[\mathbf{x}]$ is also expressed as the integral function:

$$Var[\mathbf{x}] = \int_{-\infty}^{+\infty} \left( x - E[\mathbf{x}] \right)^2 f(x) dx$$

**Sample Mean and Variance.** The *mean* value and variance of a random signal can be calculated using *summing* operations directly on the random signal.

Assuming $M$ *independent* observation, the sample mean value $\hat{\mu}_x$ and sample variance $\hat{\sigma}^2_x$ of the sampled signal $x$ are estimated as:

$$\hat{\mu}_x = \frac{1}{M}\sum_{i=1}^{M} x_i$$

$$\hat{\sigma}^2_x = \frac{1}{M}\sum_{i=1}^{M} (x_i - \hat{\mu})^2$$

**Ergodicity.** It can be readily shown [11] that:

$$\hat{\mu}_x \to E[\mathbf{x}] \quad (M \to \infty)$$

Thus, the random variable $\hat{\boldsymbol{\mu}}_{\mathbf{x}} = \hat{\mu}_x$ tends to $E[\mathbf{x}]$ in a mean square sense. Its variance $Var[\hat{\boldsymbol{\mu}}_{\mathbf{x}}]$ tends to zero as $M \to \infty$:

$$Var[\hat{\boldsymbol{\mu}}_{\mathbf{x}}] = E\left[(\hat{\mu}_x - E[\mathbf{x}])^2\right] \to 0 \qquad (3)$$

with

$$\frac{Var[\hat{\boldsymbol{\mu}}_{\mathbf{x}}]}{E[\mathbf{x}]^2} \to \frac{C}{2BT} \qquad (BT >> 1) \qquad (4)$$

where $BT$ is the bandwidth-time product. Notice that $2BT$ also corresponds to the number of independent estimates $M$ [12]. Thus, as illustrated in Fig. 3, the variance $Var[\hat{\boldsymbol{\mu}}_{\mathbf{x}}]$ decreases inversely with the number of samples $M$. This leads to the following result:

$$10\log_{10}\frac{Var[\hat{\boldsymbol{\mu}}_{\mathbf{x}}]}{E[\mathbf{x}]^2} \propto -10\log_{10} M \qquad (5)$$

The frequency of an oscillator can be measured using an external instrument or an on-chip instrument. Since there is always some noise, signal averaging is required to measure the frequency of a randomly fluctuating oscillation.

The average frequency $\hat{\mu}_x$ of the oscillator, which is measured by taking a sequence of $M$ samples over a long time interval $T$, converges to the average frequencies $E[\mathbf{x}]$ of $M$ identically distributed independent oscillators. This corresponds to the statistical mean.

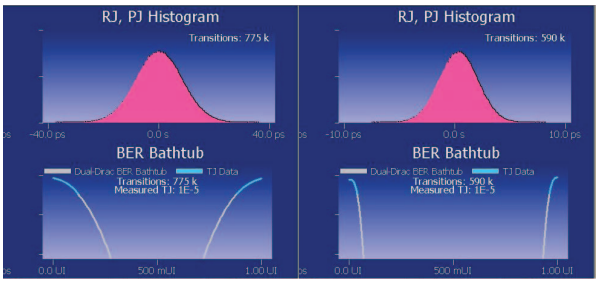
## 3. Correlated Jittery Edges to Reduce Random Skew

In order to reduce random skew, a source synchronous system has to preserve the correlation between the jitter in the incoming data and the jitter in the received clock.

### 3.1 Experimental Validation of Equation (2)

In this sub-section, the relationship between two timing jitters and the resultant random clock skew in (2) is validated with experimental data. The experiment uses an oscilloscope (Agilent Technologies, DSO81304B) and its built-in clock recovery circuit.

First, an uncorrelated source clock of $\rho \approx 0.0$ was generated as a sampling clock by the clock recovery circuit that is built into the oscilloscope. Fig. 4(a) shows the PDF and the estimated BER curves. The $\sigma$ value of random jitter (RJ) was 8.3 $ps_{RMS}$. Next, a correlated DUT clock of $\rho \approx 1.0$ was applied to the oscilloscope as a sampling clock. Fig. 4(b) shows the PDF and the estimated BER curves. The $\sigma$ value of RJ was 1.6 $ps_{RMS}$.




(a) (b)

**Fig. 4. Correlation between jitter on the source clock and jitter on the data. (a) Uncorrelated source clock: $\rho$ = 0.0, σ of RJ = 8.26 ps. (b) Correlated source clock: $\rho$ = 1.0, σ of RJ = 1.57 ps.**

In summary, the relationship described by (2) is experimentally validated for randomly fluctuating timing. That is, if the sampling clock jitter and jitter in the clock under test are uncorrelated with each other, a large $\sigma$ value of timing jitter or random skew is obtained. Alternatively, if the sampling clock jitter and jitter in the clock under test are correlated with each other, a small $\sigma$ value is obtained.

### 3.2 Source Synchronous Signaling Scheme

Since source-synchronous systems supply a clock along with the transmitted data, the requirement for a PLL to generate the synchronous clock is removed from high-speed I/O systems. In order to realize good jitter tolerance, it is critically important for a source-synchronous system to preserve the correlation between the jitter on the incoming data and the jitter on the received clock. But, in multi-bit parallel source synchronous busses, the high fan-out from clock to data causes significant clock buffer delays. This mismatch causes uncorrelated jitter in the clock on the receiving device. From (2), it can be seen that uncorrelated timing jitters maximize the random skew:

$$\sigma^2_{Skew} \to \Delta\phi^2_{j,RMS} + \Delta\phi^2_{k,RMS} \qquad (\rho \to 0)$$

This severely impacts the jitter tracking performance of the device.

Reference [1] proposes a clock-embedded source-synchronous signaling scheme and validates this scheme with experimental data at 5 Gb/s using a 40 nm LP CMOS. It superimposes the clock in the common-mode signal across two differential pairs, thus reducing clock pin overhead. Furthermore the clock edges for transmit and/or receive can be aligned with reasonable trace-length matching. From (2), it can be seen that correlated timing jitters minimize the random skew between clocks:

$$\sigma^2_{Skew} \to \left(\Delta\phi_{j,RMS} - \Delta\phi_{k,RMS}\right)^2 \qquad (\rho \to 1)$$

Therefore, the system can be made more tolerant to high-frequency jitter in the source clock.

The receiver performance can be easily validated by measuring BER bathtubs in the configuration of the parallel loopback [see Fig. 12 of 1].

## 4. Uncorrelated Jittery Edges to Reduce Phase Noise

It will be shown next how VCOs and PLLs can reduce phase noise by utilizing a sample mean. Phase noise of a PLL can be reduced by averaging out noise from phase error signals [13]. Similarly, phase noise of a VCO can be reduced by averaging the phase noise of two independent VCOs [14]. Furthermore, jitter in the input clock can be reduced by phase-blending the two edges, which are uncorrelated with each other due to the $NT$ delay [15].

### 4.1 Multi-PFD PLL

Reference [13] has recently proposed a method for improving PLL phase noise performance. In order to reduce the dominant noise due to the PFD, a single PFD can be replaced by the combination of $M$ PFDs, together with a summing amplifier.

For example, both the reference clock and a VCO output are split into four pairs, and the four pairs are each fed into four separate PFDs. Each PFD then outputs a pulse, the width of which is proportional to the phase difference between the reference clock and VCO output. The output pulse from each PFD is input to a lowpass filter to smooth out glitches and remove high-frequency noise. Finally the four outputs from the filters are directly connected to a summing amplifier to yield a sample mean of the four phase differences. It is clear that this summing amplifier reduces the random noise power by $M$ times in accordance with (5).

A multi-PFD PLL IC was fabricated in a 0.18 μm SiGe BiCMOS process. The square symbol in Fig. 5 shows the measured phase noise value as a function of the number of the PFDs $M$. It is clear that the phase noise power decreases as $M$ increases.

Phase noise measurement is required in order to validate the performance of the multi-PFD PLL.

### 4.2 VCO Coupling Method

Reference [14] proposed a method for improving VCO phase noise performance. The phase noise power, which is defined in the numerator of (1), can be reduced by connecting the outputs of multiple VCOs together. This connected VCO network produces a sample mean of phase noise power. The phase noise reduction of the connected VCO network is $M$ times greater than that of a conventional stand-alone VCO in accordance with (5).

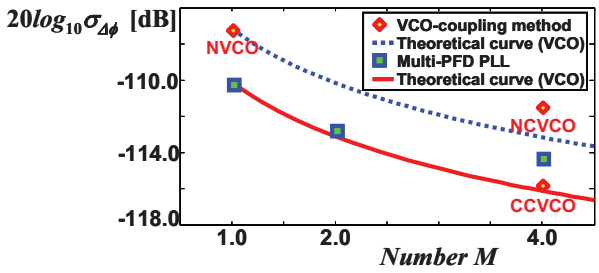



**Fig. 5. Measured in-band phase noise of the multi-PFD PLL ($f_{clk}$ = 15 GHz) & the connected multi-VCO ($f_{clk}$ = 13 GHz).**

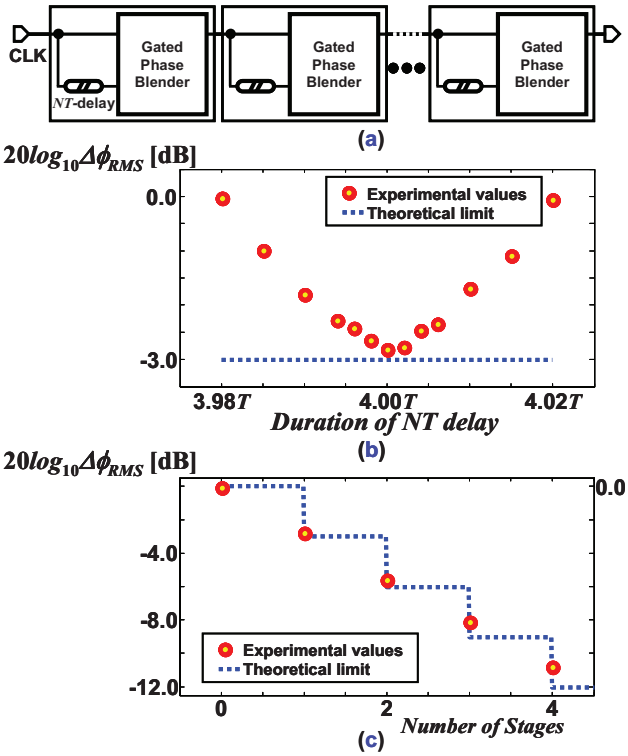



**Fig. 6. A clock jitter reducer using correlation coefficient $\rho$ = 0. A 65 nm CMOS circuit, $f_{CLK}$ = 500 MHz. (a) The reducer consists of multiple cascaded stages of the gated phase blending circuit. (b) Measured rms value of timing jitter as a function of the duration of $NT$-delay, single stage. (c) Measured rms value of timing jitter as a function of number of cascaded stages.**

Prototype VCO designs were fabricated in a 65 nm LP CMOS. The diamond symbol in Fig. 5 shows the measured phase noise power as a function of the number ($M$) of connected VCOs. It is clear that the phase noise value decreases as $M$ increases.

Since the *complementary-cross-coupled-pair coupled VCO* (CCVCO) uses complementary nMOS & pMOS cross-coupled pairs at the tanks, it has superior flicker noise performance. Thus, as shown in Fig. 5, the

CCVCO topology outperforms both the *nMOS crosscoupled VCO* (NVCO) and the *nMOS cross-coupled pair coupled VCO* (NCVCO) topologies.

Phase noise measurement is required in order to validate the performance of this connected VCO network.

### 4.3 Phase-Blending Circuits

A new circuit for reducing jitter in an input clock has been recently proposed [15]. As illustrated in Fig. 6(a), an input clock is split into two paths; one fed directly into a phase-blender circuit, while the other goes through a $NT$ delay before being fed into the same phase-blender circuit. This intentional misalignment generates two uncorrelated edges, which are then phase-blended to interpolate between the two edges: $M = 2$. Using (5), a single stage phase-blender can reduce the random timing jitter by 3.01 dB.

A jitter reduction circuit was fabricated in a 180 nm CMOS process. The circle symbol in Fig. 6(b) shows the measured rms value of timing jitter as a function of the period around $4T_0$, where $T_0$ is the period of the input clock. It can be seen that the timing jitter in the output clock has its minimum rms value at around $4T_0$, which corresponds to $\rho \approx 0.0$. The rms value of the timing jitter in the output of a four-stage, cascaded phase-blender circuit is shown in Fig. 6(c). It is clear that the phase-blender together with a self-delay successfully reduces timing jitter by 3.01 dB / stage.

## 5. Sum of Two RVs to Extract Timing Jitter

A new architecture presented in this section provides all-digital timing jitter measurement using a clock under test as a referenced clock to directly measure the timing jitter [2]. The operational principle of this circuit is based on the sum of two random variables.

### 5.1 Self-Referenced Clock to Extract Period Jitter

In previous works [16] showed how a reference clock is not needed if the clock signal under test is split into two paths. One path that goes directly into the latch, and the other path goes through the delay line with delay time = one clock period $T$. The extracted time difference between the clock under test and the delayed clock, which equals to one period fluctuation, is then integrated to obtain timing jitter. Note that, by substituting $\rho = 1.0$ into (2),

$$\sigma_{Skew} = \Delta\phi_{j+1,RMS} - \Delta\phi_{j,RMS}$$

is obtained, which is exactly the period jitter.

Thus, a conventional circuit requires an integrator for accumulating a period jitter sequence to extract timing jitter from it. Until now, no circuit has been proposed which can extract timing jitter directly from the input clock.

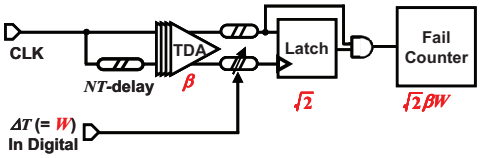



**Fig. 7. Proposed timing jitter measurement circuit with TDA.**

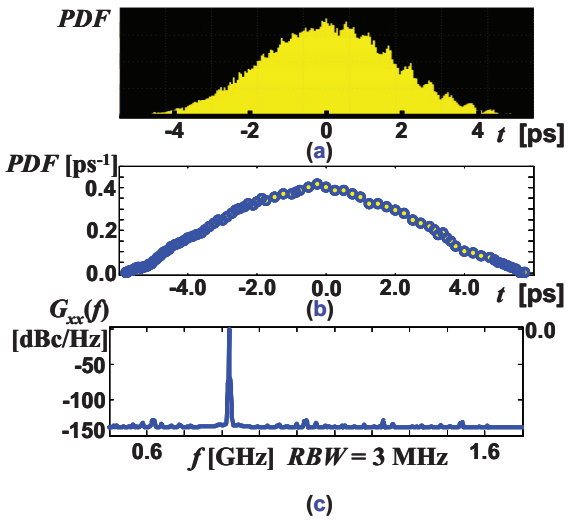



**Fig. 8. Measured timing jitter PDFs and RF spectrum: $f_{CLK}$ = 820 MHz. (a) Measured PDF by an oscilloscope (Tektronix DSA71254): $\Delta\phi_{RMS}$ = 1.61 ps. (b) Measured PDF by the timing jitter measurement circuit with 4T delay: $\Delta\phi_{RMS}$ = 1.73 ps. (c) Measured RF spectrum by a spectrum analyzer (Advantest R3681): $\sigma_{\Delta\phi}$= 1.55 ps.**

### 5.2 Self-Referenced Clock to Extract Timing Jitter

Fig. 7 shows the schematics of the proposed circuit for measuring timing jitter [2]. It consists of variable delay elements, a fixed delay element, a cascaded time difference amplifier (TDA), a latch, and counters. The proposed timing jitter measurement circuit adopts a self-referenced clock technique to eliminate the requirement for a reference clock.

However, unlike the previous approach, our proposed method sets delay of the delay line to multiples of the clock period $NT$, with $N \geq 3$. Two edges which are apart from each other by $NT$, are uncorrelated with each other: $\rho \approx 0.0$. From (2), the time difference between the clock under test and the delayed clock is detected as:

$$\sigma^2_{Skew} = \Delta\phi^2_{j+N,RMS} + \Delta\phi^2_{j,RMS} = 2\Delta\phi^2_{j,RMS}.$$

Hence, the proposed circuit can directly measure the timing jitter with a circuit gain = $\sqrt{2}$ .

### 5.3 Time Difference Amplifier to Reduce Error

A four-stage cascaded TDA with a gain $\beta \approx$ 100 amplifies the time difference between the rising edges of the non-delayed and $NT$ delayed clocks.

If the time resolution of the variable delay line is set to $W$ , PDFs can be measured with effective time resolution $W_{effective} = \sqrt{2}W\beta$ . In words, measurement of the effective time resolution of $W_{effective}$ can be performed by with a delay time resolution $W$ , which is $\sqrt{2}\beta$ times coarser than $W_{effective}$ . This leads to a variance error associated with PDF measurements which is reduced by $\sqrt{2}\beta$ . This is critically important for high-resolution PDF measurement [17].

### 5.4 Experimental Results

Test chips were designed and fabricated in 65 nm and 40 nm standard CMOS technology.

The timing jitter CDF and PDF measured by the 65 nm CMOS circuit are shown in **Fig. 8(b)**, for a clock of 820 MHz; *N*=4 of *NT* delay and TDA. The calculated rms values were 1.92 [conventional method] or 1.73 ps [17] for the 65 nm CMOS, and 2.09 [conventional method] or 1.80 ps [17] for the 40 nm CMOS.circuit without TDA.

The PDF measured with a real-time oscilloscope (Tektronix, DSA71254) is shown in **Fig. 8(a)**: 1.61 $ps_{RMS}$. **Fig. 8(c)** shows the RF spectrum of the 820 MHz clock measured with a spectrum analyzer (Advantest, R3681). The rms value of the phase noise was 1.55 $ps_{RMS}$. These results show that the proposed circuit successfully detected the timing jitter with high accuracy.

## 6. Conclusion

This paper reviewed the theory and introduced architecture for a clock source with low phase noise and for measuring timing jitter. This approach utilizes a sample mean and sum of two random variables. These circuits can be implemented in either CMOS or SiGe BiCMOS. Their performance was experimentally verified.

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