Vernier Stochastic TDC Architecture with Self-Calibration

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Introduction

Research Objective

- Development of High-performance TDC
  - For good linearity
  - For self-calibration method
  - For fine time resolution
- Vernier delay line TDC
- Stochastic TDC

Proposed TDC Architecture

Self-calibration flow

- Improvement of nonlinearity due to delay-time mismatches among delay buffers

Test mode

- Using two-ring-oscillator

Normal mode

- # of '1's Counter
- Digital Correction
- Voltage output

Self-calibration

- Principle of Self-calibration

- TDC is non-linear

Simulation Results

Self-calibration Results

- Stochastic TDC
- 8 delay buffers
- 8 DFF's from one delay buffer
- MATLAB simulation

Conclusion

- We propose Vernier Stochastic TDC as TDC for fine time resolution and good linearity.
  - For fine time resolution:
    - Vernier technique (using two delay lines)
    - Stochastic topology (using process variations)
  - For good linearity:
    - Self-calibration (using a two-ring-oscillator, signal is "time")

Our Publication


Summary

Suitable for advanced low CMOS implementation