

# P58 Vernier Stochastic TDC Architecture with Self-Calibration

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## Introduction

### Research Objective

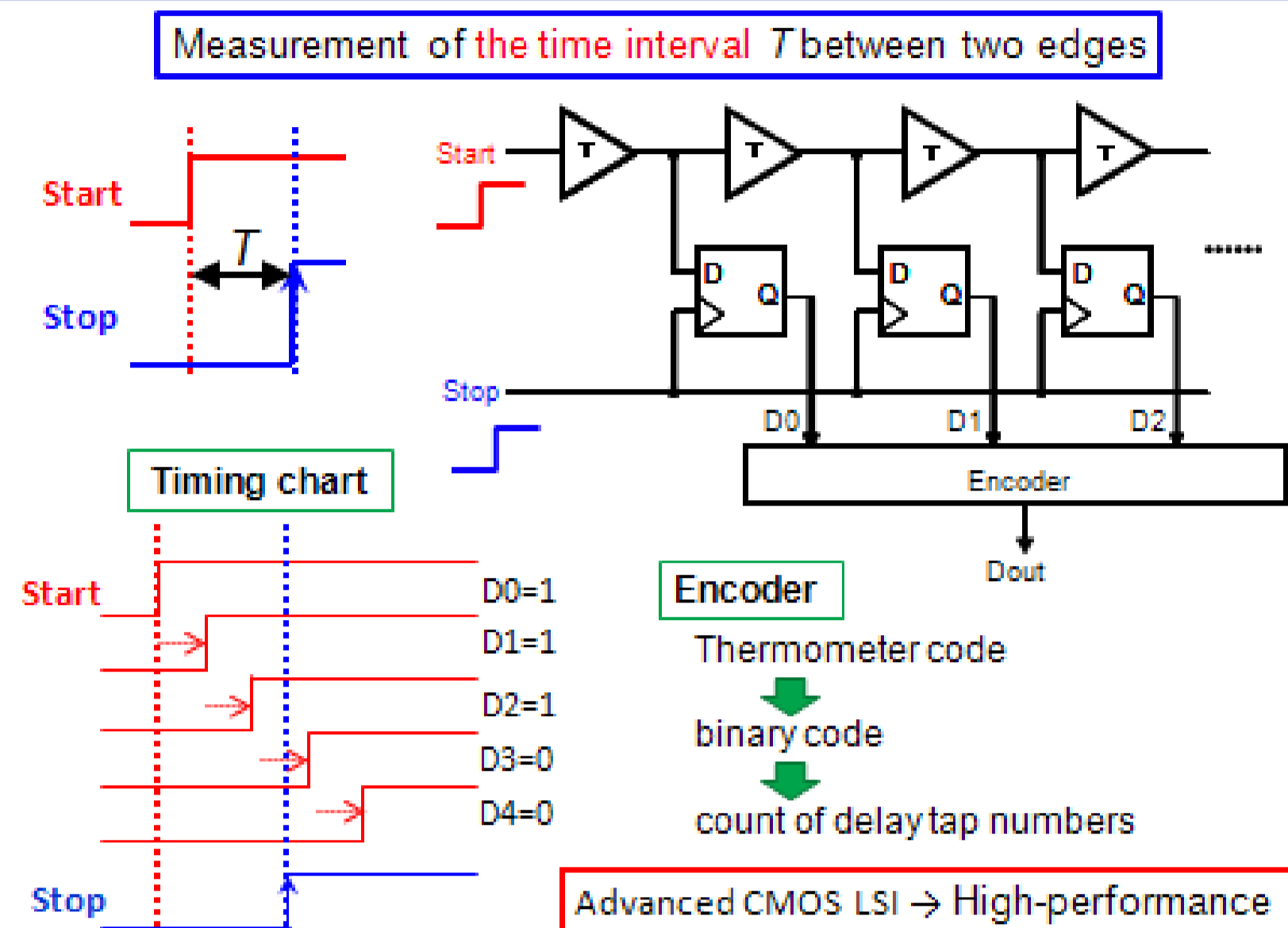
#### Development High-performance TDC

- High-performance method
    - For good linearity
      - Self-calibration method
    - For fine time resolution
      - Vernier delay line TDC
      - Stochastic TDC
- Using Histogram method

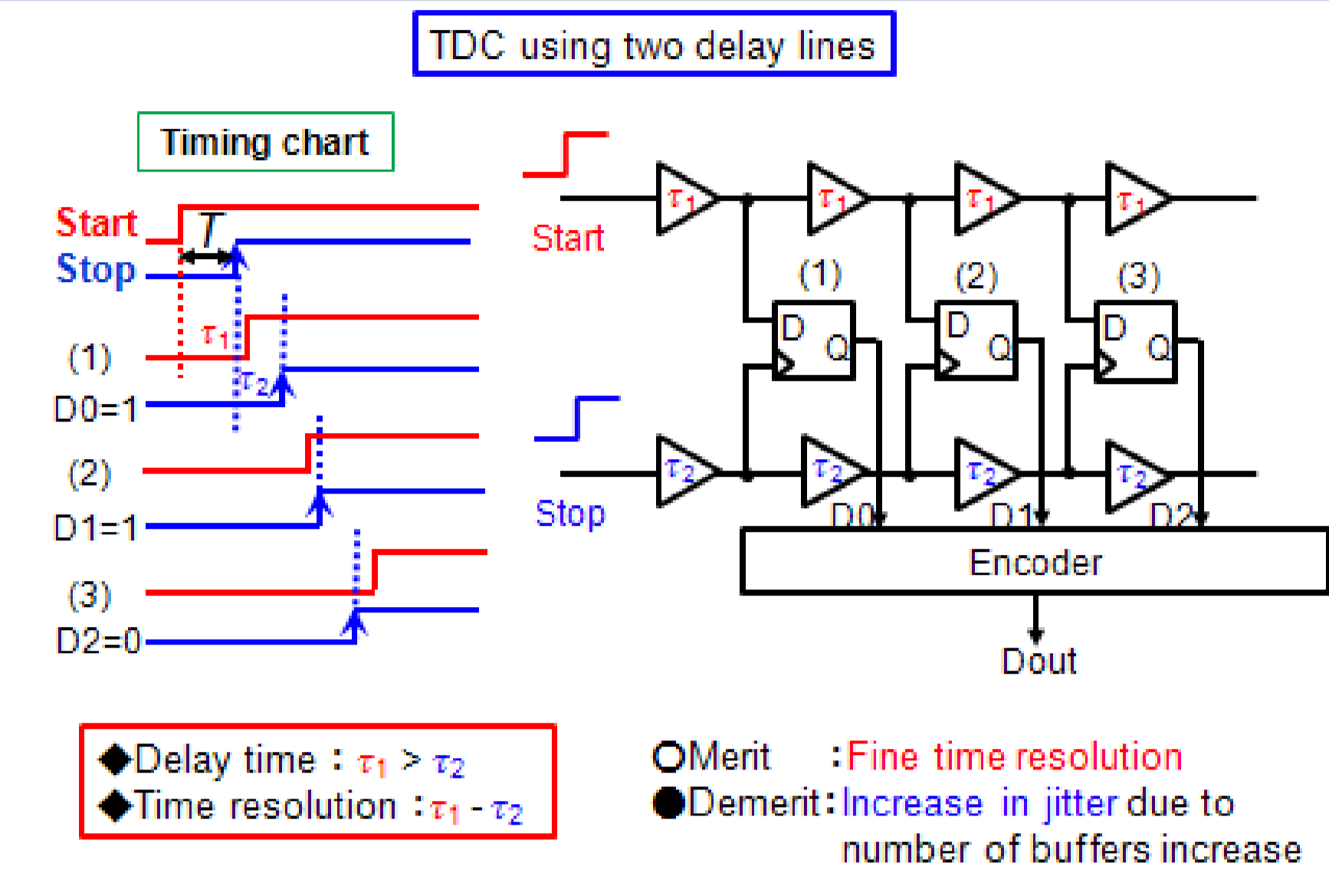
- Including TDC
- Phase comparators of all-digital PLLs
  - Sensor interface circuits
  - Modulation circuits
  - Demodulation circuits

→ Key component in nano-CMOS electronics

### Time-to-Digital Converter (TDC)

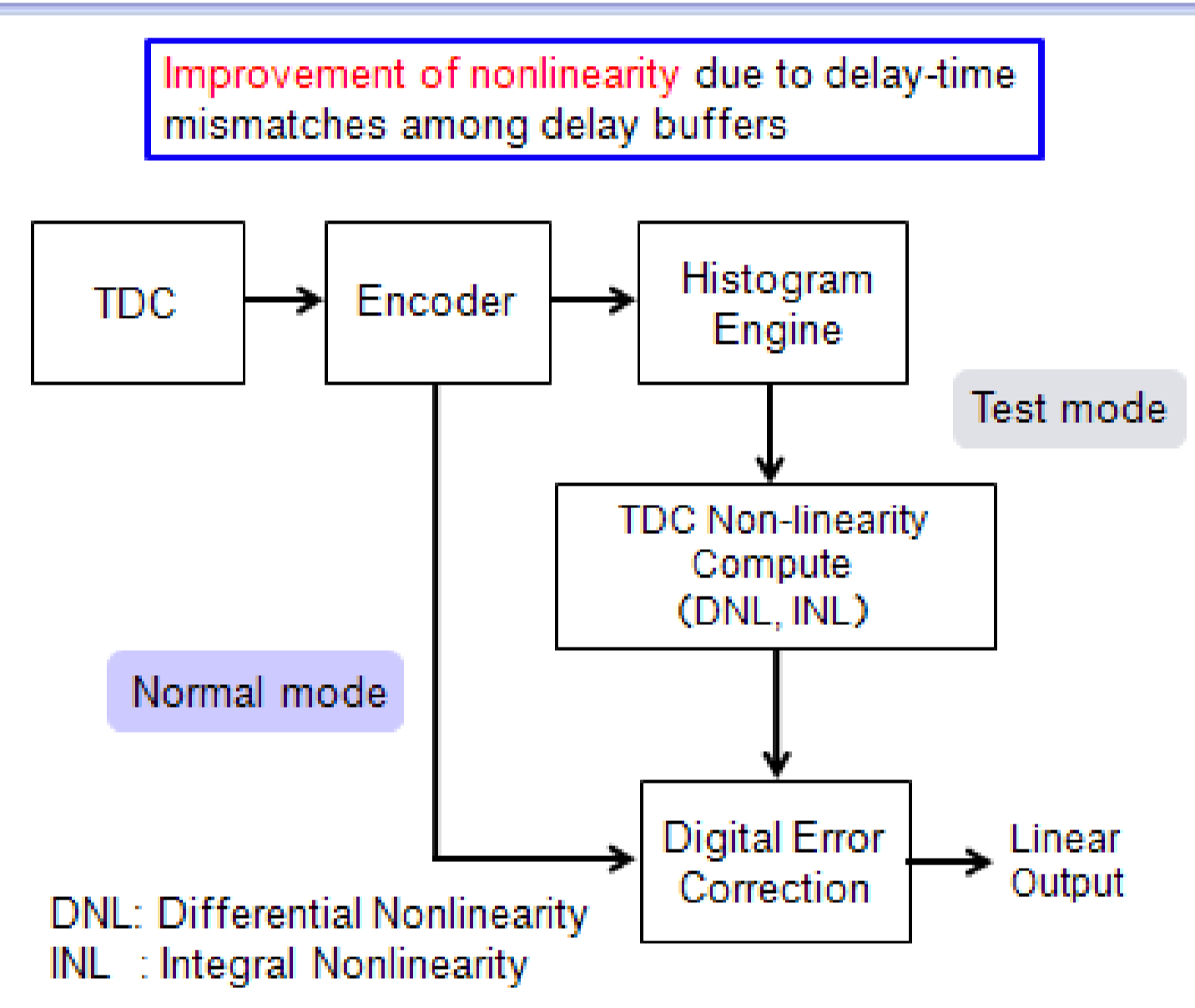


### Vernier delay line TDC

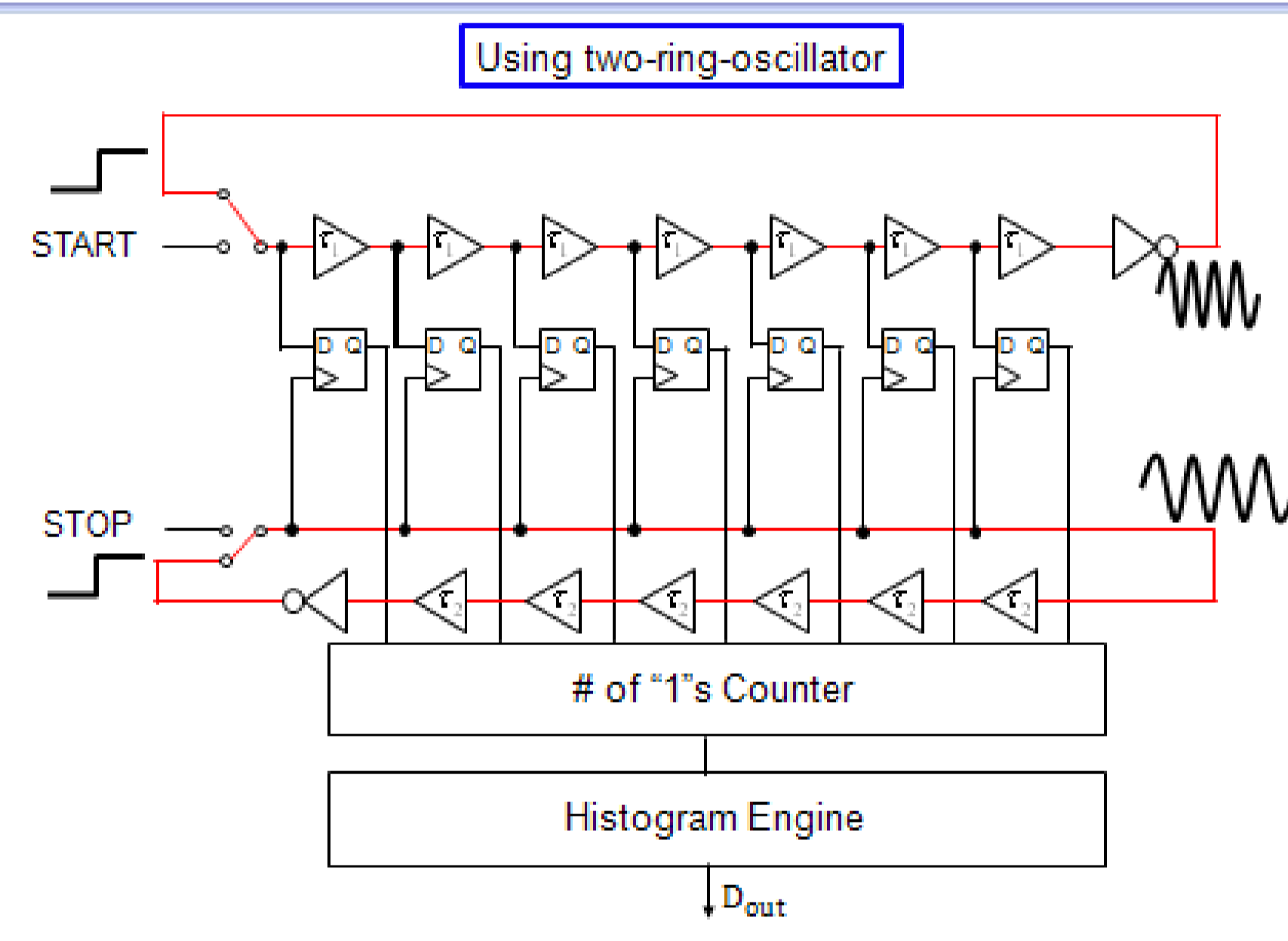


## Proposed TDC Architecture

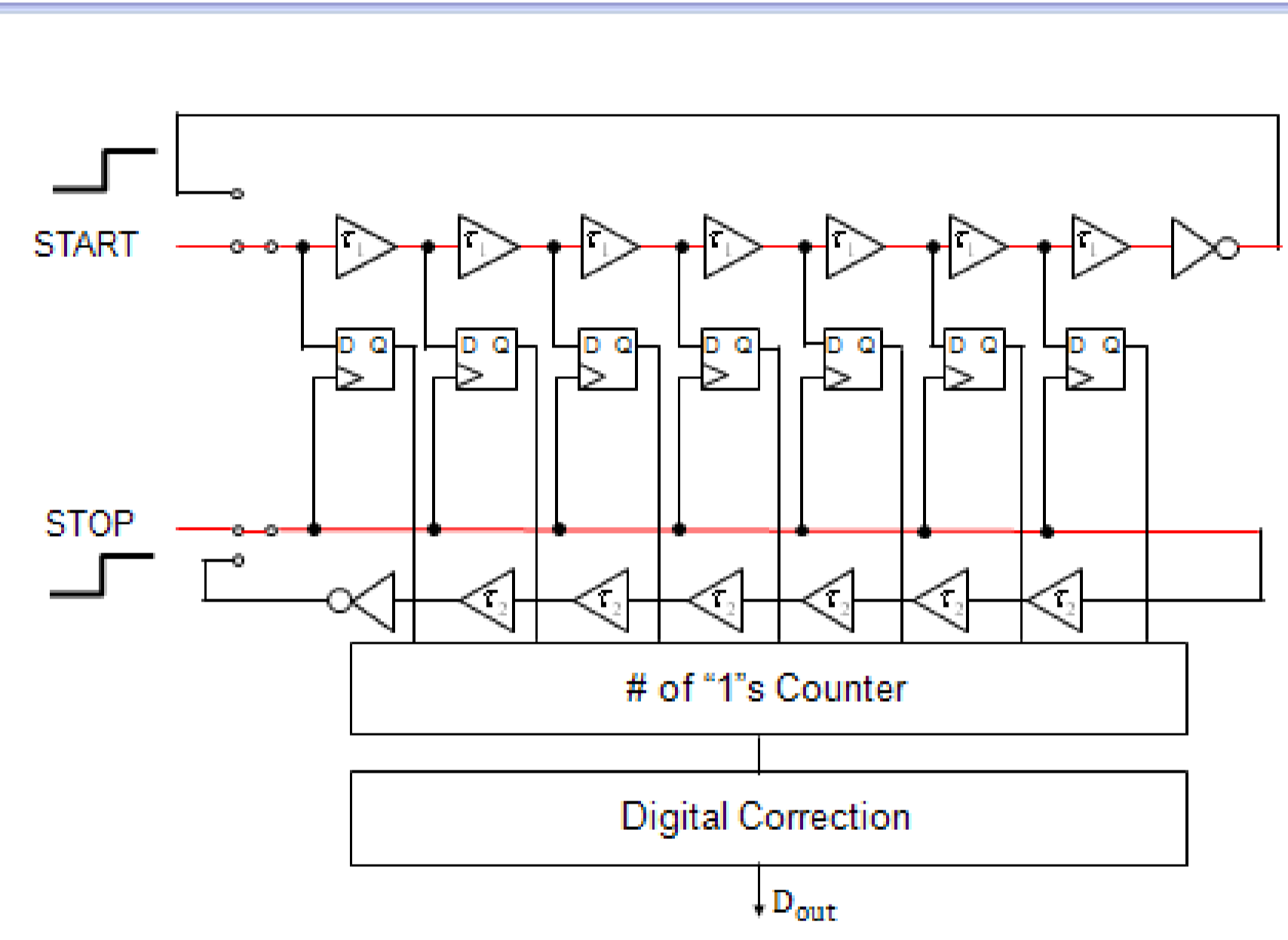
### Self-calibration flow



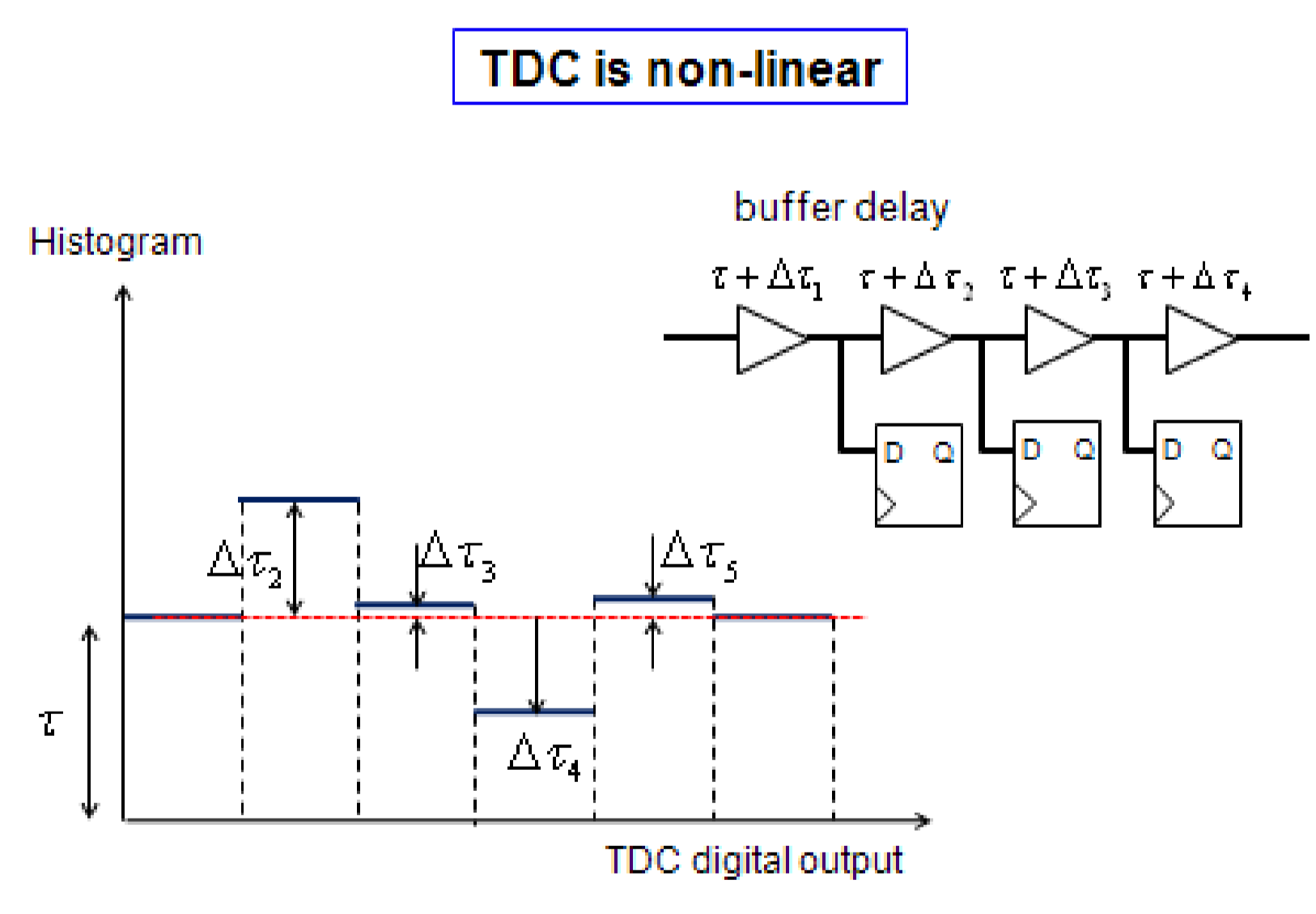
### Test mode



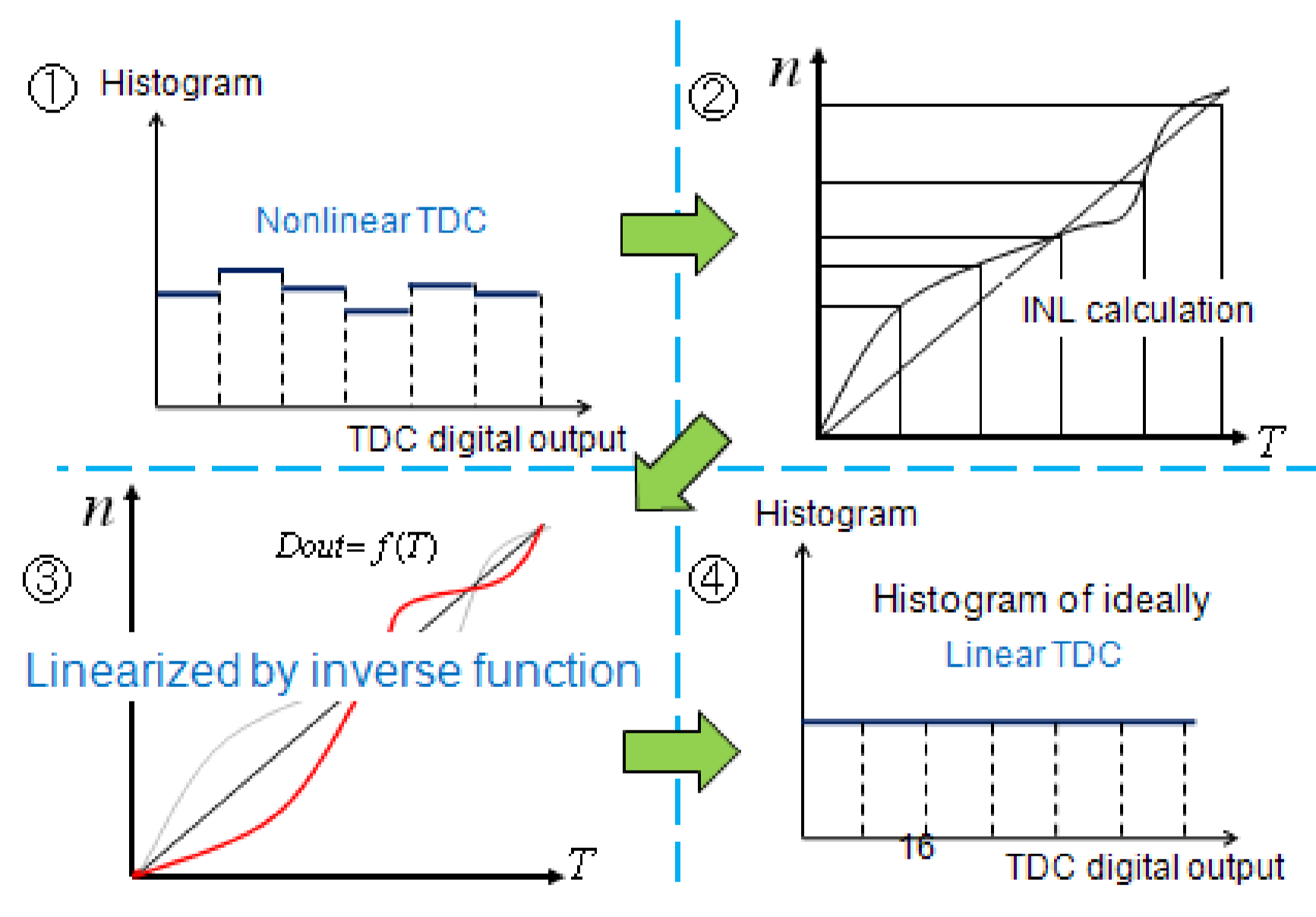
### Normal mode



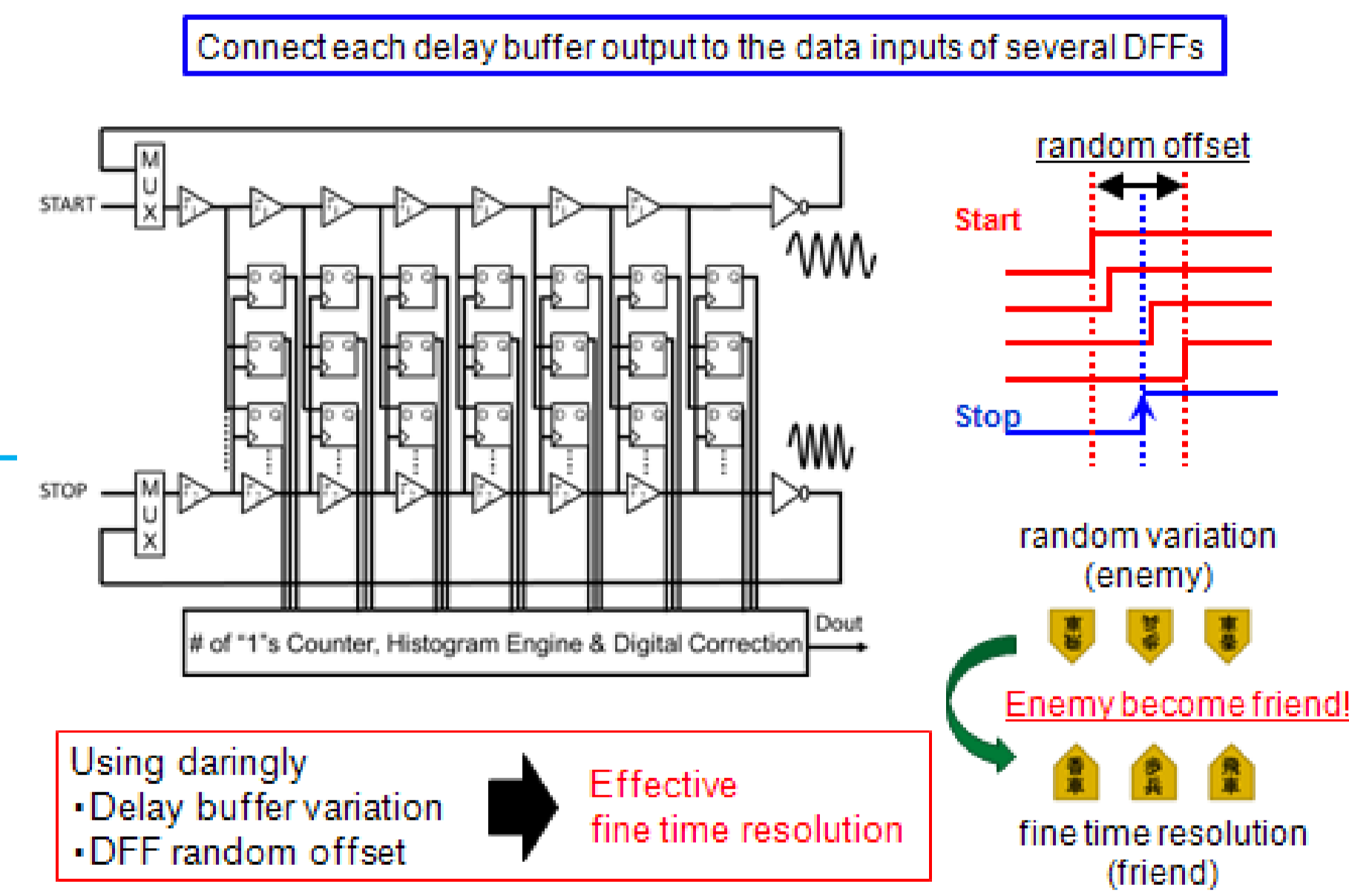
### Self-calibration



### Principle of Self-calibration

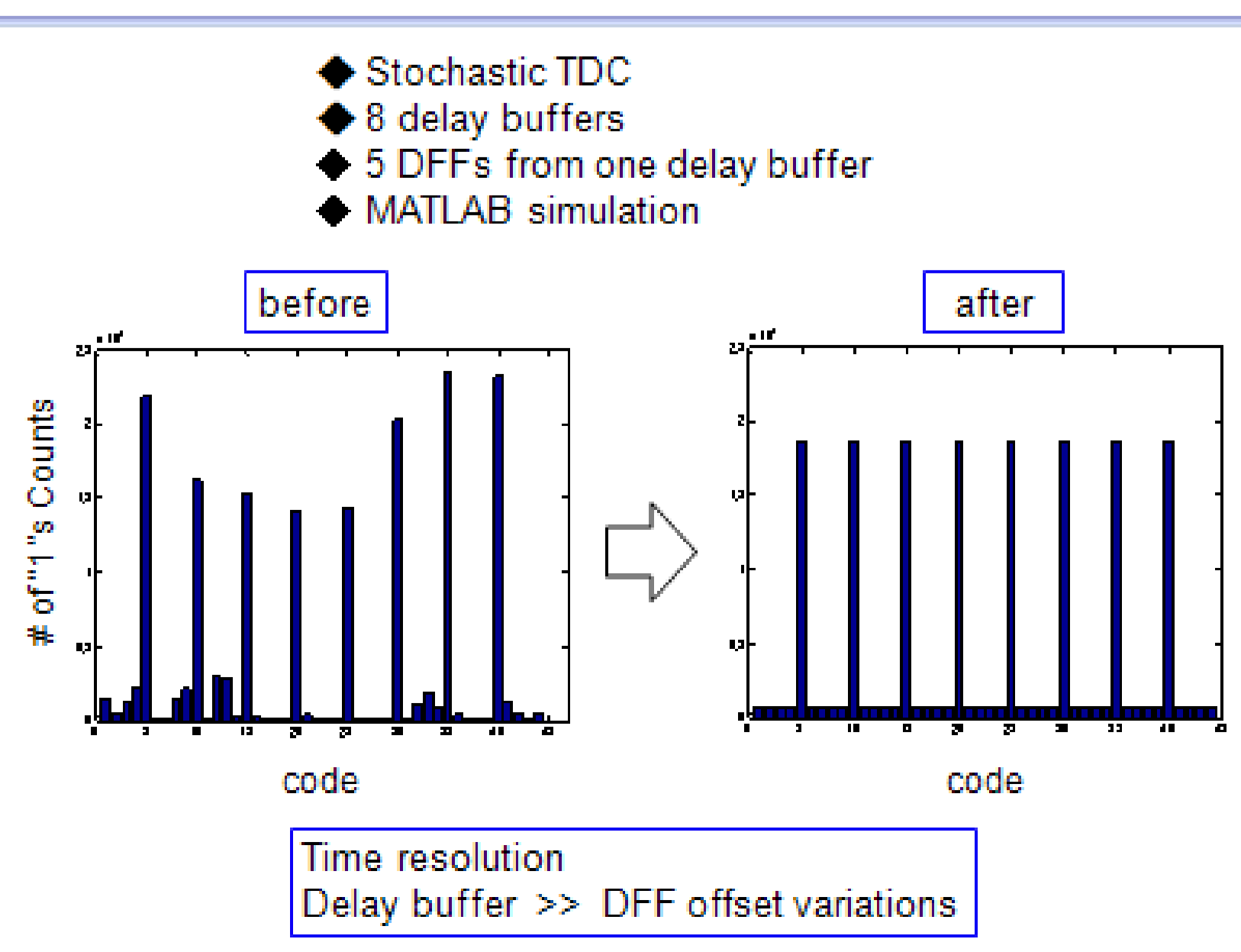


### Vernier Stochastic TDC



## Simulation Results

### Self-calibration Results



## Summary

### Conclusion

- We propose Vernier Stochastic TDC as TDC for fine time resolution and good linearity.
  - For fine time resolution
    - Vernier technique (using two delay lines)
    - Stochastic topology (using process variations)
  - For good linearity
    - Self-calibration (using a two-ring-oscillator, signal is "time")
- All digital circuit
- Suitable for advanced fine CMOS implementation

### Our Publication

[1] S. Ito, S. Nishimura, H. Kobayashi, et al., "Stochastic TDC Architecture with Self-Calibration," IEEE Asia Pacific Conference on Circuits and Systems (Dec. 2010).

[2] S. Uemori, M. Ishii, H. Kobayashi, Y. Doi, O. Kobayashi, T. Matsuura, K. Niitsu, F. Abe, D. Hirabayashi, "Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement", IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (May 2012).