Vernier Stochastic TDC Architecture with Self-Calibration

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This paper describes a vernier time-to-digital converter (TDC) architecture with digital self-calibration as well as stochastic topology to have good linearity and fine time-resolution (Fig.1).

TDC: The TDC measures the time interval between two edges, and TDC applications include phase comparators of all-digital PLLs, sensor interface circuits, modulation circuits, demodulation circuits, as well as TDC-based ADCs. The TDC will play an increasingly important role in the nano-CMOS era, because it is well suited to implementation with fine digital CMOS processes; a TDC consists mostly of digital circuitry, and resolution improves as switching speed increases. [1-3]

Vernier TDC [1] : A vernier TDC uses two delay lines: one, with a buffer delay of $\tau 1$, and the other, with a buffer delay of $\tau 2$. Time resolution is given by $\tau 1 - \tau 2$ (gate delay difference) which can be smaller than that of the basic TDC.

Self-Calibration [2]: The TDC may show nonlinearity characteristics due to delay-time mismatches among delay buffers; the proposed TDC self-calibration compensated for this nonlinearity. Our TDC uses a two-ring-oscillator configuration in the self-calibration mode. Since the oscillation frequencies of the two oscillators are different from each other and not synchronized, the histograms in all bins would be equal if the TDC had perfect linearity. In reality there is nonlinearity and the histogram in each bin fluctuates being proportional to DNL (Fig.2).

Stochastic Topology [1] : Next we consider to utilize the large variation in circuit characteristics of fine CMOS to obtain fine time resolution. We connect each delay buffer output to the data inputs of several DFFs (Fig.1). Since setup and hold times of the DFFs are not identical due to process variations, the edge timing which changes DFF output from 0 to 1 can be different among these DFFs. Then their statistical variation becomes the effective time resolution of the TDC, which is generally finer than the buffer delay τ.

Proposed TDC Architecture: Our proposed TDC is a combination of the above vernier technique, self-calibration, and stochastic topology for fine resolution and good linearity (Figs.1, 2), which is suitable for advanced fine CMOS implementation.

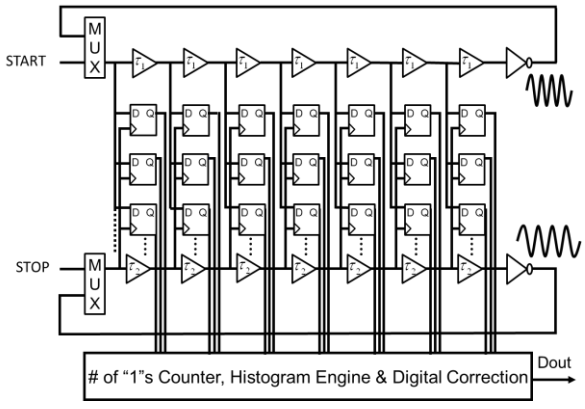

Fig.1 Proposed TDC architecture.

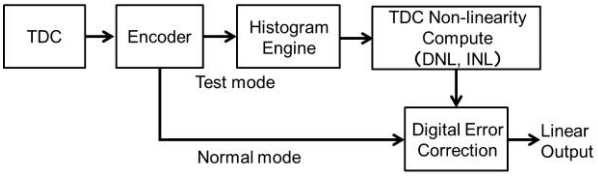

Fig.2 Self-calibration flow for TDC linearity Improvement [2].

References:

[1] Y. Park, D. D. Wentzloff, "A Cyclic Vernier TDC for ADPLLs Synthesized from a Standard Cell Library," IEEE Trans. on Circuits and Systems, vol.58, no.7, pp. 1511-1517 (July 2011).
[2] S. Ito, S. Nishimura, H. Kobayashi, et. al., "Stochastic TDC Architecture with Self-Calibration," IEEE Asia Pacific Conference on Circuits and Systems (Dec. 2010).
[3] S. Uemori, M. Ishii, H. Kobayashi, Y. Doi, O. Kobayashi, T. Matsuura,K. Niitsu, F. Abe, D. Hirabayashi, "Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement", IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (May 2012).