

Self-Calibration Technique of Pipeline ADC Using Cyclic Configuration

Yohei Tan, Daiki Oki, Yu Liu, Zachary Nosker, Haruo Kobayashi, Osamu Kobayashi ²⁾,
Tatsuji Matsuura, Atsuhiko Katayama, Li Quan, Ensi Li, Kiichi Niitsu, Nobukazu Takai
Department of Electronics, Graduate School of Engineering Gunma University,

1-5-1 Tenjin-cho, Kiryu 376-8515, Japan K_haruo@el.gunma-u.ac.jp

²⁾Semiconductor Technology Academic Research Center (STARC), Yokohama 222-0033 Japan

This paper proposes a self-calibration technique for a pipelined ADC with cyclic ADC structure. In this technique, the pipelined ADC is composed of a series of cyclic ADCs and each stage has independent digital self-calibration (Fig.1). We consider that if we measure the errors of sub-ADCs at the earlier stages by themselves in the pipelined ADC, the self-calibration accuracy would be improved. The most important and accurate stage is the first stage (which is designed to consume relatively large power to achieve high accuracy) in the pipelined ADC, and hence we consider that the errors of the first stage should be measured by the first stage itself instead of the later stages (which are designed to be relatively inaccurate with low power). Because of this, our technique achieves higher accuracy calibration than the conventional method that calibrates by using later stages [1].

Applying the proposed method, we have simulated the pipelined ADC with MATLAB and shown that higher accuracy calibration can be achieved with a smaller number of pipeline stages (i.e., high accuracy and low power can be realized). Fig.2 shows one of simulation results and Fig.3 shows a circuit design example for cyclic ADC operation in calibration mode. We expect that such a self-calibration technique would become more important in nano CMOS era [2].

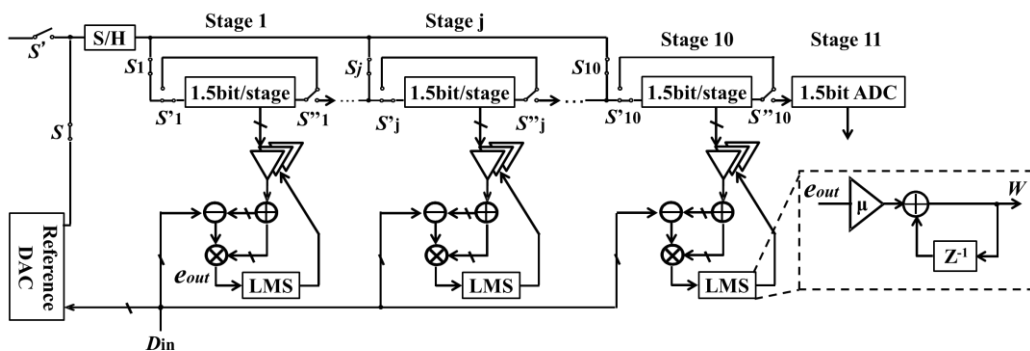


Fig. 1 Proposed 10-bit pipeline ADC with self-calibration.

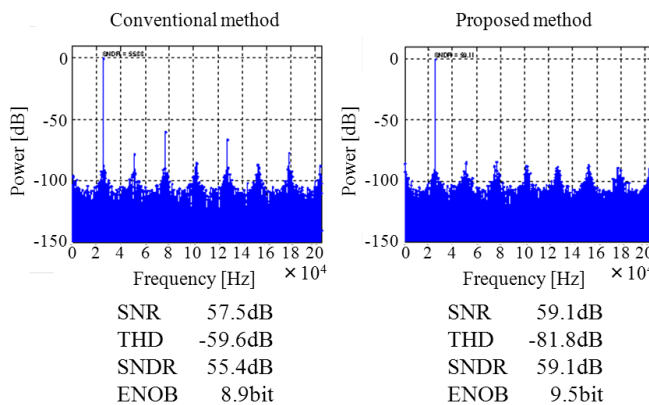


Fig. 2 FFT result of ADC output

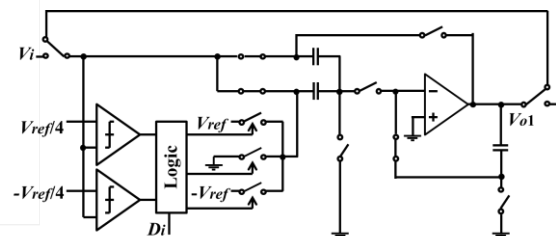


Fig. 3 Circuit design of cyclic ADC configuration at each stage in calibration mode .

- [1] A. Verma, B. Razavi, "A 10b 500MS/s 55mW CMOS ADC", IEEE ISSCC (Feb. 2009).
[2] T. Yagi, K. Usui, T. Matsuura, S. Uemori, Y. Tan, S. Ito, H. Kobayashi, "Background Calibration Algorithm for Pipelined ADC with Open-Loop Residue Amplifier Using Split ADC Scheme", IEICE Trans. on Electronics, Vol.E94-C, no.7, pp. 1233-1236 (July 2011).