P51 Self-Calibration Technique of Pipeline ADC Using Cyclic Configuration

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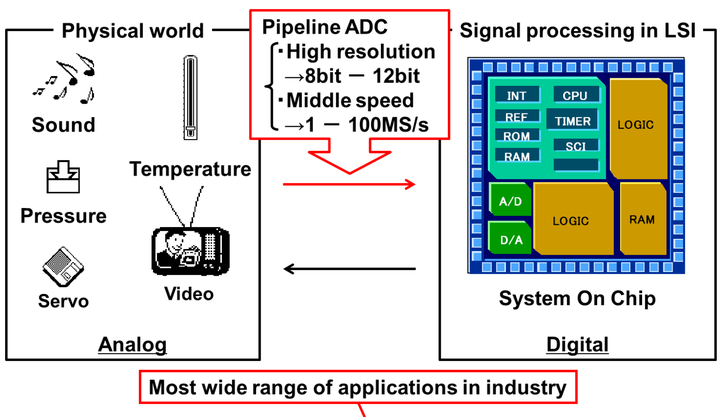
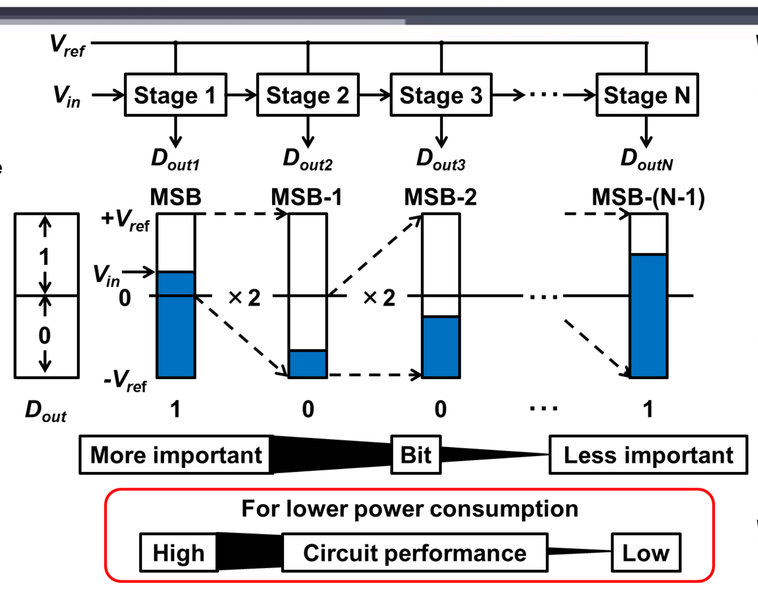
Introduction

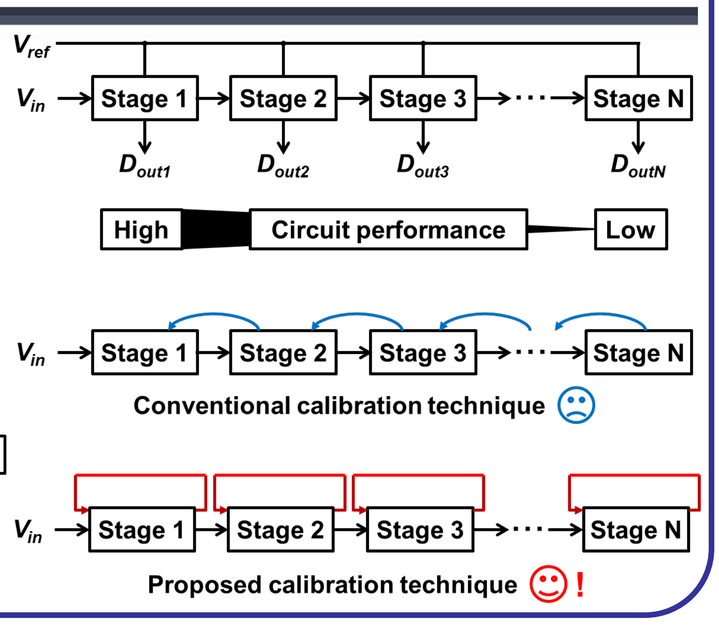
Research Objective



Pipeline ADC Configuration

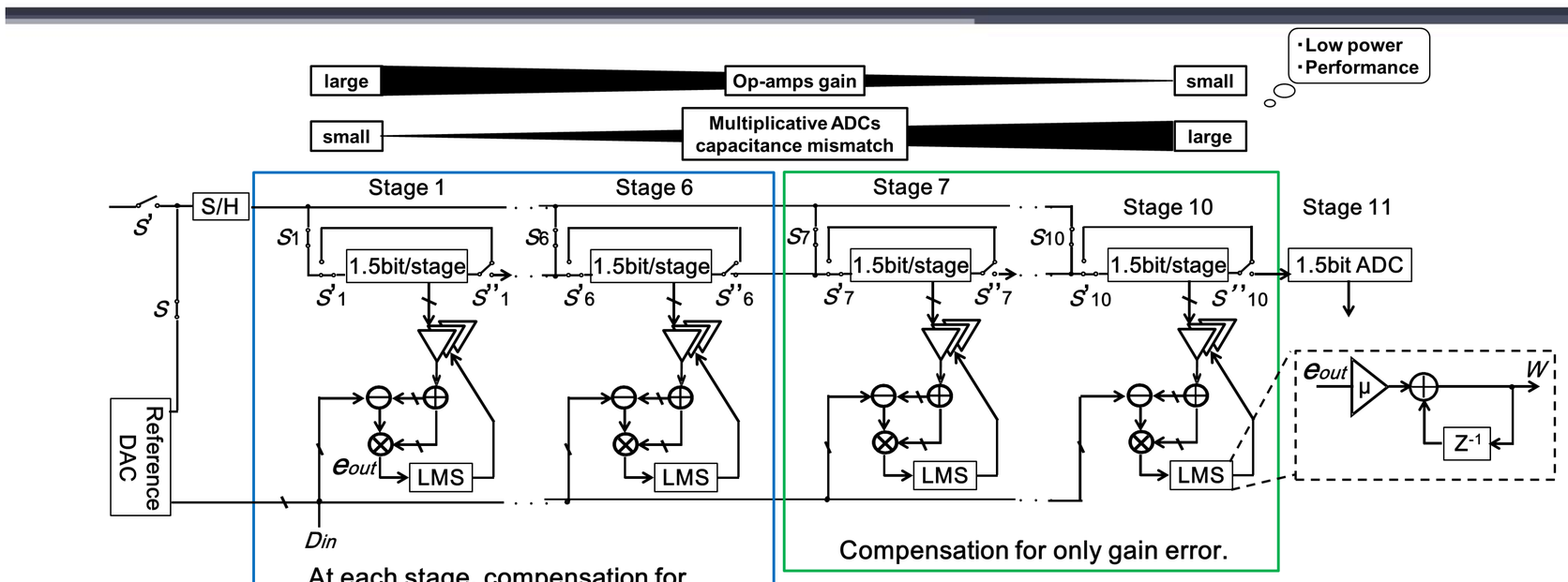


Concept of This Work



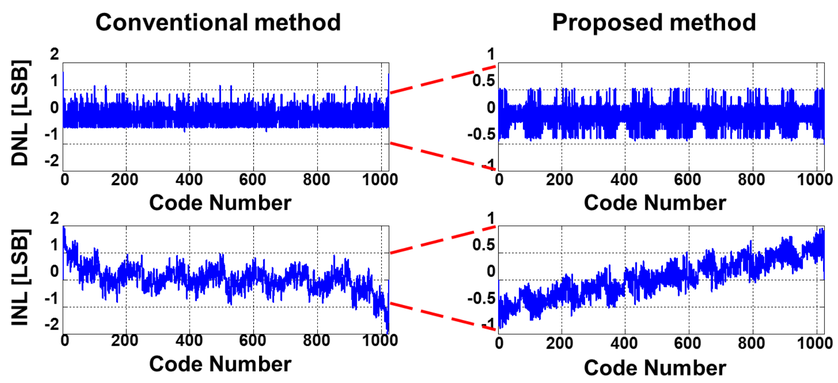
Proposed Calibration Technique

Proposed 10-bit Pipeline ADC with Self-Calibration



Verification with MATLAB Simulation

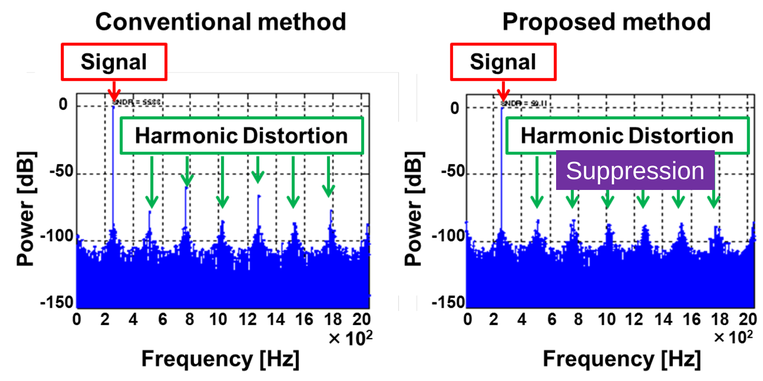
DNL and INL Simulation Results



MAX DNL:+1.6/-0.55
MAX INL :+2.1/-2

MAX DNL:+0.52/-0.52
MAX INL :+0.95/-0.91

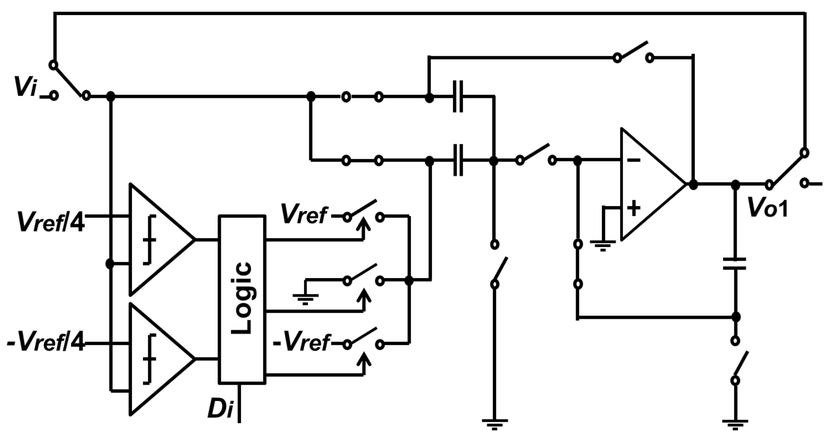
FFT Results of ADC Output



	Conventional method	Proposed method
SNR	57.5dB	59.1dB
THD	-59.6dB	-81.8dB
SNDR	55.4dB	59.1dB
ENOB	8.9bit	9.5bit

Circuit Design

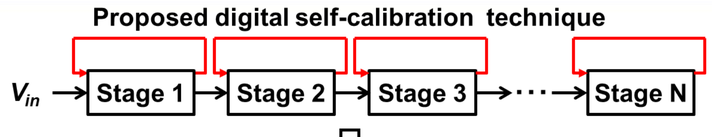
Cyclic ADC Configuration of Each Stage in Calibration Mode



Summary

Conclusion

Proposed digital self-calibration technique



Higher accuracy calibration

	Conventional technique	Proposed technique
Linearity	MAX DNL:+2.1/-0.72 MAX INL :+2.5/-2.5	MAX DNL:+0.73/-0.63 MAX INL :+1/-0.98
SNR	53.4dB	58.1dB
THD	-59.2dB	-72.9dB
SNOB	52.4dB	58.2dB
ENOB	8.4bit	9.4bit

References

[1] A. Verma, B. Razavi, "A 10b 500MS/s 55mW CMOS ADC", IEEE ISSCC (Feb. 2009).

[2] T. Yagi, K. Usui, T. Matsuura, S. Uemori, Y. Tan, S. Ito, H. Kobayashi,"Background Calibration Algorithm for Pipelined ADC with Open-Loop Residue Amplifier Using Split ADC Scheme", IEICE Trans. on Electronics, Vol.E94-C, no.7, pp. 1233-1236 (July 2011).