

# P54 High Resolution On-Chip Measurement Technique - New Analog-BIST Scheme Using Comparator Delay -

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Supported by STARC

## Background & Objective

### Research Objective:

Development of on-chip measurement circuit for **Milli-Volt order** high resolution voltage detection

### Innovation:

• **Time-domain signal processing**

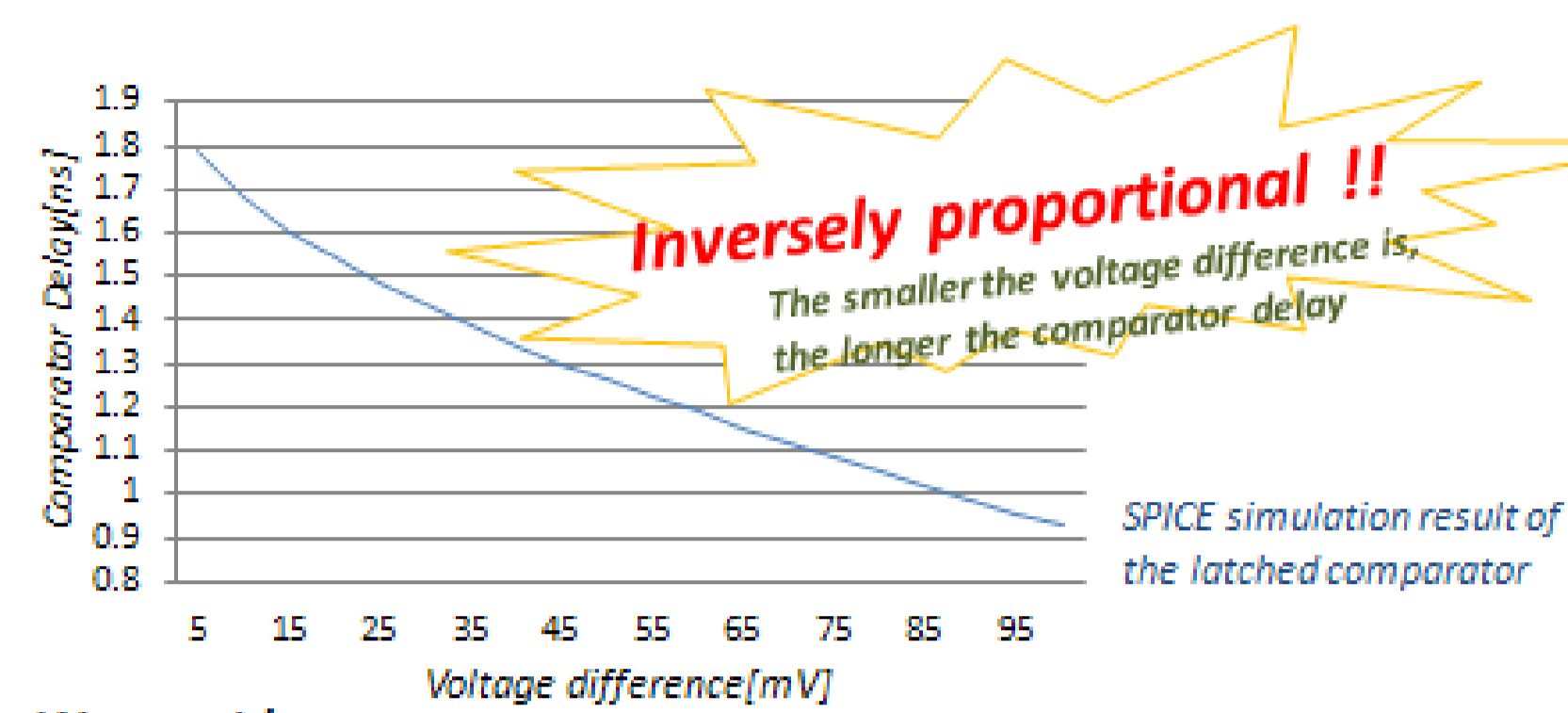
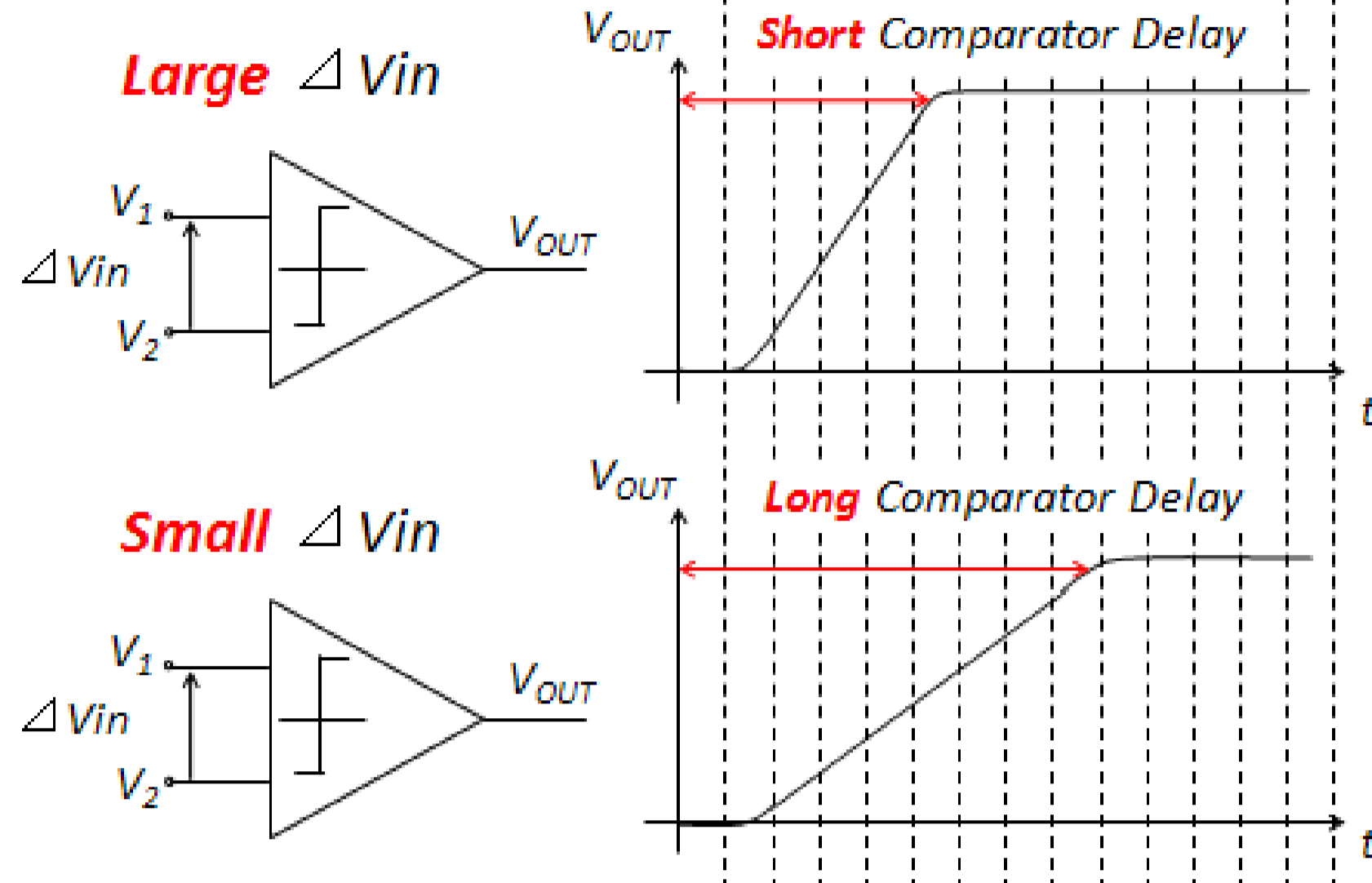
The smaller  $\Delta V_{in}$  is, the longer the delay is.  
 → The easier its detection is.

• **Simple** circuit implementation

### Application:

Analog Built-In-Self-Test & Measurement scheme for high precision Digital-to-Analog Converter

## Principle of proposed method



### We provide

- Measurement result,  $\Delta V$  and  $\Delta I$
- Test result, PASS or FAIL

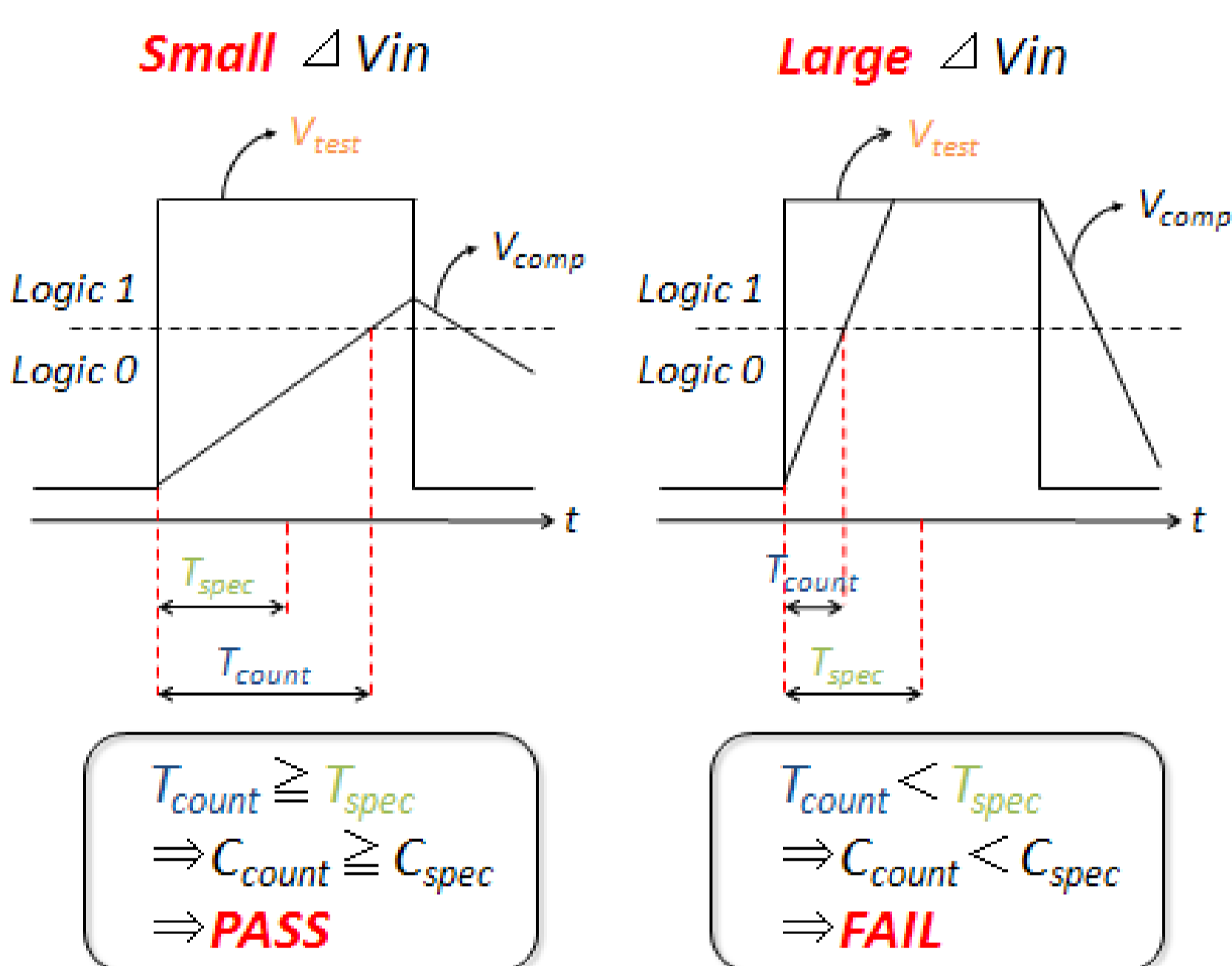
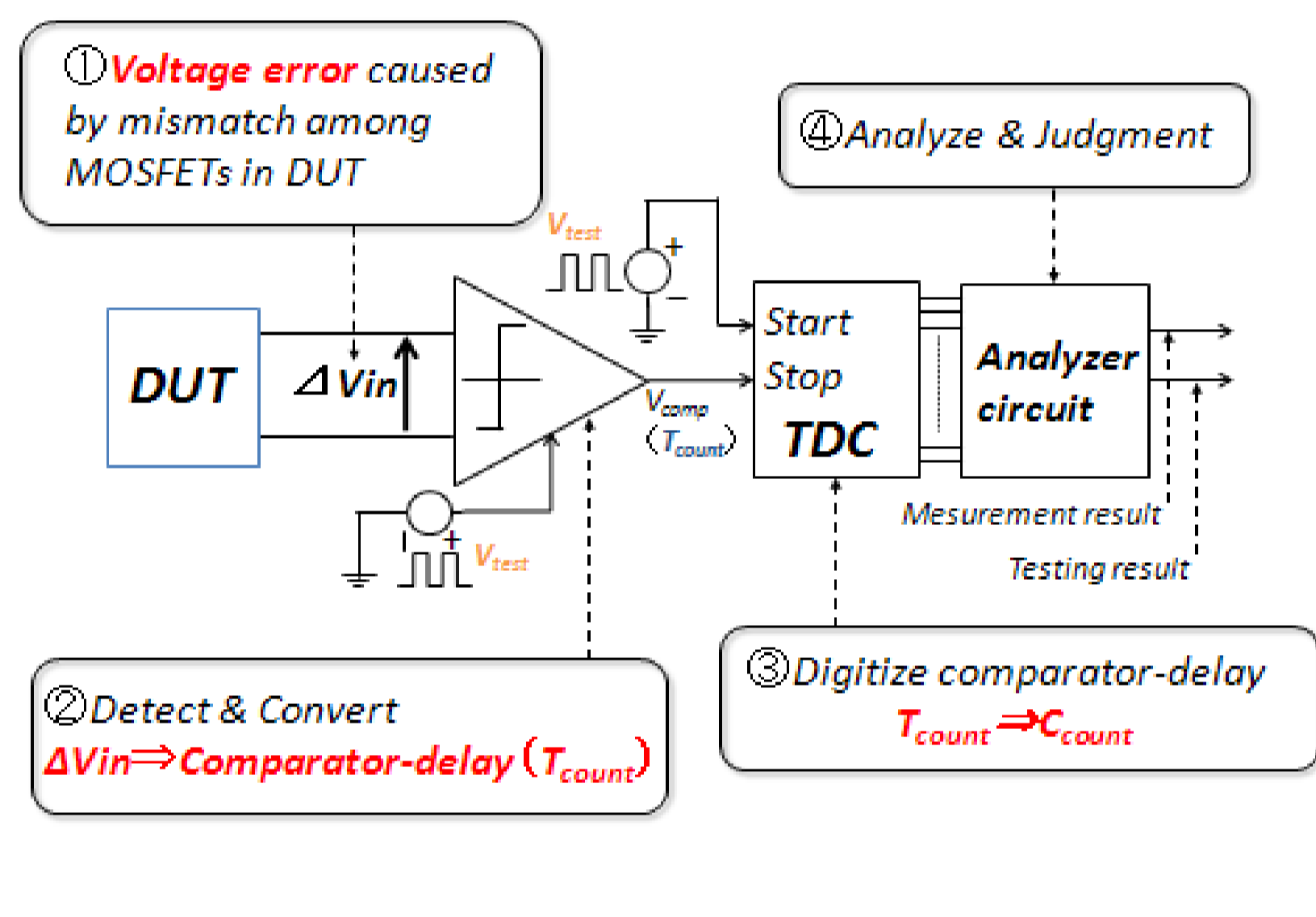
### We use

This inversely proportional relationship

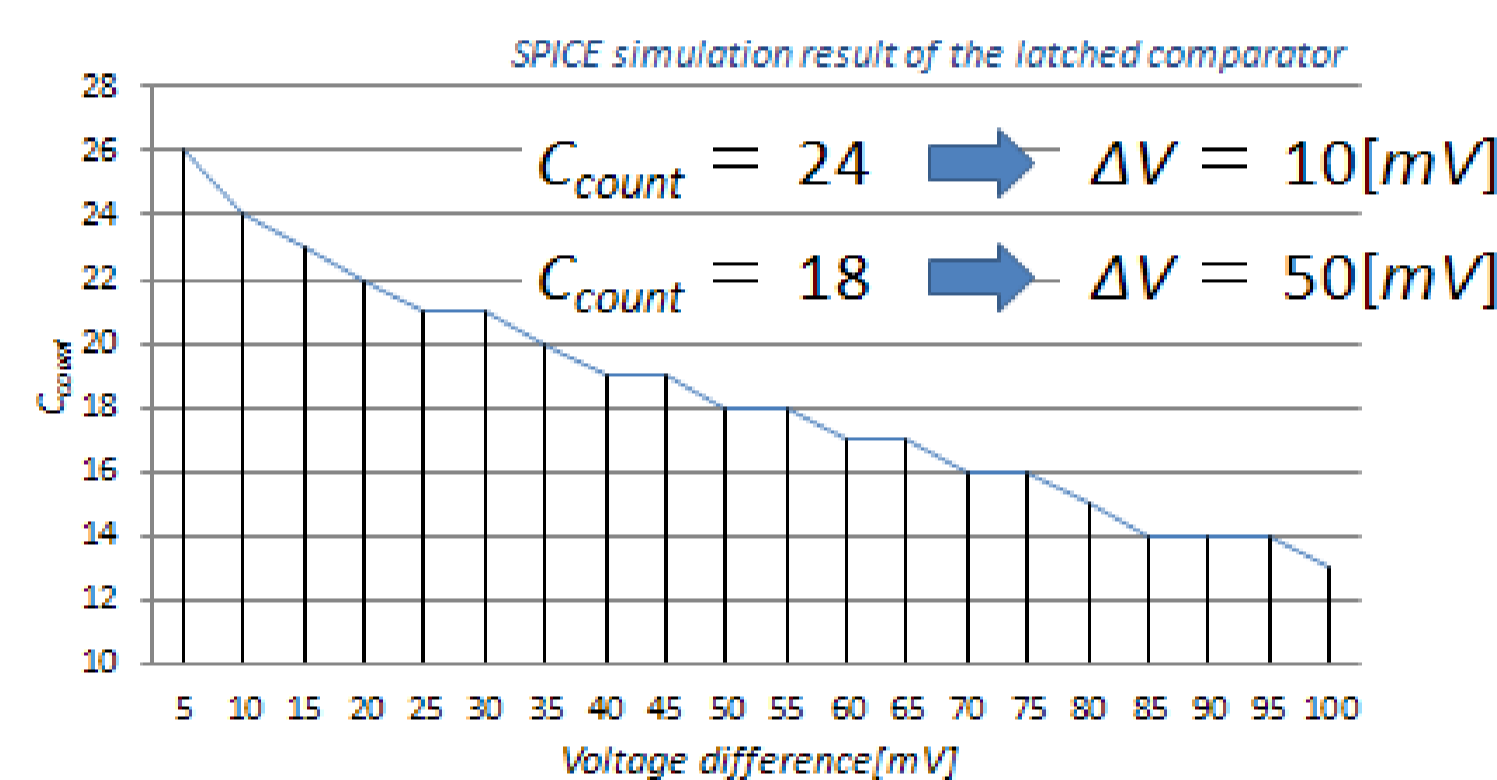
### Merit

The smaller the voltage difference is, the easier to detect

## Concept of proposed BIST scheme



## Measurement Method



Examine this characteristics in advance

Robust against process variation

Proposed Test Method

## Simulation Result

Test target: Current Steering DAC

#of Test: 10/Current-Source

Failure condition:  $C_{count} < 8$

Supply voltage variation:  $V_{pp} = 66.7[mV]$

SPICE simulation with 180nm CMOS

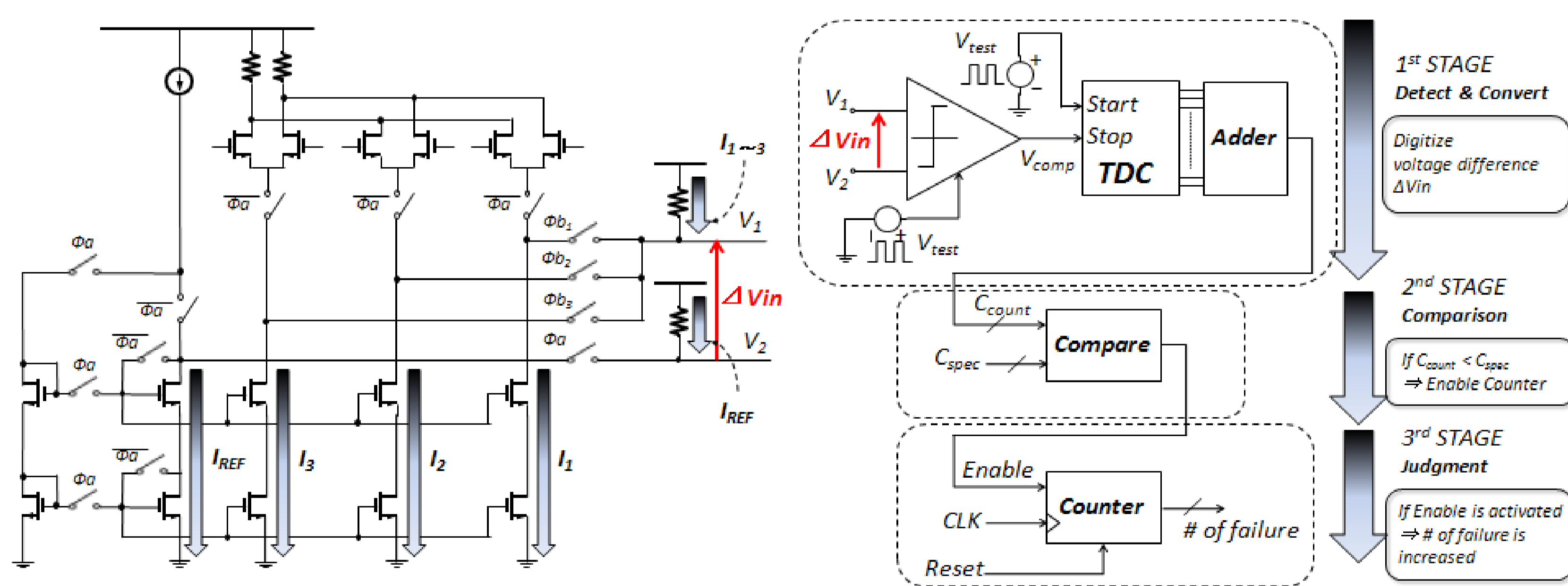
	$\Delta I [\mu A]$	$\Delta V [mV]$	$C_{count}$	#of Failure	Testing Result
I1	0	0	27, 28	0	PASS
I2	5.723	51.51	16, 17	0	PASS
I3	11.77	105.9	11	0	PASS
I4	18.13	163.2	8	0	PASS
I5	24.81	223.3	7	10	FALSE
I6	31.84	286.5	6	10	FALSE
I7	39.22	353	5	10	FALSE

This is robust against supply voltage variation

## Summary

- Proposal of on-chip measurement and analog BIST scheme
  - Milli-Volt order high resolution voltage detection
  - Simple circuit
  - Robust against process, supply voltage variation
- SPICE simulation demonstrates the effectiveness of the proposed scheme.

Application Example



## Current Source Test for Current Scaling DAC

