High Resolution On-Chip Measurement Technique
- New Analog-BIST Scheme Using Comparator Delay -

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This paper presents a high resolution on-chip measurement technique for very small voltage or current difference between two signals using comparator delay; this can be a new analog-BIST (Built-In Self-Test) scheme [1] to measure such as current source mismatches caused by mismatch among MOSFETs in a digital-to-analog converter. The comparator output delay is *inversely* proportional to the input voltage difference (Figs.1, 2); the smaller the voltage difference is , the easier to measure with this technique, and this is a very important feature to enable very small voltage detection. We use a time-to-digital converter (TDC) to measure the delay to have digital compatibility.

Fig.3 illustrates the proposed analog-BISTscheme. It is composed of a latched-comparator , a flash-TDC[2], and some digital circuits. We have performed circuit level SPICE simulation with TSMC 0.18um CMOS parameters to validate the effectiveness of the proposed technique and analog BIST scheme.

Here are some remarks for practical applications:

(i) The relationship between the input voltage difference and the comparator delay can change due to process variation, supply voltage and temperature. However, self-calibration mechanism can be simply incorporated by providing one referencence voltage (such as bandgap reference voltage) and voltage divider circuit composed of a voltage follower, a resistor ladder and some MOS switches. .

(ii) The accurate and fine resolution measurement of signals inside an LSI is only possible if we use on-chip circuit cooporated with external measurement instruments.

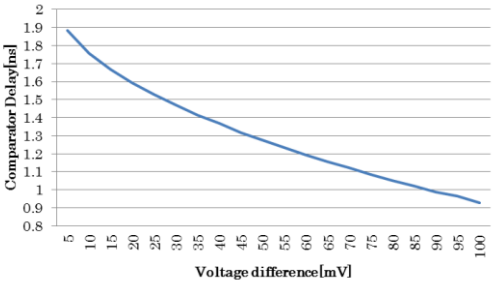

Fig. 2 SPICE simulation result of the input voltage difference vs comparator delay.

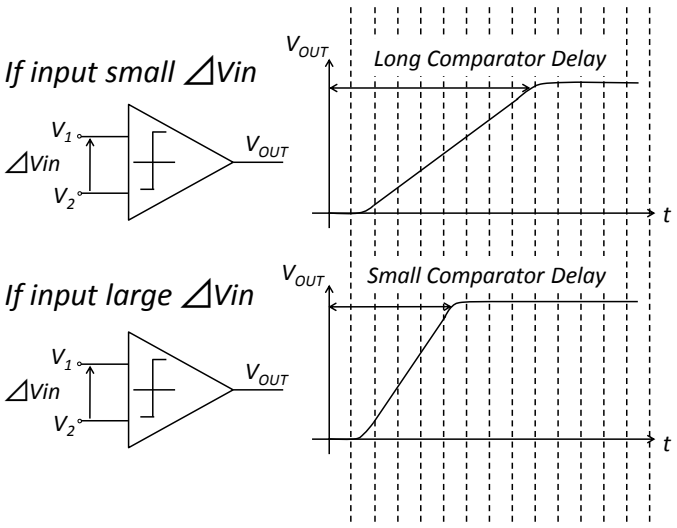

Fig. 1 Comparator output waveforms for small and large input voltage diferrences

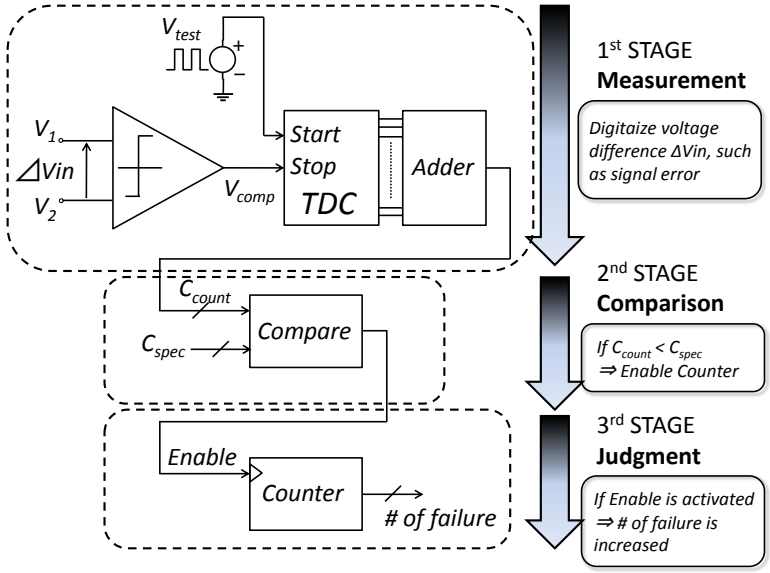

Fig. 3 Overview of the proposed analog-BIST scheme.

[1] K.-T. Cheng, H.-M. Chang, "Recent Advances in Analog, Mixed-Signal and RF Testing", IPSJ Trans. on System LSI Design Methodology (Feb. 2010).
[2] P. M. Levine, G. W. Roberts, "A High Resolution Time-to-Digital Converter and Calibration Scheme" , IEEE International Test Conference (2004).