

High Resolution On-Chip Measurement Technique -New Analog-BIST Scheme Using Comparator Delay-

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Research Objective:

Development of on-chip measurement circuit
for **Milli-Volt order** high resolution voltage detection

Innovation:

• **Time-domain signal processing**

The smaller ΔV_{in} is, the longer the delay is.



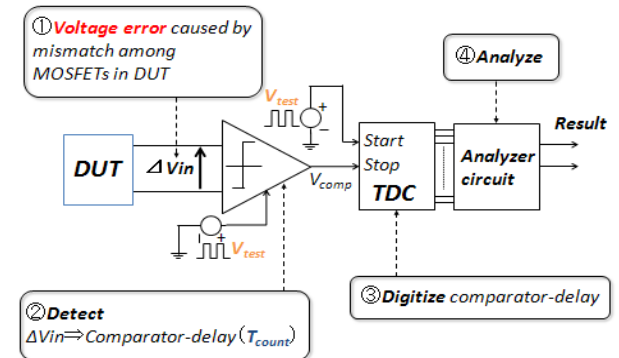
The easier its detection is.

• **Simple** circuit implementation

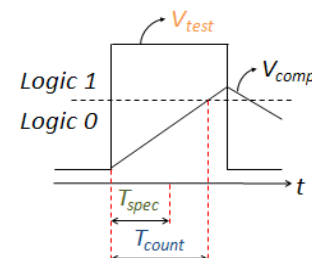
Application:

Analog Built-In-Self-Test & Measurement scheme
for high-precision Digital-to-Analog Converters

Concept of proposed BIST scheme

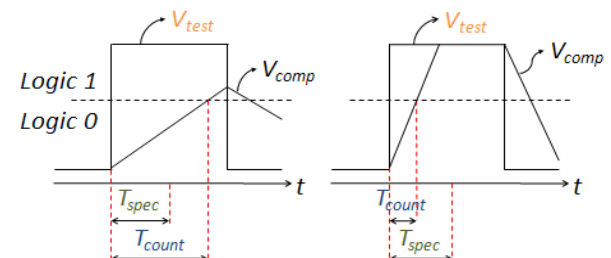


Small ΔV_{in}



$T_{count} \geq T_{spec}$
⇒ **PASS**

Large ΔV_{in}



$T_{count} < T_{spec}$
⇒ **FAIL**