Self-Calibration Technique of Cyclic ADC

Yu Liu, Haruo Kobayashi, Tatsuji Matsuura, Oamu Kobayashi † , Nobukazu Takai, Kiichi Niitsu
Department of Electronics, Graduate School of Engineering Gunma University,
1-5-1 Tenjin-cho, Kiryu 376-8515 Japan k_haruo@el.gunma-u.ac.jp
† Semiconductor Technology Academic Research Center (STARC), Yokohama 222-0033 Japan

This paper proposes a self-calibration technique for a cyclicADC. In this technique, the cyclic ADC is composed of two comparators, an MDAC, an amplifier by a factor of 2.0, digital calibration logic and a reference DAC (whose resolution is the same as that of the cyclic ADC) (Fig.1). The cyclic ADC works in two modes; high-power mode and low-power mode. In high-power mode, the bias currents in the amplifier are large so that the amplifier works correctly and the capacitor mismatches associated with the MDAC are measured. In low-power operation mode, the bias currents are low and we can also measure the amplifier error effects in this mode. In normal operation, the cyclic ADC works in low power mode with calibration based on these measured errors.

We create a mathematical model of self-calibration for capacitor mismatches and amplifier finite gain effects (Figs. 2,3). We have simulated the cyclic ADC with the proposed calibration using MATLAB and shown that the capacitor mismatch and amplifier gain error effects are corrected (Fig.4, 5). We expect that such a self-calibration technique would become more important in nano CMOS era [1].

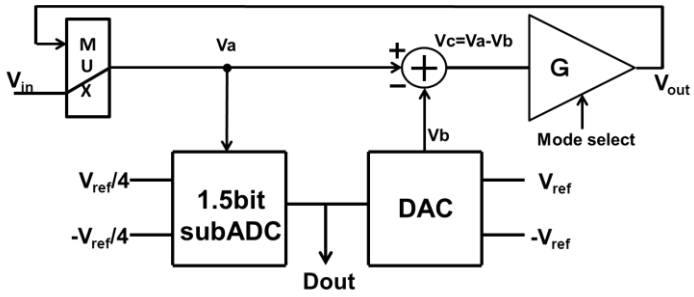

Fig. 1 CyclicADC block digagem.

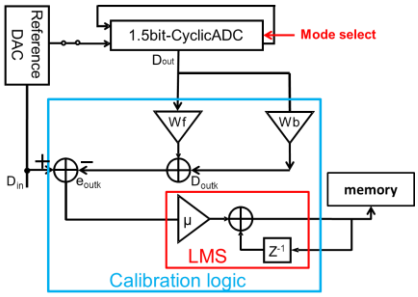

Fig. 2 Structure of the proposed calibration for cyclic ADC.

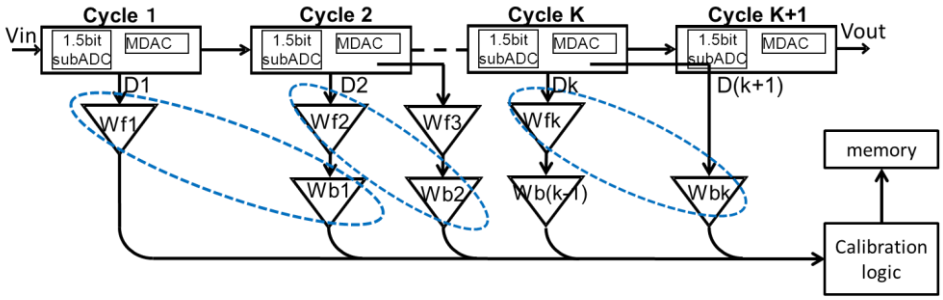

Fig.3 The proposed self-calibration operation for cyclic ADC.

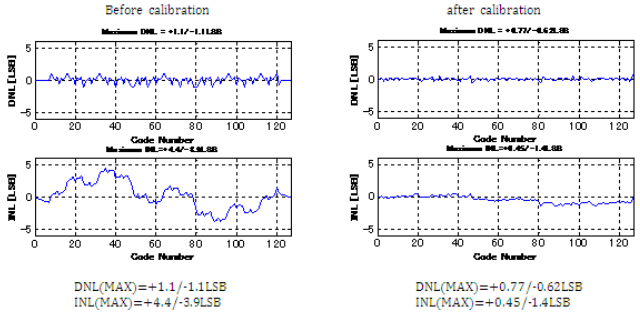

Fig. 4 DNL and INL of a 7bit cyclic ADC.

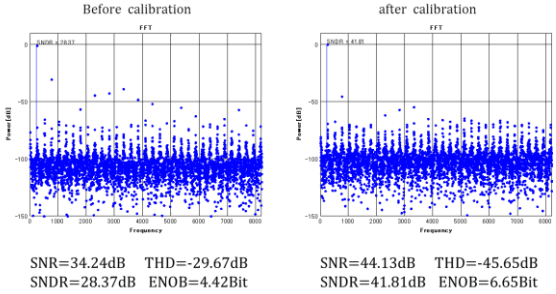

Fig.5 Power spectrum of a 7bit cyclic ADC.

[1] A. Verma, B. Razavi, “A 10b 500MS/s 55mW CMOS ADC”, IEEE ISSCC (Feb. 2009).