P56 A Self-Calibration Technique of Cyclic ADC

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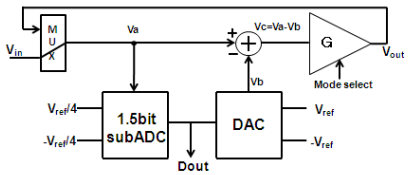
introduction

Research purpose

CyclicADC

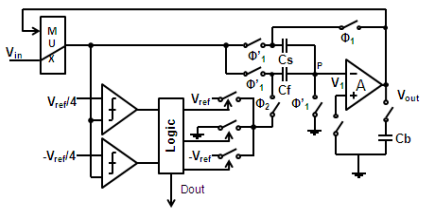
- Smaller chip area → Low cost applications
- Demands for further → low power, high accuracy
- Our goal is to develop a new Self-Calibration Technique to realize them

CyclicADC configuration & operation



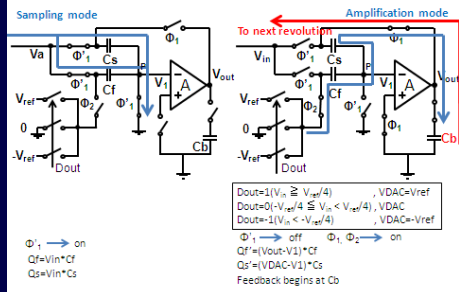
$$Vout = 2Vin - D \times Vref \qquad D = \begin{cases} 1 & (Vin \geqq Vref/4 \quad Vb = Vref) \\ 0 & (-Vref/4 \leqq Vin \leqq Vref/4 \quad Vb = 0) \\ -1 & (Vin \leqq -Vref/4 \quad Vb = Vref) \end{cases}$$

CyclicADC Circuit



Proposed test method

CyclicADC Circuit operation



Transfer function of CyclicADC

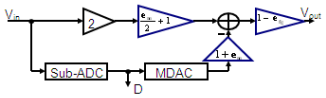
Calculate the transfer function with charge conservation in P

$$-Qf - Qs = -Qf' - Qs' \quad , \quad V1 = Vout/A$$

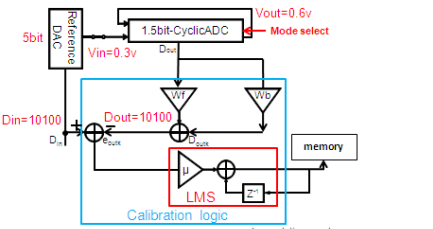
$$Vout = \frac{Vin - D \times VDAC \times \frac{Cs}{Cs+Cf} - \frac{Cf}{Cf+Cs} \times \frac{1}{A}}{\frac{Cf}{Cf+Cs} - \frac{1}{A}} = \frac{\left(1+\frac{Cs}{Cf}\right)Vin - \frac{Cs}{Cf} \times D \times VDAC}{1 + \frac{1}{A\beta}}$$

A:amp gain
Capacitor mismatch : em=(Cs-Cf)/Cf
Finite gain : efg=1/Aβ

$$Vout = (1 - efg)\left(1 + \frac{em}{2}\right) \times 2Vin - (1 + em)D \times Vref)$$

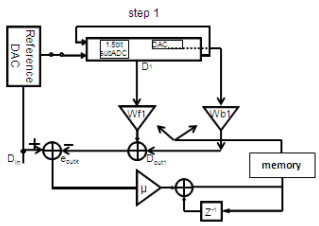


Proposed Self-Calibration block diagram

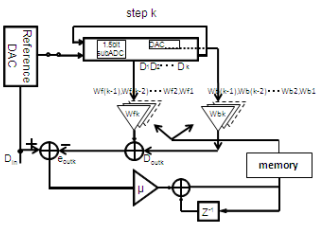


k:revolution number
μ:LMS step gain
Wf:capacitor mismatch error coefficient
Wb:amp error coefficient

Self-calibration at step 1

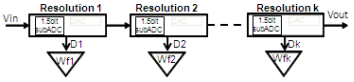


Self-calibration at step k

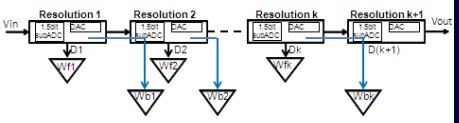


Error analysis

- In high-power mode → Measure capacitor mismatch error

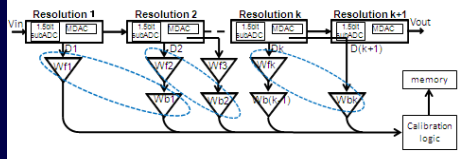


- In low power mode → Measure amp error(add one more resolution)

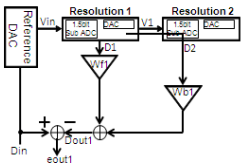


Error analysis(mathematical model)

- The circuit worked on different modes, the error of circuit is like this diagram.



Calibration coefficient calculation



- Calculate the difference of Din and Dout1

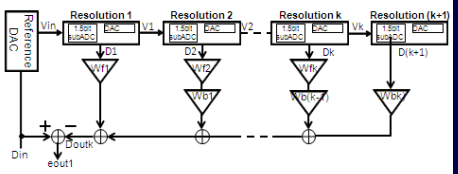
No.1 resolution

Dout1=Wf1*D1+Wb1*D2=Wf1*D1+Wb1*V1

V1=(1-efg)[(1+em/2)*2*Vin-(1+em)*D1*Vref]

Vref=1

Calibration coefficient calculation (continued)



No.(k+1) resolution

Doutk=Wf1*D1+Wf2*Wb1*D2+Wf3*Wb2*D3+・・・Wfk*Wb(k-1)*Dk+Wbk*D(k+1)

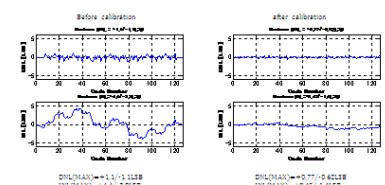
Vk=(1-efg)[(1+em/2)*2*V(k-1)-(1+em)*Dk*Vref]

Vref=1

Conclusion

Linearity (simultaion)

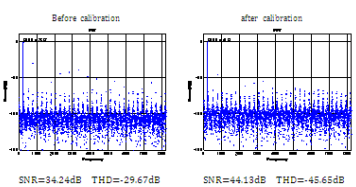
Resolution : 7bit
Sampling frequency : 2^16
Vref : 1
Step gain : μ=1/128
Amp error : efg=0.16
Capacitor mismatch error : em=0.08



- After the calibration, the linearity is better than before

Power spectrum(simulation)

Resolution : 7bit
Sampling frequency : 2^16
Vref : 1
Step gain : μ=1/128
Amp error : efg=0.16
Capacitor mismatch error : em=0.08



- After the calibration, SNDR is better than before

Conclusion

Novel Cyclic ADC Self-Calibration Technique

- High-power mode → Capacitor mismatch correction
- Low-power mode → Amp error correction

Verified with Matlab simulation