Analog/mixed-signal circuit design in nano CMOS era

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Abstract: This paper describes analog/mixed-signal circuit design in the nano CMOS era. Digitally-assisted analog technology is becoming more important, and as an example, our fully digital FPGA implementation of a TDC with self-calibration is shown. Since pure analog circuits are still present and "good" device modeling is required for their designs, device modeling technology for nano CMOS with complicated behavior is also reviewed.

Keywords: digitally-assisted analog technology, self-calibration, error correction, dynamic matching, FPGA, device modeling

Classification: Integrated circuits

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1 What is required for AMS design in nano CMOS SOC

In current Systems-on-a-Chip (SoC), digital technology is dominant although there are usually some analog circuits present. Most devices are targeted for digital circuit improvement; if the design of analog/mixed-signal (AMS) circuits were taken into account, the manufacturing cost would increase. The role of AMS circuit designers, who have to be very adaptive, is to design high-performance AMS circuits utilizing digital-friendly devices. Nano CMOS processes are digital device oriented and AMS designers face challenges of

low voltage supply, small intrinsic gain and large device parameter variation as well as reliability and testing problems. The solution to this problem has been suggested as *digitally-assisted analog technology*, which utilizes digital technology extensively for AMS circuit performance improvement.

As CMOS processes scale down, design and implementation of a full custom SoC becomes more difficult technically and economically. On the other hand, a field programmable gate array (FPGA) is attractive due to its flexibility, and it can be used for so-called *disruptive innovation.* We consider that FPGA implementation (design, simulation, verification, and testing) of all AMS, logic and memory would be one of the goals for the digitally-assisted analog technology.

However the digitally-assisted analog technology cannot solve everything in practice. Analog circuits such as analog filters, operational amplifiers, low noise amplifiers, RF amplifiers, and power amplifiers often require sophisticated analog circuit design. Additionally, reliability and testing are serious issues. In this case, "good" nano CMOS device models—an interface between circuit designers and process/device engineers—is necessary because nano CMOS devices behavior is complicated.

We review the digitally-assisted analog technology in Section 2, and show an example, the full digital design of a time-to-digital converter with self-calibration in Section 3. Then we review nano CMOS device modeling in Section 4 and provide a conclusion in Section 5.

2 Digitally-assisted analog technologies

We consider that signals and circuits can be classified into four domains as shown in Fig. 1 and Table I. All four of these domains have to be fully utilized to realize high-performance AMS circuits in nano CMOS SoCs.

One of the goals for digitally-assisted analog technology is full digital implementation (design, simulation, verification, and testing) of all AMS, logic and memory due to the following benefits for digital circuits:
- Small chip area, low power, and high performance
- Easy to design, verify, and test
- Process portability, scalability
- Programmability
- Successful working chip of the first prototype.

(a) (b)
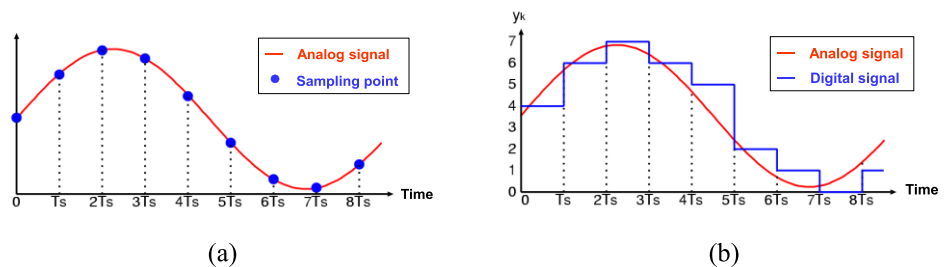
Fig. 1. (a) Time quantization (sampling). (b) Amplitude quantization.

Table I. Circuit and signal classification in 4 domains.

	Continuous Time	Discrete Time
Continuous Amplitude	Domain 1 (pure analog)	Domain 2 (sampling)
Discrete Amplitude	Domain 3 (TDC, PWM)	Domain 4 (digital)

2.1 Circuit in domain 1 (continuous time and amplitude: pure analog circuit)

(i) Uses all MOSFET operation regions (saturation, velocity saturation, triode, and sub-threshold regions).

(ii) Uses standard CMOS logic-like circuits (such as Nauta operational transconductance amplifier (OTA) which uses CMOS inverter-like circuits (Fig. 2)) for low voltage analog circuits.

(iii) *Anti-scaling analog circuits* are another possibility (which is opposite to digitally-assisted analog technology), where the analog circuit designer adjusts the sizes of R, C, and MOSFETs. Matching characteristics are better with fine CMOS process, and calibration would not be required.
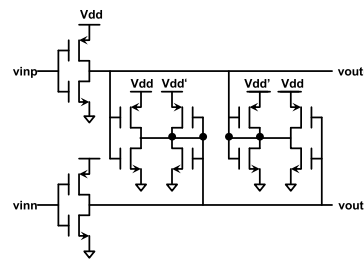
Fig. 2. Nauta OTA.

2.2 Circuit in domain 2 (discrete-time analog circuit)

Many waveform sampling techniques (such as oversampling, under-sampling, subsampling, quadrature sampling, and non-uniform sampling) are effective in nano CMOS. This is because sampling speed becomes high and sampling non-idealities such as jitter, and finite aperture time are reduced. Delta-sigma modulation techniques become more important, where digital rich circuits and oversampling techniques are fully utilized. Also sampling mixers with down/up sampling are often used to achieve high performance. Additionally, switched capacitor circuits can be used up to high frequency signal processing.

2.3 Circuit in domain 3 (time-domain analog circuit)

In nano CMOS, supply voltage decreases while the switching speed increases, and hence time domain analog circuits utilizing time resolution are effective [1], where a time-to-digital converter (TDC) plays an important role. The application to ADC, sensor interface (for such as capacitor, temperature), all digital PLL, and phase noise/jitter measurement are reported. Varieties of TDC architectures are proposed including flash, Vernier type, and delta-sigma TDCs [2, 3]. Many of them can be implemented only with

digital circuits. Note that as CMOS scaling progresses, the TDC performance improves, even though supply voltage decreases (though most analog circuits cannot hold this statement).

In time domain analog circuits, the signal is treated as "time" instead of "voltage". Furthermore, the "time" signal has some unique properties. Ring oscillators are often useful in this area. Also, clock synchronization and frequency division/multiplication can be positively utilized. Time continues infinitely and dynamic range of the time-domain analog circuit can be very wide if we use a long enough time interval. However we remark that in general handling "time" is more difficult than "voltage" in circuit design.

2.4 Circuit in domain 4 (digital compensation)

Digital compensation techniques for analog circuits can be classified into digital self-calibration, digital error correction and dynamic matching.

(1) Digital self-calibration technique has been used in electronic measurement instruments and it is now utilized inside an IC chip. Circuit non-idealities are measured and they are compensated by digital calculation [2]. This calibration is performed by the circuit itself without the user's recognition. For example, we have proposed a digital self-calibration method for timing skew effects in a time-interleaved ADC (Fig. 3), where the timing skew is detected by cross-correlation calculation among channel ADC outputs and compensated by our proposed linear-phase delay digital filter [4].
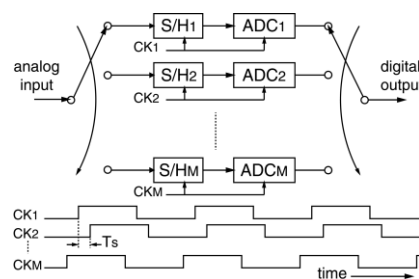

Fig. 3. A time-interleaved ADC system.

Digital self-calibration can be classified into foreground calibration and background calibration. Foreground calibration requires calibration time. The calibration may be done at testing/shipping where non-idealities are measured and the corrected data are stored in flash memory. Calibration may be done when the circuit starts to work with power supply, or it may be done during idle time when the circuit's normal operation stops. Background calibration is performed during the normal operation and its calibration time slot is not required; while this seems ideal, its actual industrial applications are limited because its algorithm convergence is difficult to guarantee. In many cases, foreground calibration uses measurement and control algorithms while background calibration uses adaptive/statistical signal processing algorithms, which are quite different.

(2) Digital error correction often uses redundancy in time (operations)

and/or space (circuits). For example, consider three identical digital circuits and provide them the same digital input (Fig. 4). Then feed their three digital outputs to the majority circuit. Even if one of three circuits works incorrectly and only two outputs are correct, we have the correct output from the majority circuit, which improves the reliability significantly.
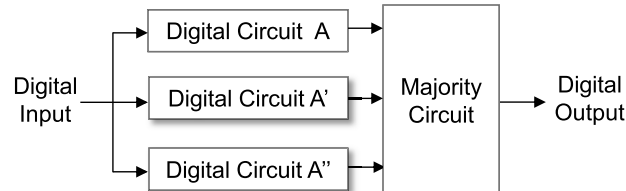
Fig. 4. Three identical digital circuits followed by majority circuit.

Another example is a non-binary successive approximation register (SAR) ADC (Fig. 5), where the number of steps is larger than a binary SAR ADC; in other words redundancy in time is used. Then reliability, low power, and fast operation are realized [5]. Non-binary algorithms may use radix $\gamma(1 < \gamma < 2)$, especially $\gamma = \sqrt{2}$ or Fibonacci/Tribonacci sequences. We have experiences that the time redundancy would often work better than the space redundancy when both redundancies are possible.
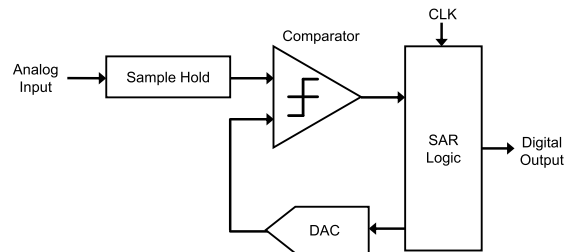
Fig. 5. Block diagram of SAR ADC.

The third example of the digital error correction is pre-distortion of a power amplifier where its non-idealities are measured and its digital input is nulled such that the non-idealities are compensated for. We have proposed a similar method for low distortion signal generation with an arbitrary waveform generator (AWG) but there we do not need to measure nonlinearities of the AWG [6].

(3) Dynamic matching also utilizes redundancy [2, 7]. It spreads out the non-idealities of circuit components in frequency domain without measuring them and their spectrum is shaped by their selection method. Many dynamic matching algorithms have been proposed for noise shaping types such as low-pass, band-pass, multi-band-pass, high-pass, complex band-pass, and complex multi-band-pass noise-shaping. This technique is mainly used in multi-bit delta-sigma DAC/ADC, which alleviates requirements for operational amplifiers and analog filters, and leads to a low power design. In other

words, the digital algorithm of the element selection assists in analog circuit power reduction.

Similar techniques are used in a random interleaved ADC [8], and also spread spectrum clocking in digital processor and power supply clocks. We propose a delta-sigma digital-to-time converter as a band select spread spectrum clocking generator [9].

Here are some remarks for the unified theory of digitally-assisted analog technology:

(1) Combination of digital and analog compensations is of course possible.

(2) Compensation techniques can be also classified into feedback and feed-forward methods. The feedback method measures circuit non-idealities whereas the feed-forward one does not. Feedback methods often use simple control and measurement algorithms.

(3) In self-calibration, a part of the circuits to be calibrated is often used as non-ideality measurement circuits. For example, calibration of capacitors in an SAR ADC sometimes uses the circuits themselves inside the SAR ADC (such as a comparator and SAR logic). Non-idealities of the first-stage in a pipeline ADC are measured by a sub ADC in the latter stage [10]. There may be a paradox that errors of one circuit is measured with another circuit which also has errors, and its self-calibration validity may be explained by *divide and conquer* of the dynamic range.

(4) The digitally-assisted analog technology has to be *mass-production-proof,* and consideration for mass production (such as yield/reliability/testing) is necessary. Its testing may be complicated because it tends to hide circuit non-idealities and they may appear in worse operating conditions. Also the calibration time may be long and included in the testing time. It is pointed out that strong dependence on the digitally-assisted technique often cannot suppress circuit variation effects enough in mass production.

(5) The digitally-assisted analog circuit designer needs knowledge of signal processing, measurement and control engineering, number theory/algorithm and power electronics as well as circuit design.

(6) *Analog-assisted digital technology* is also important. Its example is pre-emphasis/equalization techniques for high-speed digital interface circuits.

(7) For very high performance analog circuits, analog-friendly processes with (relatively) high supply voltage and traditional style analog circuit design is often more suitable.

(8) The circuit design progress has been realizing the following trends:
   - Analog technologies are being replaced with digital technologies. Digital technology is stable, reliable, and easy to implement.
   - Passive circuit elements (R, C, L) are being replaced with active circuit elements (transistors). Passive elements are linear and less noisy but they occupy a lot of chip area, and hence the circuit designer makes efforts to develop circuit techniques (including the digitally-assisted analog technology), in order to replace them with active elements (small chip area) without sacrificing circuit performance.
   - All active devices are being replaced with CMOS devices.

3 TDC calibration

A Time-to-Digital-Converter (TDC) is a popular on-chip delay measurement circuit. Time resolution of several picoseconds can be achieved when the TDC is implemented with an advanced CMOS process. TDC applications include phase comparators of all-digital PLLs, sensor interface circuits, modulation circuits, demodulation circuits, and delay measurement of memory interfaces and logic blocks [11, 12]. The TDC will play an increasingly important role in the nano-CMOS era, because it is well suited to implementation with fine digital CMOS processes; a TDC consists mostly of digital circuitry, and its time resolution improves as switching speed increases.

Although the resolution of TDC is high, the linearity of TDC is low. Therefore, self-calibration technique for high linearity is required. This section introduces the stochastic calibration techniques and shows its implementation to FPGA.

3.1 TDC architectures

The architecture of TDC is classified as flash TDC and delta-sigma TDC [2]. Flash TDC has two inputs for positive transitions. It measures the time interval between the two edges of the transitions. Although the function of the TDC is simple, there are several topologies for implementation. Datta et al. proposed the basic on-chip monotonic TDC [13]. The two-step TDC uses a delay-line TDC as a coarse TDC and a Vernier delay-line TDC as a fine TDC to achieve fine resolution and large detectable range [14]. Pei et al. also proposed the area efficient modified Vernier Delay Line (VDL) [15]. The feature of this method is delay range of each stage of VDL. The delay ranges increase by a factor of two gradually, which reduces the required number of stages. Therefore, the area is smaller. In this section, we focus on the calibration of a simple monotonic flash TDC.
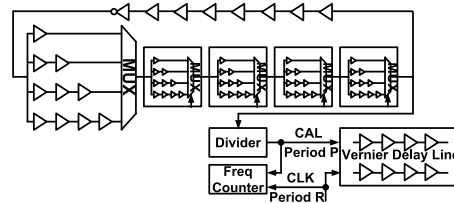
3.2 Stochastic calibration

Stochastic calibration is a calibration technique of TDC applied histogram method of ADC testing. A stochastic time interval sequence is applied with two uncorrelated oscillation signals. It can be implemented with lower extra area and no external Automatic Test Equipment (ATE). Therefore, it is attractive from the viewpoint of cost, the on-line usage, and the on-chip implementation. Several researchers have tried this method. Rivoir analyzed the stochastic calibration using a frequency selectable ring oscillator depicted in Fig. 6 and a clock generator [16, 17]. We proposed a stochastic calibration architecture using two ring oscillators shown in Fig. 7 [18], and analyzed it [19].

### 3.3 Implementation to FPGA

An 8-stage TDC with stochastic calibration system is implemented in the Xilinx Virtex5 FPGA board ML501 [20]. Figure 6 shows ML501 [21]. We confirm the convergence of the calibration with the implemented system.

The Subsection 3.3.1 shows the abstract of the implemented system. To get Differential Nonlinearity (DNL), the estimated delay of the buffers of TDC should be obtained. Subsection 3.3.2 describes the measurement method, and the measured result of the delay of the buffers of TDC. Subsection 3.3.3 gives the result of the evaluation of the DNL of the calibration.

Fig. 6. Ring-oscillator with 1024 selectable oscillation periods generating calibration events for a VDL-based TDC [16].
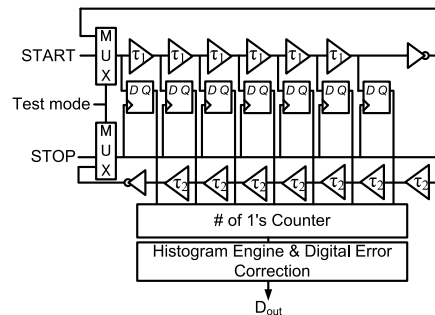
Fig. 7. TDC with stochastic calibration using two ring oscillators [18].

3.3.1 Implemented system

Figure 8 shows the implemented system on the FPGA board shown in Fig. 9. The system includes an 8 stage TDC. The TDC contains 7 buffers. The delay of the buffer of the ith stage is τ_i. The bit length of CNT_0-CNT_7 is 8. Six signal lines are connected to the START input of the TDC through selectors. We can send the external 27 MHz clock source, the output from Digital Clock Manager (DCM) DCM_{in0}, the output from the 16 stage ring oscillator, the 32 stage ring oscillator, the 48 stage ring oscillator, and the 64 stage ring oscillator to the START input.

We can send the external 100 MHz clock source, the output from DCM DCM_{in1}, the output from the 16 stage ring oscillator to the STOP input.

When the delay of buffers is measured, DCM_{in0}/DCM_{in1} are selected as START/STOP inputs.

When a calibration is performed, an external clock source or an output of a ring oscillator are selected as START and STOP inputs. Generally, the amount of jitter of an external clock source is less than that of a ring oscillator.
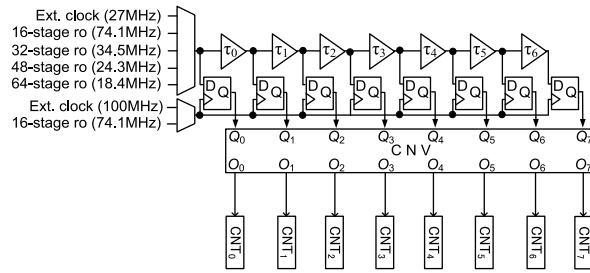
Fig. 8. Implemented system.
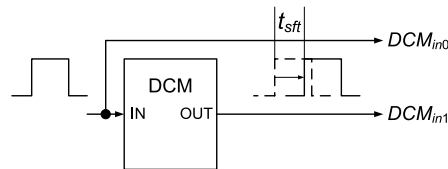

Fig. 9. Xilinx ML501 FPGA board.

Fig. 10. Interface between DCM and TDC.

3.3.2 Measurement of delay of buffers

We measure the delay of the buffers τ_0-τ_6 using the dynamic phase control function of DCM of Virtex5 [12]. DCM_{in0} is connected to the START input and DCM_{in1} is connected to the STOP input. Figure 10 shows the connection among DCM, DCM_{in0}, DCM_{in1}. The input IN of DCM is the source signal. The output OUT of DCM is a t_{sft} delayed signal of IN. The input IN is connected to DCM_{in0}, the output OUT is connected to DCM_{in1}. The delayed time t_{sft} is swept up from 0 to the cycle of the source signal. The resolution is 40 ps. By observing the t_{sft} and the corresponding measurement results, the delay of each buffer is estimated.

Table II shows the estimated delay of the buffers. These values are treated as the truth values of the buffers.

Table II. Estimated buffer delay.

Delay	τ_0	τ_1	τ_2	τ_3	τ_4	τ_5	τ_6
dl(ns)	0.70	0.63	0.39	0.70	0.12	0.43	0.20

3.3.3 Specification of calibration

Calibrations are performed in several pairs of the frequency of the upper ring oscillator F_0 and the frequency of the lower ring oscillator F_1 under the

condition that the number of the sampling of the calibration $N_{MEAS} = 4,096$. The DNLs are shown in Table III. We confirm the convergence of the error from the result.

Table III. Evaluation result of DNL.

F_0 (MHz)	F_1(MHz)	DNL_{4096}
74.1	34.5	0.026
74.1	24.3	0.033
74.1	18.4	0.044

3.4 Conclusion

This section shows that a TDC with its linearity calibration, which is an analog or mixed-signal circuit, can be implemented with fully digital circuits, or an FPGA, using HDL/Verilog instead of SPICE.

4 Nano-CMOS device modeling

In order to design SoC analog integrated circuits with nanometer CMOS devices, device modeling is the key to ensure the first prototype works. Device models and their model parameters should be accurate in any analog electrical ranges from low to high voltages and from DC to milli-meter wave frequencies. There are mainly two types of device models for nano-scale bulk MOSFETs used for analog integrated circuit design. The first is surface potential models, which include PSP model [22] developed by NXP Research (formerly part of Philips Research) and the group of Prof. Gildenblat at Arizona State University (formerly at Pennsylvania State University) and HiSIM2 model [23] developed by the group of Prof. Miura at Hiroshima University and Semiconductor Technology Academic Research Center (STARC). The second is charge based models, which include BSIM3, 4, and 6 models [24] developed by the BSIM (Berkeley Short-channel IGFET Model) Group, located in Department of Electrical Engineering and Computer Sciences at University of California, Berkeley and EKV model [25] developed by EPFL, Lausanne, Switzerland. Recently, BSIM and EKV models are merged in BSIM6. Both types of model have been tested by TechAmerica Compact Model Coalition (CMC) member companies to meet the needs of industrial users. Although CMC is an American council, most industries and academic organizations in the world use MOSFET models approved by CMC.

These models have been actively improved by their authors. Also, their model parameter extraction methods and software have been developed by design tool suppliers and device manufactures. However, from the circuit designers' point of view, many issues still remain for successful circuit simulations. As far as we studied, there are three major issues that need to be solved. One is the model operations in particular conditions, the second is the models for statistical simulations, and the last is the models for reliability simulations.

4.1 Forward body bias operation model of n-channel MOS-FETs

As an instance of the model operations in particular conditions, we will introduce forward body bias operation of nano-scale n-MOSFETs [26] modeling approach.

An effective approach to operate MOSFETs at low bias voltages is a forward body-biasing scheme for extending bulk-Si CMOS technology scaling. A forward body bias improves threshold voltage roll-off behavior and enables the use of shorter gates. To simulate circuits with the forward body-biasing scheme, the MOSFET model is the key to reproduce the effect accurately. However, there are two major problems to characterize n-MOSFETs. One is the threshold voltages of n-MOSFETs that cannot be monotonically scaled whereas p-MOSFETs can. The other is the bulk charge which is mainly affected in the velocity saturation region.

During our circuit design process, we found that the existing MOSFET compact models, including BSIM3, 4, 6, PSP, and HiSIM2, do not make sufficient attention to the forward body bias operations. In particular the simulated drain current of n-MOSFET by the circuit simulator is much lower than the measured value under the forward body bias condition.

The method first formulates depletion thickness (X_d) which is dominant to determine the threshold voltage (V_{TH}) using vertical and horizontal doping profiles. Next the bulk charge effect dependencies on reverse to forward body biases are analyzed and modeled. Then, these results are implemented into BSIM4 as an instance for simulating drain current from reverse to forward body bias ranges. Finally, the model is compared with measurement of 60 nm n-MOS transistors. The proposed model improved the forward body biased drain current simulation accuracies without sacrificing simulation accuracies of the null and reverse biased drain current in 60 nm n-MOSFET process devices.

4.2 Statistical modeling for Design for Manufacturability (DFM)

Increasing CMOS device variability has become one of the most acute problems facing the semiconductor manufacturing and design industries at, and beyond, the 45 nm technology generation. Most problematic of all is the statistical variability introduced by the discreteness of charge and granularity of matter in transistors with features already of molecular dimensions [27]. The variability in the transistor characteristics will be one of the major challenges for the CMOS industry in the next decades. The intrinsic parameter fluctuations (IPF) introduced by the discreteness of charge and matter start to dominate the variability of the scaled devices and become a major stumbling block to scaling and integration.

At the 65 nm technology node, the statistical variability already impedes the use of conventional (bulk) MOSFETs in SRAMs and prevents the scaling of the supply voltage and will force radical changes in the way circuits and systems are designed in the future. Therefore it is extremely important to

gain using simulations reliable early estimates for the magnitude of intrinsic parameter fluctuations in the next generation conventional and novel CMOS devices.

In this case for circuit simulations, model parameter extraction procedures and statistical algorithms for treating model parameters should be developed rather than new compact device models. An advanced method [28] to generate a statistical variability model is shown in Fig. 11.
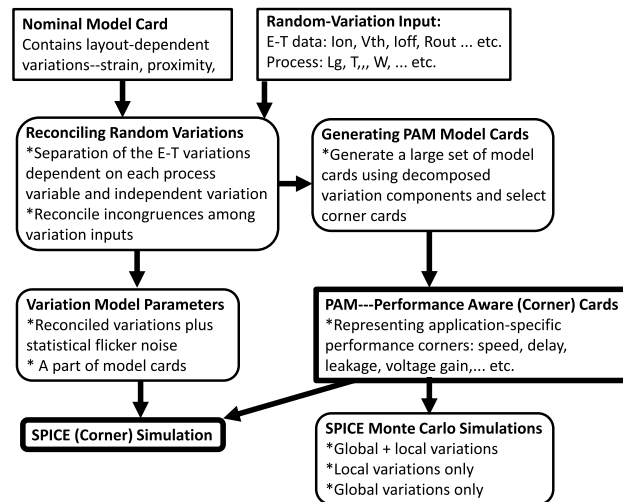
Fig. 11. A flow chart for statistical compact modeling of nano-scale CMOS variations.

Fig. 11 shows the advanced flow for performance aware modeling of device variation. The inputs to the variation modeling process are the nominal model card, the process electrical test (E-T) variations (V_{th}, l_{on}, l_{off}, R_{out}, etc.) and the process variations (L_g, T_{ox}, W, etc.). The nominal model card that is already extracted by using such as [8] already includes the layout-dependent variation (strain, well proximity effect, etc.).

Accuracy is improved by emphasizing electrical variation data and reconciling the process and electrical variation data. Performance Aware Model (PAM) supports corner ($\pm 1\sigma$ and $\pm 2\sigma$) simulation and Monte Carlo simulation. Furthermore, PAM supports application-specific corner cards, for example, for gain sensitive applications.

4.3 Reliability modeling for Design for Reliability (DFR)

Two transistors next to each other on the chip with exactly the same geometries and strain distributions may have characteristics from each end of a wide statistical distribution. In conjunction with statistical variability as described in Section 4.2, negative/positive bias temperature instability (NBTI/PBTI) and/or hot carrier degradation can result in acute statistical reliability problems. It already profoundly affects SRAM design, and in logic circuits causes statistical timing problems and is increasingly leading to hard digital faults. In both cases, statistical variability restricts supply voltage scaling, adding to power dissipation problems.

Although the reliability modeling has been researched and reported by any universities and manufacturers, many issues still remain to be solved. One of these issues is on noise degradations. For low frequency ranges, 1/f and thermal noise degradation affects oscillator circuits. For high frequencies, noise figure characteristics mainly caused by thermal noise degradation affects low noise amplifiers, mixers, and other circuit modules. Although a few papers [30, 31] were published so far, a practical noise degradation model has not yet been developed. We are currently in the process of researching the noise degradation modeling supported by STARC [32].

5   Conclusion

This paper reviews AMS circuit design in nano CMOS era; (i) digitally-assisted analog technology, and (ii) nano CMOS modeling technology for sophisticated circuit design. As an example of (1), our fully digital implementation of a TDC circuit with self-calibration is shown.

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