Fully Digital Calibration of Timing Mismatches in Interleaved ADC

Minghui Wu, Ru Yi, Koji Asami, Haruo Kobayashi, Atsuhiro Katayama and Kentaroh Katoh
Department of Electrical and Electronic Engineering, Gunma University
1-5-1 Tenjin-cho, Kiryu 376-8515, Japan k_haruo@el.gunma-u.ac.jp

This paper describes a method of reducing timing mismatches of interleaved ADC[1,2,3,4] by using autocorrelation among channel ADC outputs[3,4] and our proposed delay digital filter[2].

A time-interleaved ADC is an architecture that cycles through a set of sub-ADCs, such that the aggregate throughput is times the sample rate of the individual sub-ADCs [1]. However, the performance of interleaved ADCs is ultimately limited by mismatches among the channels. Gain, offset, and timing mismatches heavily impact the overall signal-to-(noise+distortion) ratio (SNDR), and the timing mismatch is the most difficult to calibrate because it does not easily lend itself to detection or correction.

The calibration of timing errors in interleaved ADCs consists of two steps, namely, detection and correction. Our proposed approach here is fully digital for the detection and correction (which is new). The autocorrelation of each channel output signal can serve as a measure of the timing mismatch[3,4]. The value of this autocorrelation R(Δt) is a function of the timing difference Δt between the sampling edges of the two ADCs, and is maximized when the timing difference is reduced to zero (Fig.1).

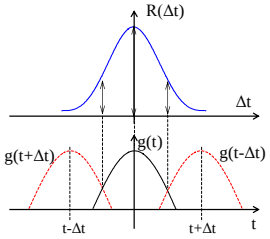

Fig. 1 Autocorrelation.

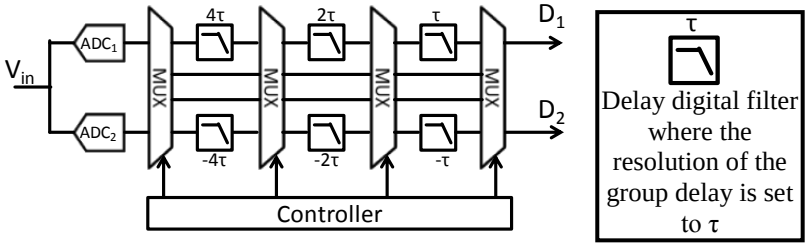

Fig. 2 Successive approximation calibration using delay digital filters.

Then we use the delay digital filter to correct the timing skew. The delay digital filter is proposed by our lab which the group delay can be set with arbitrary small time resolution, and has not necessarily odd or even symmetry coefficients [2]. Fig.2 shows successive approximation calibration using the delay digital filters.

We performed MATLAB® simulations to confirm the effectiveness of the proposed method in a 2-channels interleaved ADCs. Table.1 shows the simulation conditions. Fig.5 shows the powers spectrum without compensation and after compensated.

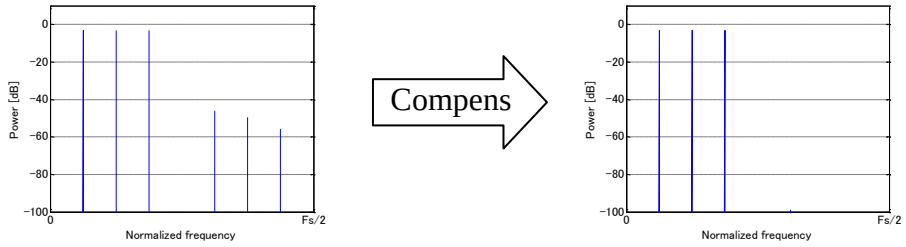

Fig.5 Signal Power Spectrum

Since the proposed approach is fully digital, it is reliable and suitable for fine CMOS implementation.

[1] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC System," IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications, vol.48, no.3, pp.261-271 (March 2001).

[2] K. Asami, H. Miyajima, T. Kurosawa, T. Tateiwa, H. Kobayashi, "Timing Skew Compensation Technique Using Digital Filter with Novel Linear Phase Condition," IEEE International Test Conference, Paper 11.3, Austin, TX (Nov. 2010).

[3] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit Time-Interleaved Fash ADC with Background Timing Skew Calibration," IEEE J. Solid-State Circuits, vol. 46, pp. 838-847 (Apr. 2011).

[4] B. Razavi, "Problem of Timing Mismatches in Time-Interleaved ADCs," IEEE Custom Integrated Circuits Conference, (Sept. 2012).