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Full Digital Compensation of Timing Mismatches in Interleaved ADC

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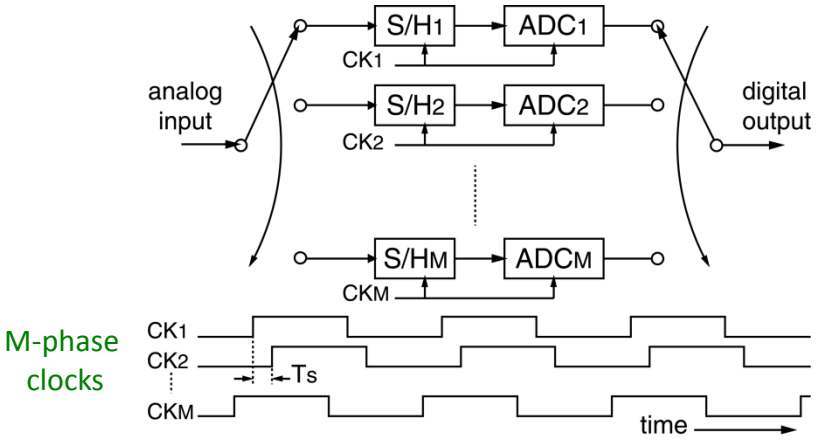
■ Interleaved ADC

A high sampling-rate ADC with M channel ADCs operating in a interleaved manner.

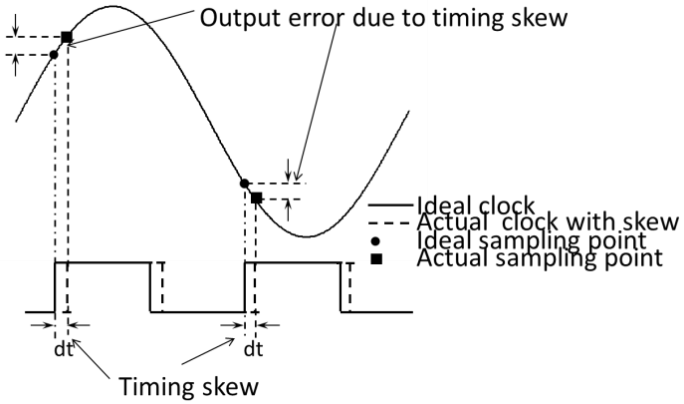


M channel ADCs = M times sampling rate

■ Timing Skew Problem

M-phase clocks

- ➡ timing skew dt
- ➡ cause ADC output error
- ➡ difficult to correct



■ Proposed Timing Skew Calibration Method

Skew Detection : Autocorrelation among channel ADC outputs

Correction : Proposed linear-phase delay digital filter

➡ Fully Digital

Stable, reliable, easy to design