DAC Architecture with Fibonacci Sequence Weighted Current Sources

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We describe here a current-steering digital-to-analog converter (DAC) architecture using Fibonacci sequence to realize high accuracy. We introduce three methods to improve performance of the current-steering DAC with modest redundancy utilizing Fibonacci sequence properties.

Fibonacci sequence is defined by following recurrence relation[1].

$$F_n = F_{n-1} + F_{n-2} \qquad (1)$$

Fibonacci numbers are expressed by following.

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610...

Fibonacci sequence have many interesting properties and we use them for DAC design.

Usually current sources of the current-steering DAC are weighted with binary or unary. The binary-weighted current-steering DAC has no redundancy and hence it can be realized with simple circuit and operate fast. However, its glitch energy is large, and also it suffers from current source mismatches and its monotonicity characteristics is not guaranteed. On the other hand, the unary-weighted (or segmented) current-steering DAC has a lot of redundancy with large circuits but its glitch energy is small, and also its monotonicity characterisitics is guaranteed. Hence in many cases, the combination of the binary and unary-weighted DAC architecture is used.

We consider here a different DAC architecture as a *lateral thinking*. Fig.1 shows an example of our current-steeering DAC where current sources are weighted with Fibobnacci sequence numbers. A decoder circuit from binary to switches P1, ..., P12 can be implemented with a look-up table (LUT).

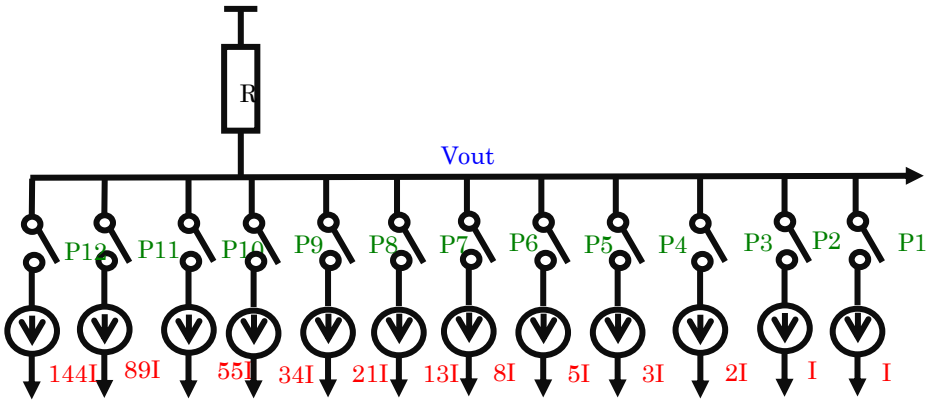

Fig.1 Current-steeering DAC weighted with Fibobnacci sequence numbers.

There can be mismatches among current sources which cause DAC characteristics nonlinearities and degrade spurious free dynamic range (SFDR). We propose here three methods to compensate for the mismatch effects in the Fibobnacci sequence weighted current-steering DAC (Fig.1).

(1) **Current Source Calibration:** Using the property of eq.(1), the n-th current source I_n is calibrated so that $I_n = I_{n-1} + I_{n-2}$ by adjusting the current source I_n (analog method), or with a small additional DAC for calibration (digital method).

(2) **Current Source Selection:** Due to some redundancy, there can be several combinations of ON switches for one digital input. For example, for digital input 9, corresponding ON switchies are (P6, P1), (P6, P2), (P5, P4,P1),(P5,P4,P2) or (P5, P3, P2, P1) . We select one of them which cancels the mimatches among the corresponding current sources and obtains better linearity.

(3) **Dyamic Matching:** Selection of the corresponding ON switches for a digital input are altered sequentially or randomly so that mismatch effects among current soureces are spread in frequency domain and DAC SFDR charactersistics is improved.

We have performed Matlab simulations and a part of the effectiveness is verified.

[1]Alfred S.Posamentier, Ingmar Lehmann, Syunsuke Matsuura: *Husigina suuretsu Fibonacci no himitsu* [The Fabulous FIBONACCI Numbers], NikkeiBP Publisher (Aug.2010)