Phase Noise Measurement with Delta-Sigma TDC

Yusuke Osawa[1)], Daiki Hirabayashi[1)], Naohiro Harigai[1)], Haruo Kobayashi[1)], Osamu Kobayashi[2)], Kiichi Niitsu[3)], Takahiro J. Yamaguchi[1)], Nobukazu Takai[1)]

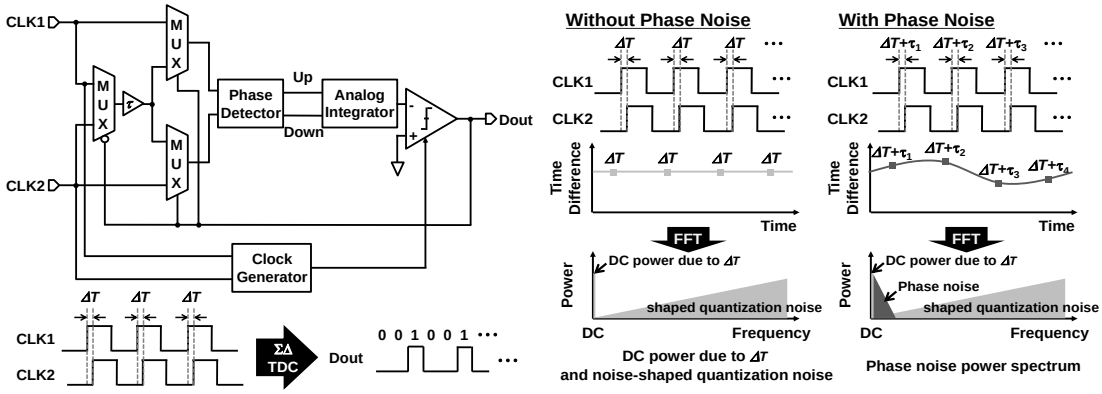
[1)]Division of Electronics and Informatics, Gunma University
1-5-1 Tenjin-cho, Kiryu 376-8515, Japan
t13801416@gunma-u.ac.jp

[2)]Semiconductor Technology Academic Research Center (STARC), Yokohama 222-0033 Japan

[3)]Graduate School of Engineering, Nagoya University, Nagoya 464-8603 Japan

This paper describes a phase noise measurement technique for a clock using a delta-sigma time-to-digital converter (TDC) and shows its simulation results with Matlab and Spectre. The proposed technique can be implemented with relatively small circuitry, and its time resolution can be finer with longer measurement time. High performance spectrum analyzers with long measurement time (about 10s order due to average of several-time phase measurement results), which are very costly, would not be needed for phase noise measurement with the proposed technique.

Fig.1 shows a block diagram of a delta-sigma TDC and Fig.2 shows the proposed phase noise measurement principle using the delta-sigma TDC; the phase noise frequency characteristics from the carrier (clock) frequency can be obtained by FFT of the TDC output. Note that e.g., a vernier-type TDC can acquire a one-shot timing but the time resolution of the delta-sigma TDC is limited. However its time resolution can be very fine (e.g. finer than 0.1ps) by increasing the measurement time, though it can apply only for *repetitive* clock timing.



(a) (b)

Fig. 1. (a) Block diagram of Delta-Sigma TDC.

(b) Principle of the proposed phase noise measurement with a Delta-Sigma TDC. CLK1 is a clock under test (CUT) with phase noise and CLK2 is a reference clock without phase noise.

Our Matlab as well as Spectre simulations used the input clock of 1 MHz with a 10 kHz sine wave as phase fluctuation, and we observed that the phase fluctuation spectrum at 10 kHz from TDC output power spectrum obtained by FFT (Fig.3). The amount of phase fluctuation obtained by simulation agreed with the above theoretical calculation. Finally we note that a multi-bit delta-sigma TDC with linearization techniques can further reduce the phase noise measurement time[1].

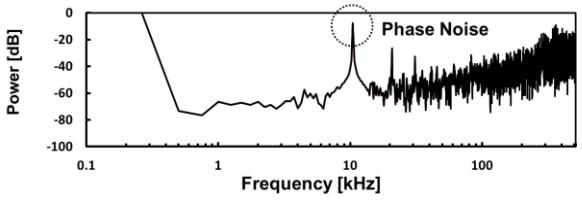


Fig.2 Matlab simulation results for power spectrum of TDC output signal with phase noise at 10kHz

Reference

[1]S. Uemori, M. Ishii, H. Kobayashi, et. al., "Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement", IEEE International Mixed-Signal, Sensors and Systems Test Workshop, pp.67-72, Taipei, Taiwan (May 2012). [2]D. Hirabayashi, Y. Osawa, N. Harigai, H. Kobayashi, et. al., "Phase Noise Measurement with Sigma-Delta TDC", IEEE International Test Conference, Poster Session, Poster No. 3, Anaheim, CA (Sept. 2013).