Noise-Shaping Cyclic ADC Architecture

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This paper presents an ADC architecture comprising a pipelined cyclic ADC and a continuous-time delta-sigma ADC; it provides high resolution at medium speed, with small power requirements. Fig.1 shows the configuration of our noise-shaping cyclic ADC and Fig.2 shows its timing chart. It is reconfigurable for various combinations of speed, precision, and power consumption.

The ΔΣ ADC accumulates the quantization error of the cyclic ADC, and the accumulated quantization error is compared to the reference voltage V_{1LSB} to check whether it is over 1LSB analog voltage. When it is over 1LSB analog voltage, the ΔΣ ADC outputs 1 and the accumulated error is subtracted by 1LSB analog voltage; otherwise it outputs 0.

Fig.3 shows simulation results of the noise-shaping cyclic ADC output power spectrum. We see that low frequency noise is decreased whereas high-frequency noise increased; in other words noise shaping is realized.

The whole ADC outputs are combination of the digital outputs of the cyclic ADC and the delta-sigma ADC so as to achieve high resolution. Fig.4 shows signal-to-quantization-noise-and-distortion (SQNDR) vs. over-sampling ratio (OSR); we see that the SQNDR of the noise-shaping cyclic ADC is better than that of the cyclic ADC.

The delta-sigma ADC can be implemented simply with continuous-time analog circuitry. We describe the overall ADC architecture and operation, show simulation results, and describe features such as its potential for reconfiguration.

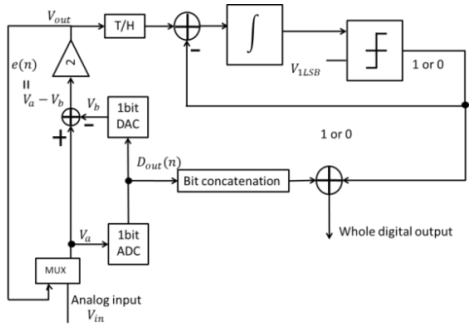

Fig.1 Proposed noise-shaping cyclic ADC configuration.

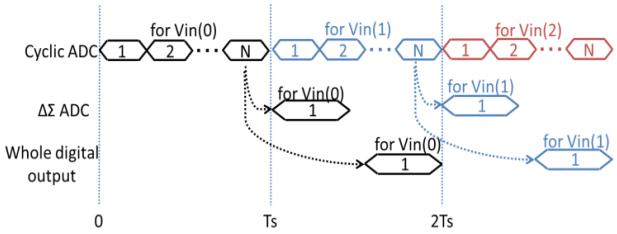

Fig.2 Operation of the proposed noise-shaping cyclic ADC.

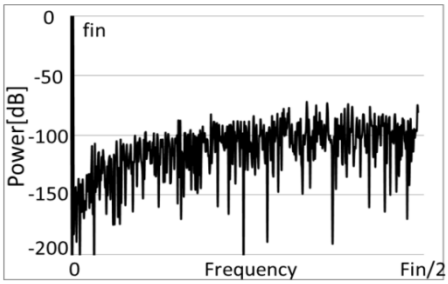

Fig.3 ADC output power spectrum of the noise-shaping cyclic ADC

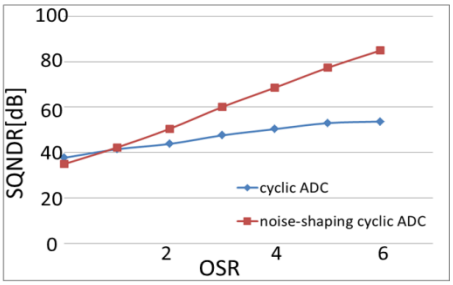

Fig.4 SQNDR comparison of a 6-bit cyclic ADC and a noise-shaping cyclic ADC.

[1] F. Maloberti, *Data Converters*, Springer (2007).
[2] R. J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, Springer (2010).
[3] R. Schreier, G. C. Temes, *Understanding Delta-Sigma Data Converters*, Wiley (2005).