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Noise-Shaping Cyclic ADC Architecture

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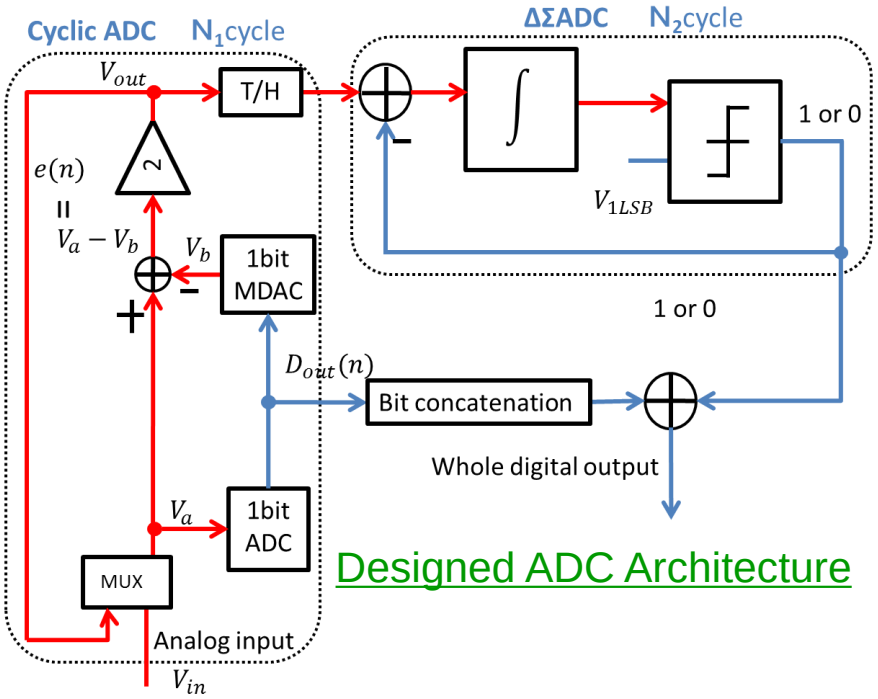
Research Objective

Development of well-balanced, flexible analog-to-digital converter (ADC) architecture

High resolution, medium speed, low power with simple circuitry



Designed ADC Architecture

Our Approach

Pipeline of cyclic ADC & ΔΣ ADC

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Utilization of both advantages

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Reconfigurable for different combinations of speed, resolution & power

ΔΣ ADC Multiple-cycle