ADC/DAC Redundancy Design Using Fibonacci Sequence

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We describe redundancy design of ADCs/DACs and their calibration method using Fibonacci sequence to realize accurate and/or high-speed conversion. We introduce theoretical basis to improve performance of SAR ADCs with time redundancy and current-steering DACs with space redundancy utilizing Fibonacci sequence properties.

Fibonacci sequence is defined by following recurrence relation[1].

$F_n = F_{n-1} + F_{n-2}$

And Fibonacci numbers are expressed by following.

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610...

Fibonacci sequence have many interesting properties and we use them for ADC/DAC redundancy design.

SAR ADC is one of Analog-to-Digital Converter that compares analog input voltage with reference voltage and gets digital output from result of comparison. To enable digital calibration we increase number of comparison steps using time redundancy and alter reference voltage value[2]. Fibonacci sequence is used to determine that value. Generally, the value is detemined freely by SAR ADCs designer, but we have noticed that we can get this value by applying properties of Fibonacci sequence such as the closest terms ratio called "golden ratio" and realization of all terms with integers. In addition, digital calibration enable resulting high-speed conversion. Thus we consider to improve reliabillity and speed of SAR ADCs by using moderate redundancy.

We also consider applying the theory to current-steering Digital-to-Analog Converters (DACs). In current-steering DACs, we increase number of current sources using space redundancy and alter electrical current value of current sources to Fibonacci-number weighted. This means one of output level is expressed by several digital values. So we can select a combination of current sources having the best linearity and random selecting the combination realize imploving Spurious Free Dynamic Range(SFDR). Furthermore we use Fibonacci sequence property that the sum of closest terms is next term to enable self-calibration.

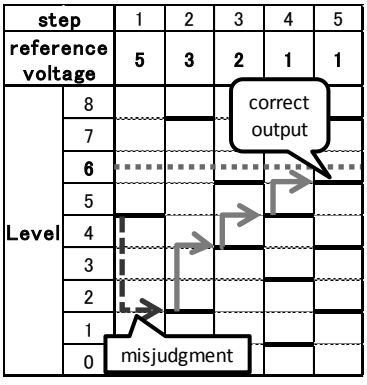

Fig. 1 Operation of a redundant search algorithm of a 3-bit SAR ADC with 5 steps in case of error judgment.

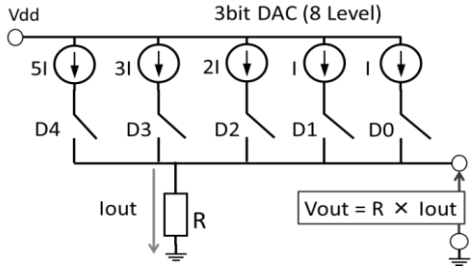

Fig. 2 A Fibonacci-number weighted current-steering DAC.

[1]Alfred S.Posamentier, Ingmar Lehmann, Syunsuke Matsuura: "*Husigina suuretsu fibonacci no himitsu*[The Fabulous FIBONACCI Numbers]", NikkeiBP, (Aug.2010)
[2]T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, H. San, T. Matsuura, A. Abe, K. Yagi, T. Mori : "SAR ADC Algorithm with Redundancy and Digital Error Correction", IEICE Trans. Fundamentals, vol.E93-A, no.2, (Feb. 2010).