

P77 ADC/DAC Redundancy Design Using Fibonacci Sequence

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New Idea Learning from the Past

Research Background and Objective

Automotive Electronics are more and more gathering attention

ADC/DAC are required better performance

- high-resolution
- high-speed
- high-accuracy
- high-reliability
- low-cost
- low-power
- small-chip

ADC : Analog-to-Digital Converter
 DAC : Digital-to-Analog Converter

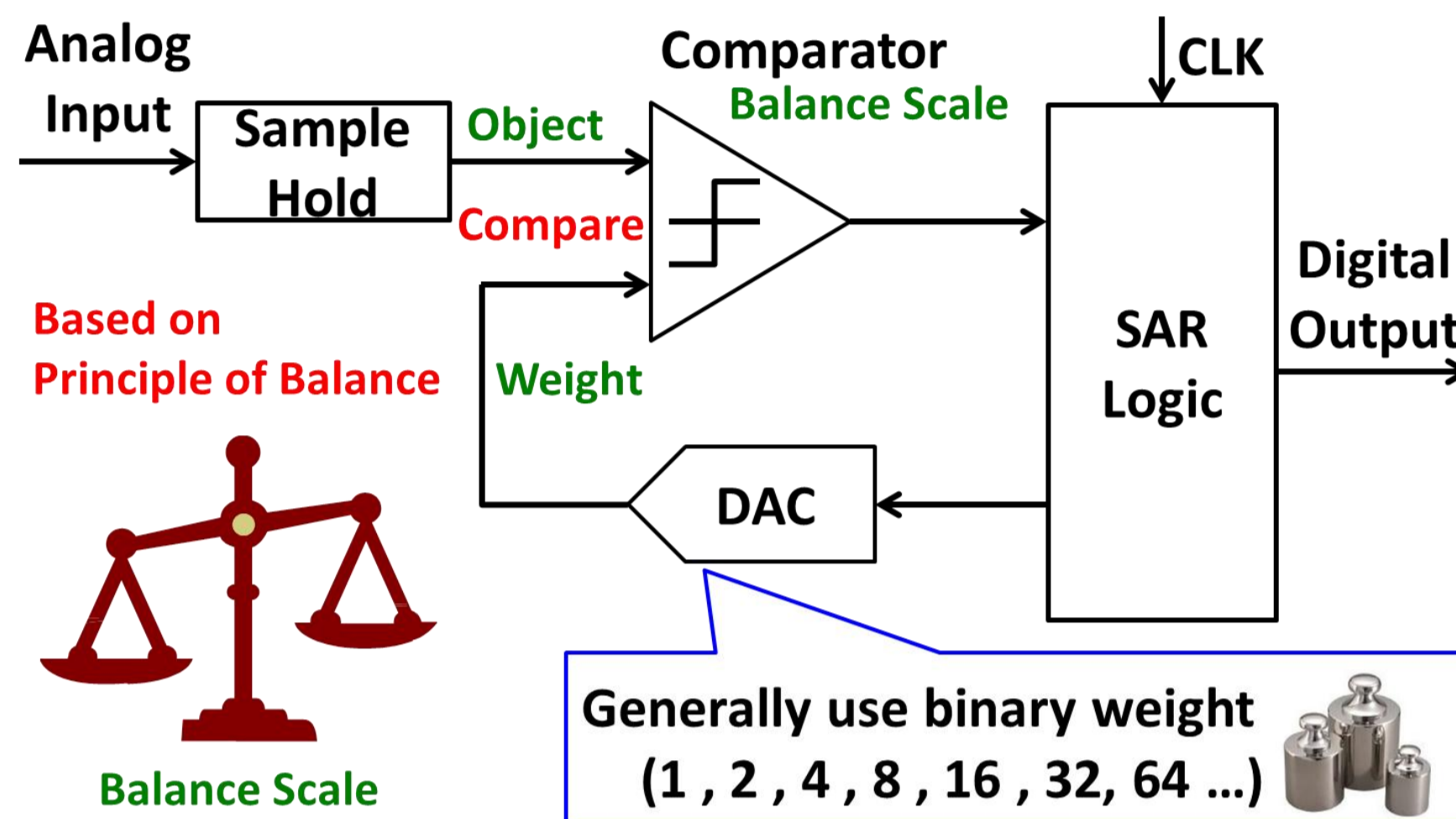
Objective

Design high-reliability ADC/DAC by using redundancy theory !



SAR ADC

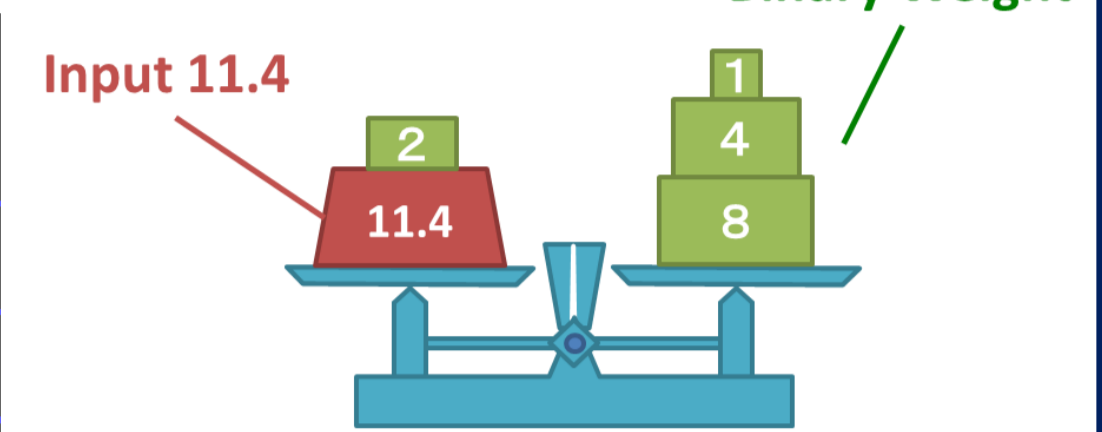
SAR ADC : Successive Approximation Register type A-D Converter



Binary Search SAR ADC Operation

Comparator repeats comparison

Step	Reference Voltage	1	2	3	4
15	8				
14	4				
13	2				
12	1				
11	0.5				
10	0.25				
9	0.125				
8	0.0625				
7	0.03125				
6	0.015625				
5	0.0078125				
4	0.00390625				
3	0.001953125				
2	0.0009765625				
1	0.00048828125				
0	0	1	0	1	1



$$D_{out} = 1011$$

$$8 + 4 - 2 + 1 + 0.5 - 0.5 = 11$$

One-to-one correspond between Decimal and Binary codes

1 Misjudgment leads to incorrect output

Proposed Redundancy Design using Fibonacci Sequence

SAR ADC Redundancy Design

Redundancy : Surplus , Extra

Apply to SAR ADC

Using Time Redundancy

- ◆ Increase comparison steps
- ◆ Change reference voltage values

Increase number of output expressions
 $(11)_{10} = (110000)_2, (101100)_2, (101010)_2$

Enable digital error correction

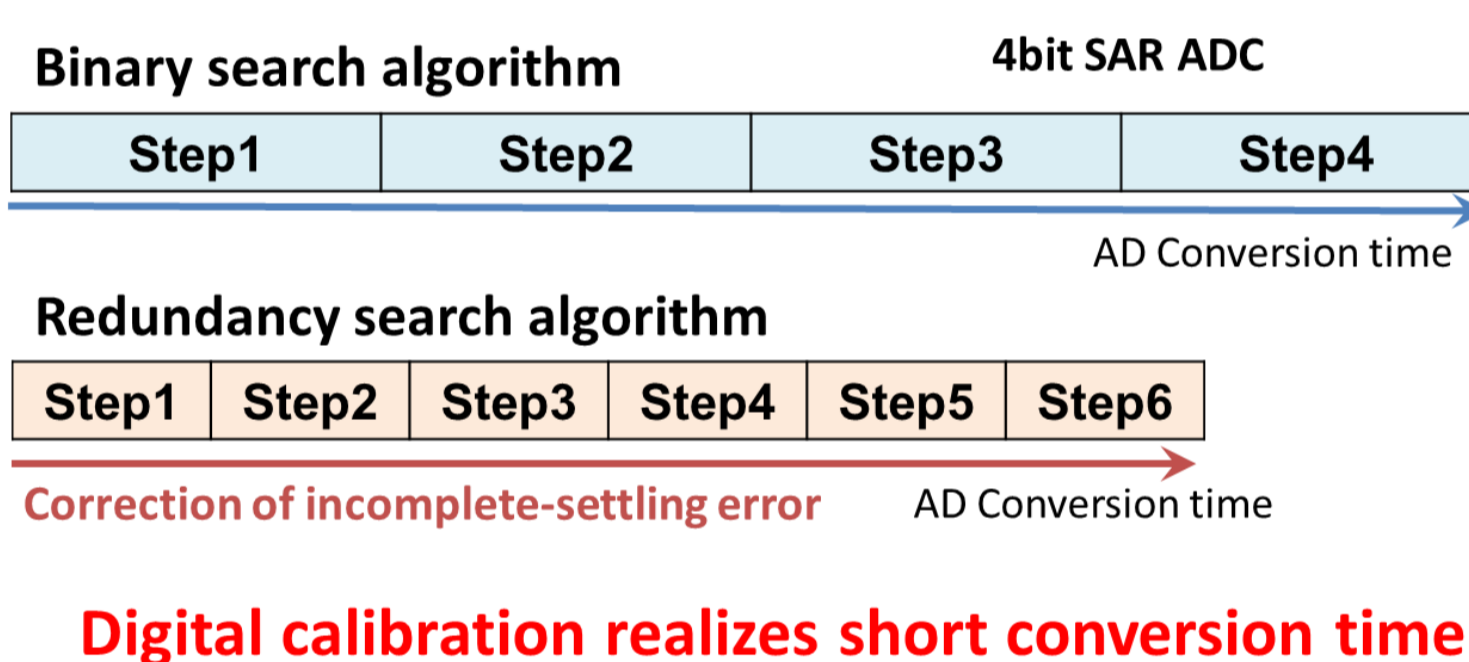
Step	Reference Voltage	1	2	3	4	5	6
15	8						
14	5						
13	3						
12	2						
11	1						
10	1						
9							
8							
7							
6							
5							
4							
3							
2							
1							
0							

Redundancy Design Advantages

◆ High-reliability

Later steps can compensate for misjudgment of previous steps
 Get correct output

◆ High-speed



Fibonacci Sequence

Definition (n=0,1,2,3...)

$$F_{n+2} = F_n + F_{n+1}$$

$$F_0 = 0, F_1 = 1$$

Example of numbers (Fibonacci number)

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144...

Property

➢ Closest terms ratio converges to "Golden Ratio"

$$\lim_{n \rightarrow \infty} \frac{F_n}{F_{n-1}} = 1.61803398874 \dots$$



Advantages of Fibonacci sequence usage

Weight of Redundancy design SAR ADCs

– Should be Sub-binary weight and Integer

◆ Conventional method

– Determined freely by SAR ADCs designer

• Inefficient

– Radix of square root of two (= 1.4...)

• Too much redundancy

◆ Proposed method (Fibonacci method)

Get radix of 1.6 weight by Integer terms

Moderate Redundancy

Method of getting Fibonacci weights

Three proposed methods

1) Fibonacci number method

• Realize radix of 1.6 weight by using Fibonacci number

2) Fibonacci recurrence relation method

• Using Fibonacci recurrence relation

3) Fibonacci number and recurrence relation method

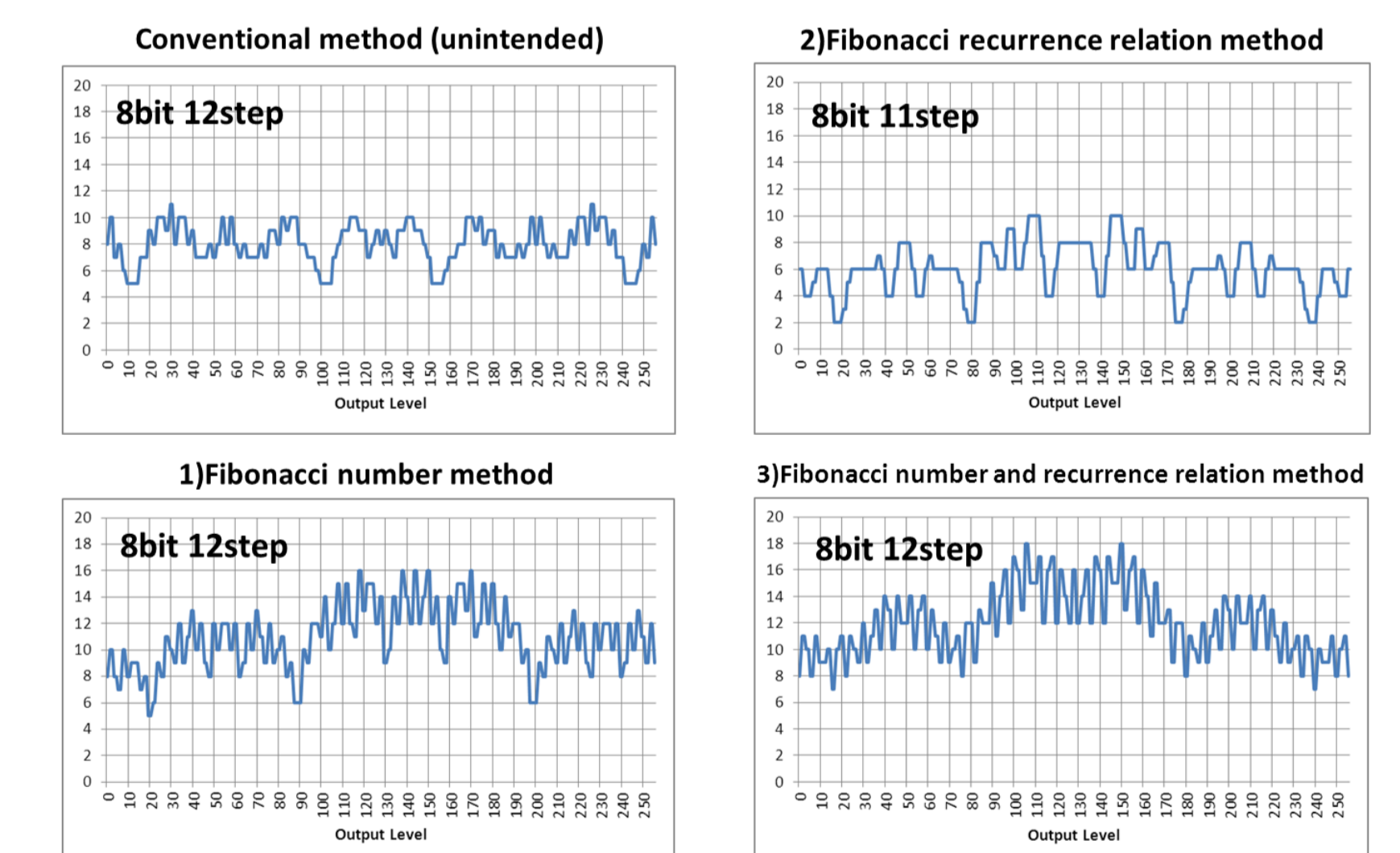
• Using method 1 and method 2

Example. 8bit SAR ADC weight design

Method	Steps	Weights
Conventional	12step	1, 2, 3, 5, 9, 16, 26, 45, 72, 100, 115, 128
method1	12step	1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144
method2	11step	1, 1, 2, 4, 7, 11, 19, 30, 49, 79, 128
method3	12step	1, 1, 2, 3, 5, 8, 11, 19, 30, 49, 79, 128

Number of Combinations

Many combinations at all output Levels

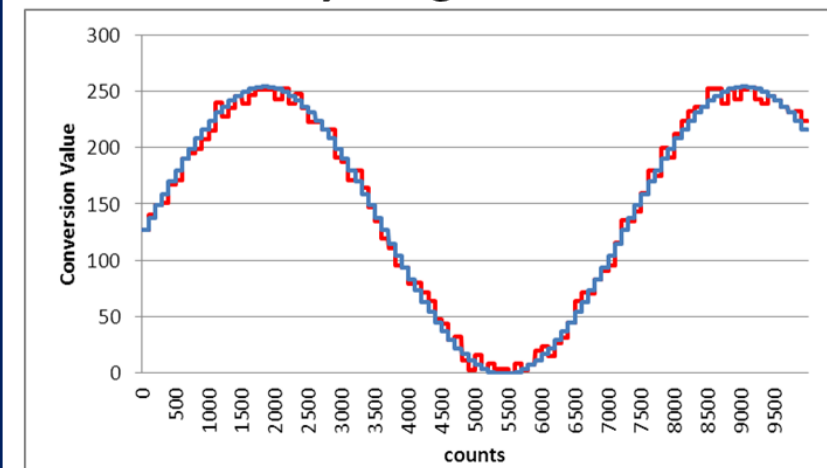


Simulation Result

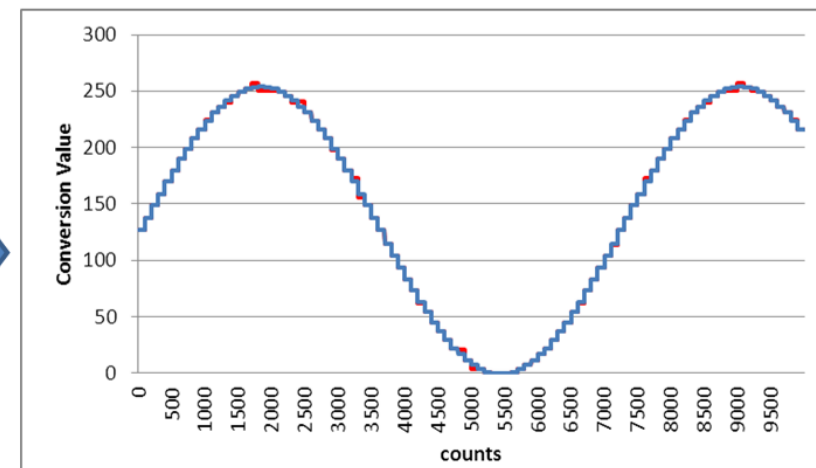
8bit SAR ADC Simulation Condition

Use C programming language
 Input : FS sine-wave
 Number of Conversion : 100 times
 Comparator in 1step to 6step occur misjudgment with 40% possibility at difference between input voltage and reference voltage is 10 or less

No redundancy design



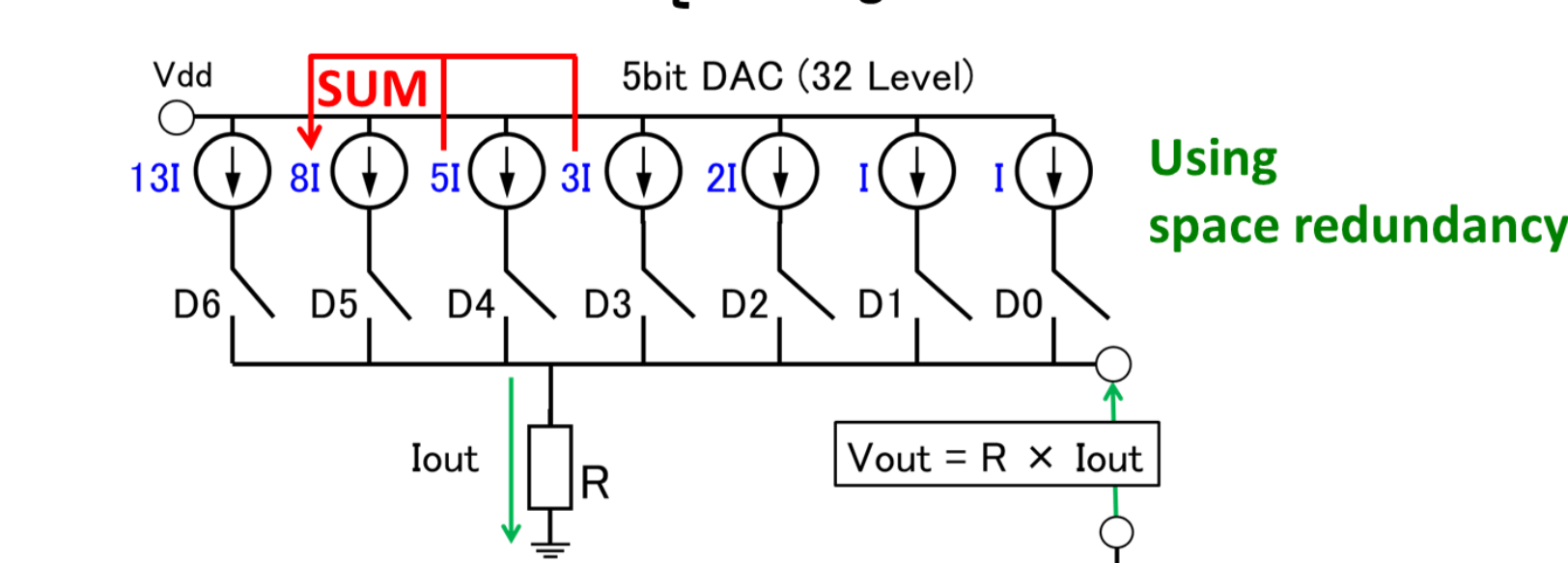
Using Fibonacci number method



Compensate 89.0% error !

Apply to Current-Steering DAC

Current-steering DAC { Increase number of current sources
 Change current value



- ◆ Improving Linearity
- ◆ Improving SFDR
- ◆ Reducing Glitch
- ◆ Self-Calibration

summary

Conclusion

- ◆ Showed effectiveness of ADC/DAC redundancy design
- ◆ Obtained moderate redundancy using Fibonacci sequence

◆ Future works

- Applying of Tribonacci sequence
- Applying of "Golden section search" to SAR ADC

References

- [1] Alfred S.Posamentier, Ingmar Lehmann, Syunsuke Matsuura: "Husigina suuretsu fibonacci no himitsu[The Fabulous FIBONACCI Numbers]", NikkeiBP, (Aug.2010)
- [2] T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, H. San, T. Matsuura, A. Abe, K. Yagi, T. Mori: "SAR ADC Algorithm with Redundancy and Digital Error Correction", IEICE Trans. Fundamentals, vol.E93-A, no.2, (Feb. 2010).