Implementation of Time-to-Digital Converter with Self-Calibration

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This paper describes the architecture and principle of time-to-digital converters (TDC) with self-calibration for high-speed I/O interface circuit test applications. We have implemented the proposed TDC using a programmable system-on-chip (PSoC), and we show here that the proposed TDC can realize timing measurement with good linearity.

A TDC measures the time interval between two edges, and time resolution of several picoseconds can be achieved when the TDC is implemented with an advanced CMOS process. The TDC will play an increasingly important role in the nano-CMOS era, because it is well suited to implementation with fine digital CMOS processes; a TDC consists mostly of digital circuitry. Although the resolution of TDC can be high, its linearity is lower. Therefore, self-calibration technique for high linearity is required. We have proposed the stochastic self-calibration technique of TDC using two ring oscillators[1,2] . Since this calibration technique is fully digital, it can be easily implemented on SoC.

Figure 1 shows architecture of the proposed TDC with self-calibration. When CTRL = 0, two ring oscillators operate asynchronously, and we obtain histogram of the output by the histogram engine. Note that it is uncorrelated the frequency of two ring oscillators. There is a direct correlation between the obtained histogram and variation of delay values (Fig. 2). When CTRL = 1, the proposed TDC performs a normal timing edge measurement operation. Then, the linearity of the TDC is improved by calibrating the output from the information of the obtained histogram.

We have implemented the proposed TDC using a PSoC (Fig. 3). Measurements results are shown in Fig. 4 and their integral non-linearity (INL) are shown in Fig. 5; we see that our proposed method improves the TDC linearity.

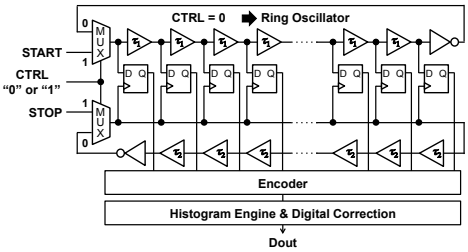

Fig. 1. Architecture of the proposed TDC.

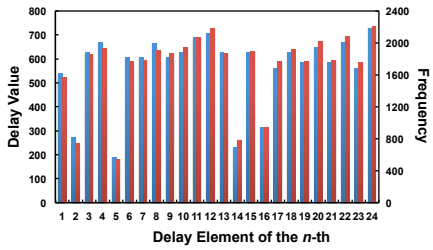

Fig. 2. Histogram and delay values of proposed TDC.

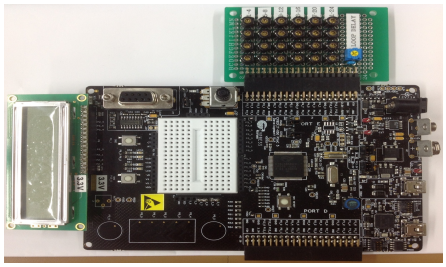

Fig. 3. Photo of PSoC which implements the proposed TDC.

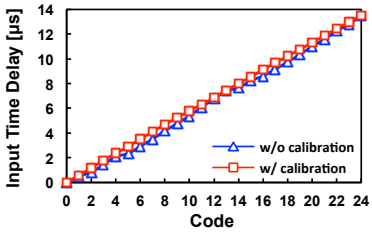

Fig. 4. Measurement results of the TDC with/without calibration.

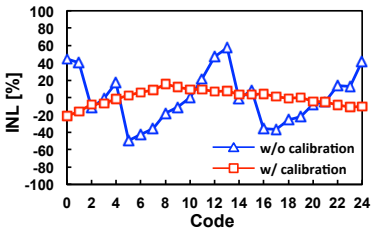

Fig. 5. INL of the TDC with/without calibration.

[1] S. Ito, S. Nishimura, H. Kobayashi, S. Uemori, Y. Tan, N. Takai, T. Yamaguchi, K. Niitsu, "Stochastic TDC Architecture with Self-Calibration," IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia (Dec. 2010).

[2] K. Katoh, et. al., "An Analysis of Stochastic Self-Calibration of TDC Using Two Ring Oscillators", IEEE 22nd Asian Test Symposium, Yilan, Taiwan (Nov. 2013).