P78

Implementation of Time-to-Digital Converter with Self-Calibration

Daiki Hirabayashi†, Takeshi Chujo†, Haruo Kobayashi†, Kentaroh Katoh††, Koshi Sato‡

† Electronic Engineering Department, Gunma University, Kiryu 376-8515 Japan email: k_haruo@el.gunma-u.ac.jp

†† Tsuruoka National College of Technology, Tsuruoka 997-8511 Japan

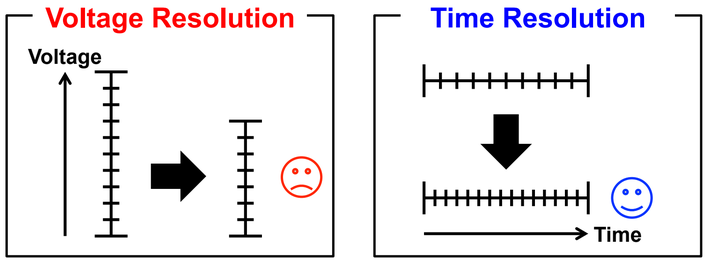
‡ Hikari Science, Fukaya 366-0801 Japan

Kobayashi Laboratory

Nano VLSI Era Circuit

Background

Nano-CMOS VLSI ➡ Low Voltage Power Supply, Fast Switching



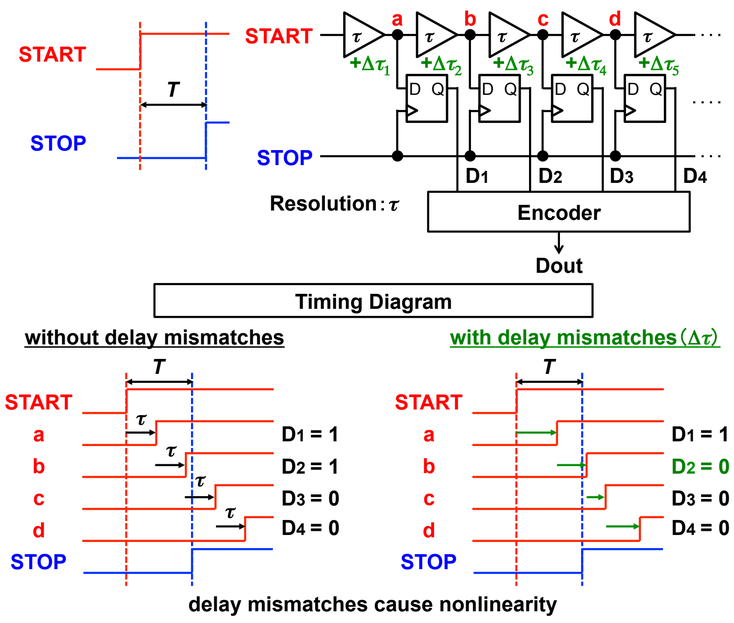
TDC converts input time difference into a digital value.

TDC is a key component of time domain analog circuits in nano-CMOS VLSI.

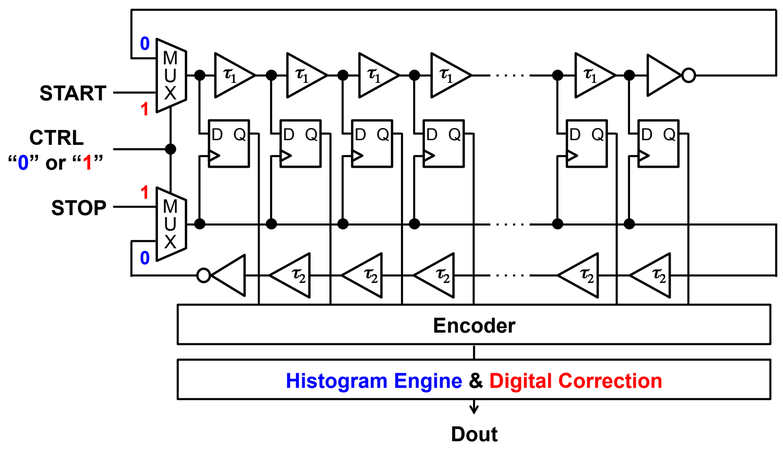
(e.g. Sensor Interface Circuit, All-Digital PLL)

High Quality TDC is required.

Conventional TDC



Proposed TDC



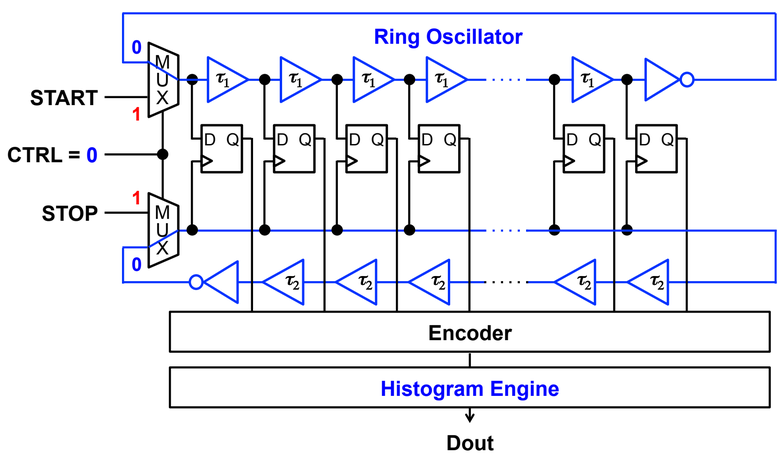
τ_1 and τ_2 are uncorrelated

CTRL = 0 ➡ Test Mode CTRL = 1 ➡ Normal Mode

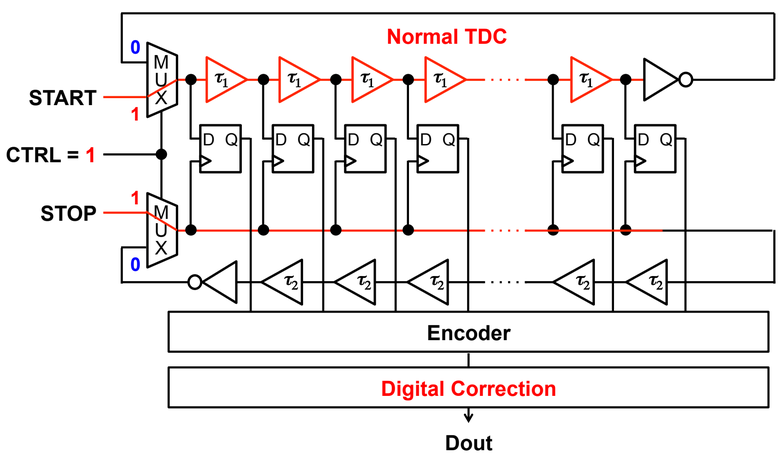
Rearch Goal : Full digital implementation of very linear TDC

Proposed TDC

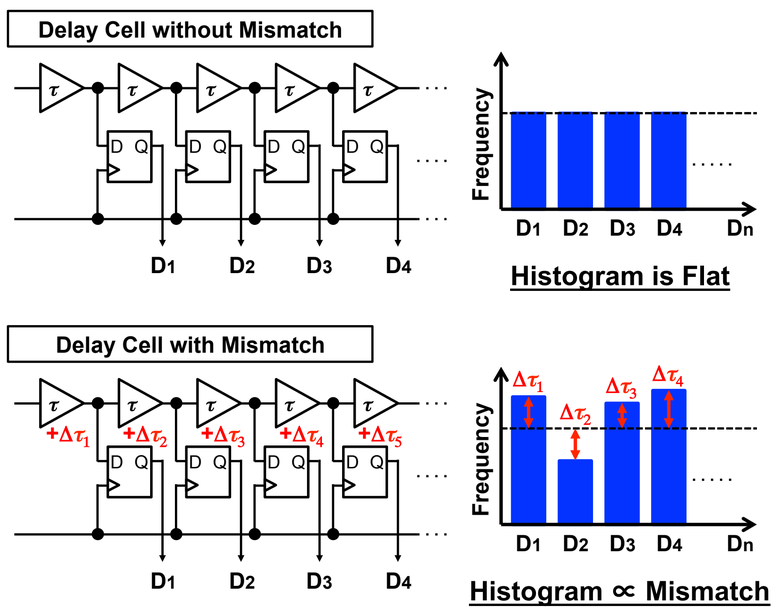
Test Mode



Normal Mode

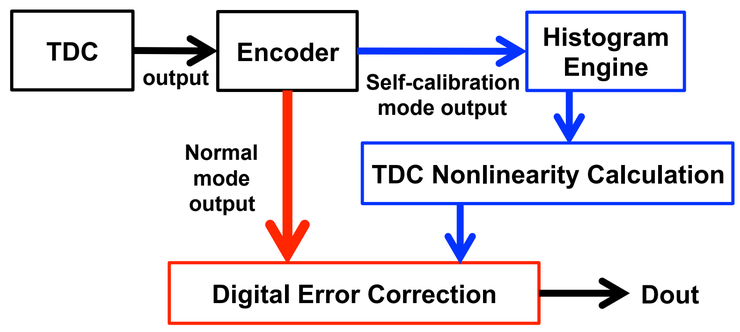


Histogram



Self-Calibration

Flow Chart of Self-Calibration



Digital Error Correction

$$Dout(i) = \frac{\sum_{i=1}^{N} Pin(i)}{\sum_{i=1}^{FS} Pin(i)} \times Full\ Scale$$

Dout(i) : output after calibration of i-th bit

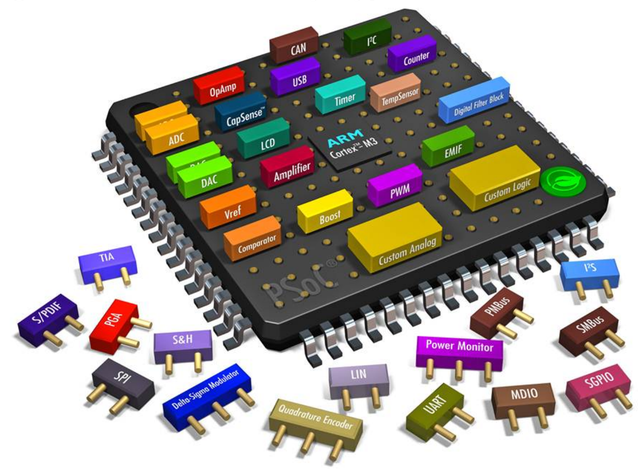
Pin(i) : histogram of i-th delay

Proposed TDC
- can be self-calibrated with a fully digital. (Analog calibration is not required.)
- can be realized with FPGA. (Full Custom LSI is not required. Design is easy and short time.)
- implemented with PSoC and verified by actual measurement.

Implementation

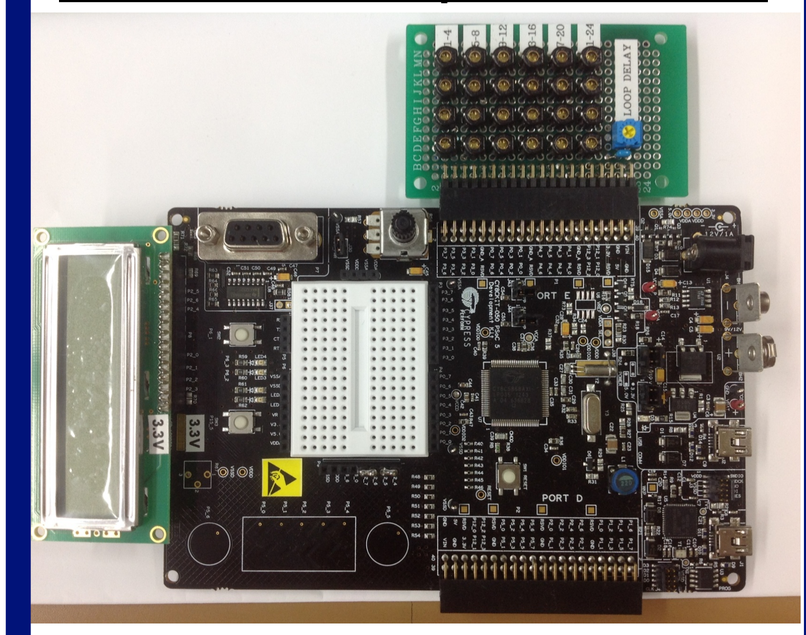
Programmable System-on-Chip

PSoC (Programmable System-on-Chip) is a family of integrated circuits made by Cypress Semiconductor.



PSoC include a CPU and mixed-signal arrays of configurable integrated analog and digital peripherals.

Photo of PSoC implemented TDC

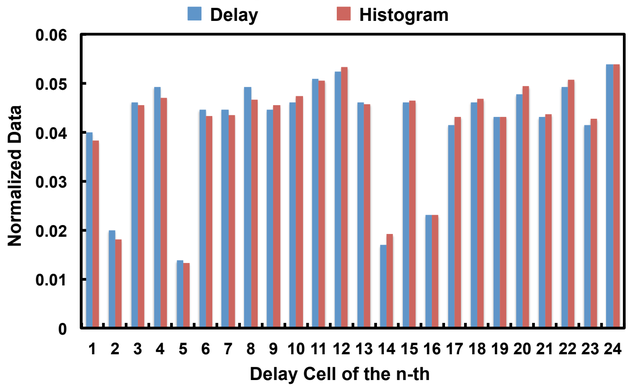


Measurement Result

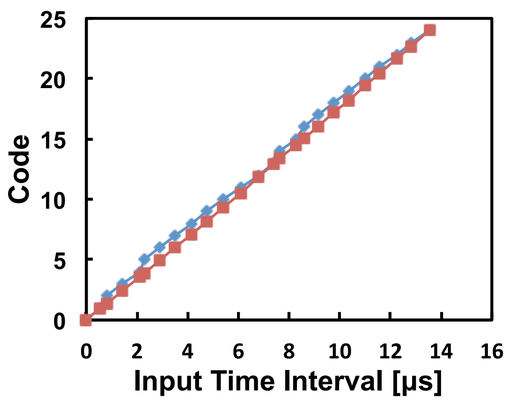
Measurement Conditions

Delay (τ_1)	187 ns ~ 729 ns
The number of delay cells	24
The number of histogram	40934
Frequency (Normal Mode)	48 MHz

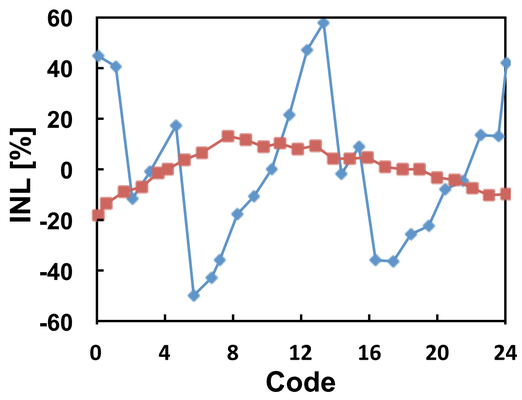
Correlation of delay and number of measurements



TDC output with/without calibration



Integral Non Linearity (INL)



without calibration with calibration

Nonlinearity : 60% ➡ 17%

Nonlinearity reduction to 1/4

Conclusion

- **Proposal of TDC**
  - Very linear
  - Full digital calibration
  - Suitable for nano-CMOS implementation
- **Implementation with PSoC**
- **Measurement results**
  - ➡ Nonlinearity reduction to 1/4

High Quality TDC