Multi-bit Delta-Sigma TDC for Timing Measurement

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This paper describes the scheme of improving lineality for a multi-bit ΣΔ time-to-digital converter (Fig.1). The data-weighted-averaging (DWA) technique[1] is simple and effective for small variation among delay cells. However, the delay cell variation may be relatively large, and there only DWA is not enough. We propose here the delay-cell sorting algorithms and their combination with DWA algorithm. Then we show how effective they are for large variation using simulation.

Note that the value of k-th delay cell τ_k can be measured with the ring oscillator configuration (Fig.1). We can measure the order from the smallest to the largest delay cell values with a digital method[2].

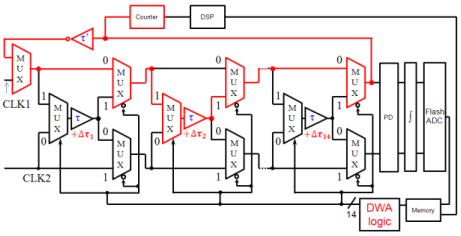

Fig.1 Circuit config of our proposed method
(Red line shows the case that $\tau + \Delta\tau_2$ is measured)

First we investigate the switching sequence post adjustment (SSPA) algorithm[3] for delay cell sorting. We propose here a 2-step SSPA algorithm; their combinations are done so that each 2-combined cell delay value is close to each other as much as possible (Fig.2).

After the sorting, we apply the DWA algorithm (Fig.3).

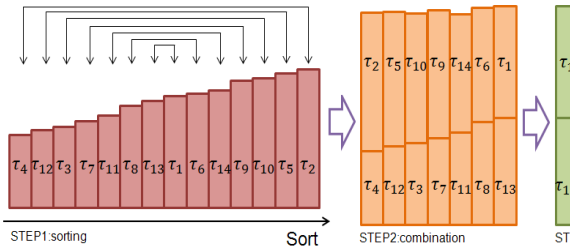

Fig.2 Step 1: Delay cell sorting.
Step 2: 2-delay-cell combination.
Step 3: Combined 2-delay-cell sorting.
Step 4: Applying DWA algorithm

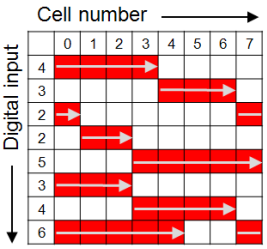

Fig.3 DWA operation.

We have performed Matlab simulation for the 3-bit ΣΔ TDC in several variation cases (their standard deviation is ~10%) and compared its linearity with or without the sorting. In most cases the avegrage linearity is improved with our sorting algorithms; Fig.4 shows the simulation results with or without sorting algorithm (without DWA). Fig.5 shows simulated linearity for possible combinations of sorting algorithms 1, 2 and DWA in 5 cases of delay cell variations. We see that the sorting algorithms are effective though the circuit becomes a little bit complicated. Fig.6 shows the simulated linearity for possible combinations of sorting algorithms 1, 2 and DWA with respect to the number of TDC output data. We see that as the number increases, the linearity is improved.

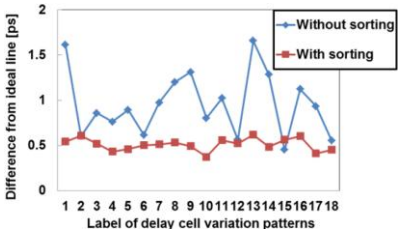

Fig.4. Averaged (rms) integral nonlinearity with or without sorting algorithm 2 in 18 cases of delay cell variations.

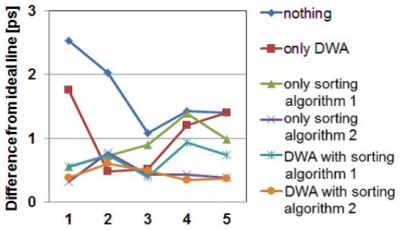

Fig.5 Simulated TDC INL (rms) for combinations of sorting algorithms 1, 2 and DWA in 5 cases of delay cell variations (number of TDC outputs is 1000).

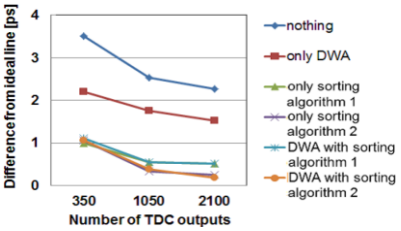

Fig.6 Simulated TDC INL (rms) for combinations of sorting algorithms 1, 2 and DWA with respect to the number of TDC output data.

[1] S. Uemori, M. Ishii, H. Kobayashi, et. al., "Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement", IEEE International Mixed-Signals, Sensors, and Systems Test Workshop, Taipei, Taiwan (May. 2012).
[2] S. Uemori, M. Ishii, H. Kobayashi, et. al., "Multi-bit Sigma-Delta TDC Architecture with Self-Calibration ", IEEE Asia Pacific Conference on Circuits and Systems, Kaohsiung, Taiwan (Dec. 2012) .
[3] T. Chen, G.Gielen, " A 14-bit 200-MHz Current-Steering DAC with Switching-Sequence Post-Adjustment Calibration", IEEE Journal of Solid-State Circuits, vol. 42, no. 11, pp. 2386-2394 (Nov. 2007).