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Multi-bit Delta-Sigma TDC for Timing Measurement

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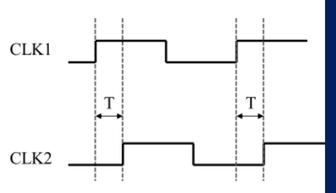
Background

Research Objective

- Testing timing difference between two repetitive digital signals
  Ex.
  Data and clock
  in Double Data Rate (DDR) memory



- Short testing time
- Good accuracy

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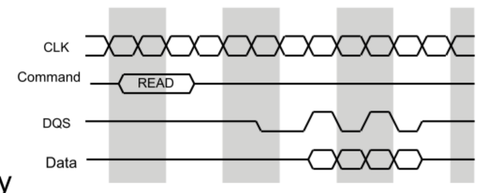
Implement with small circuitry



Our Work

Focus on Multi-bit ΣΔTime-to-Digital Converter (TDC)

- Repetitive digital signals
  ⇒ ΣΔ TDC can be used
- Simple circuit
- Fine resolution
- Testing time
  Single-bit ΣΔ TDC Long
  Multi-bit ΣΔ TDC Short
- Linearity
  Single-bit ΣΔ TDC Good
  Multi-bit ΣΔ TDC Bad due to delay elements mismatches

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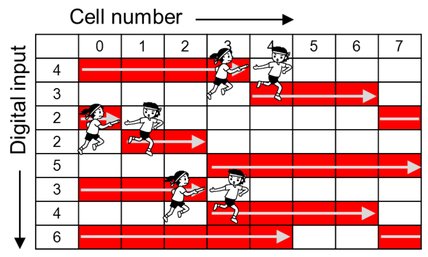
Three methods for their compensation

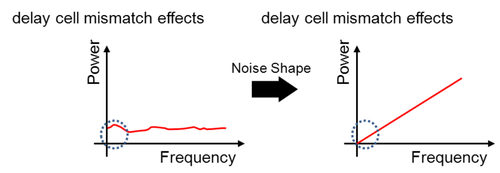
↳ DWA, Self-calibration, Delay cell sorting

Mechanism of DWA

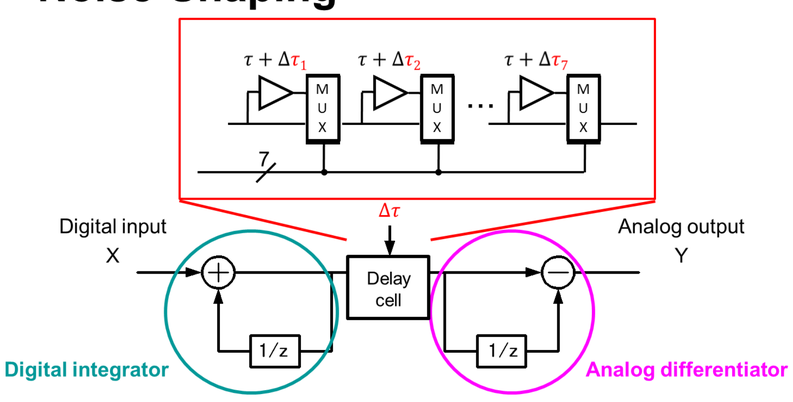
DWA & Noise Shaping



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation



Noise-Shaping



$$Y(z) = X(z) + (1 - 1/Z)\Delta\tau(z)$$

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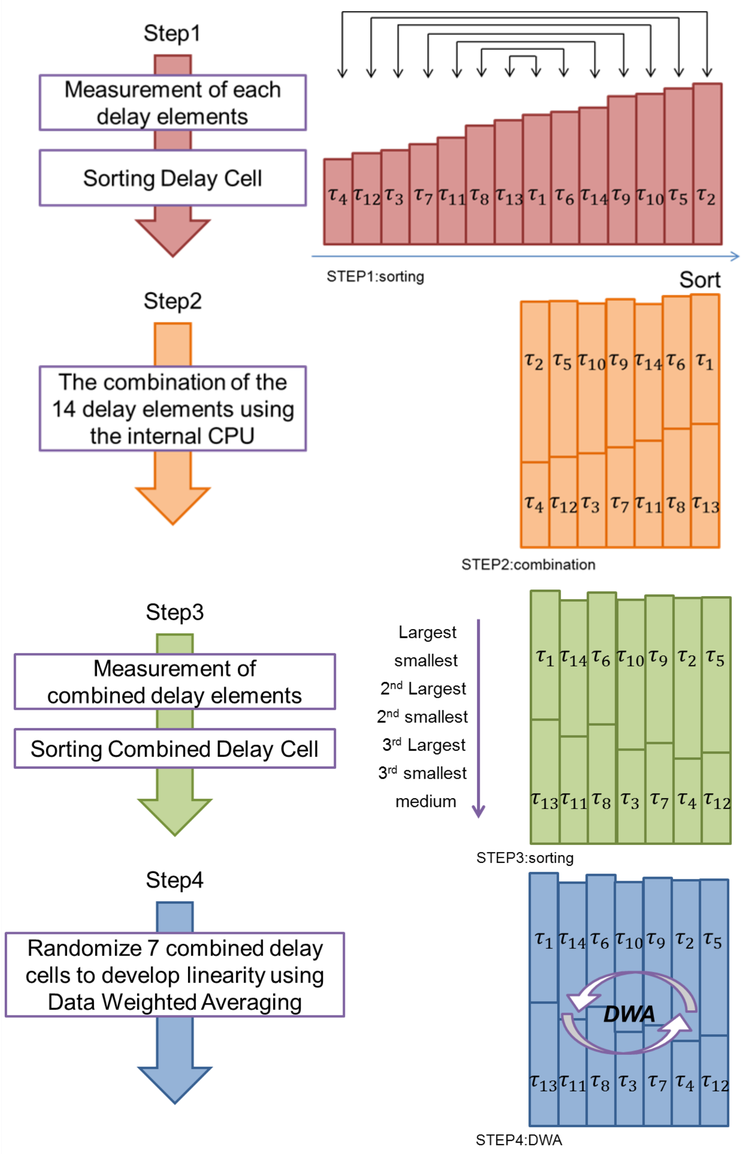
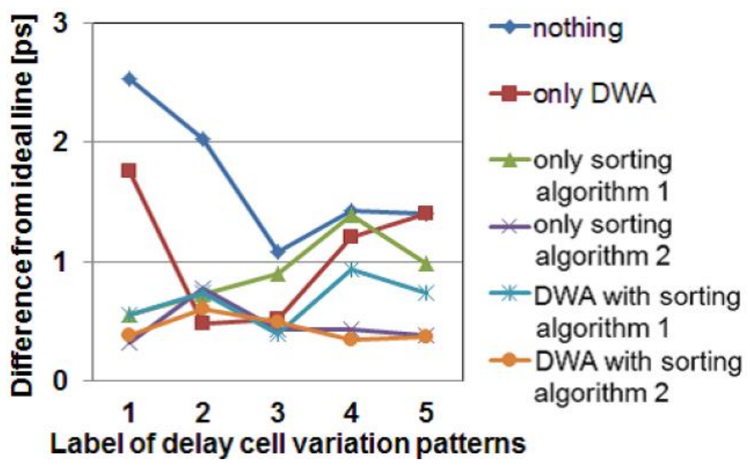
Delay mismatch $\Delta\tau$ is first-order noise-shaped.

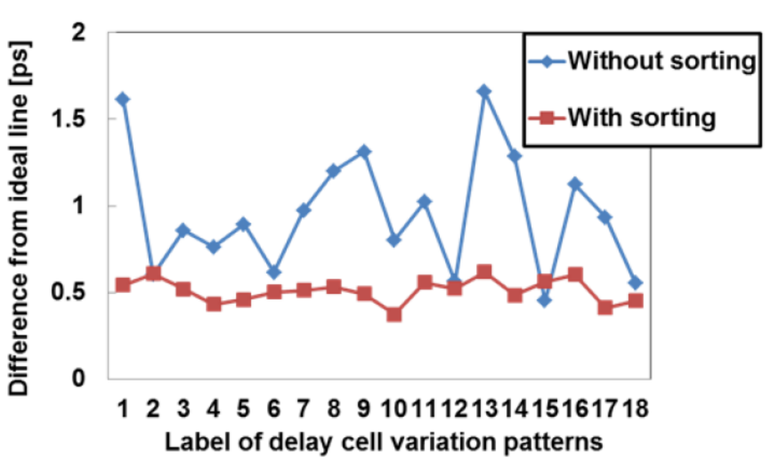
Procedure of Sorting



Matlab Simulation result



Simulated TDC INL (rms) for all possible combinations of sorting algorithms 1, 2 and DWA in 5 cases of delay cell variations



Averaged (rms) integral nonlinearity with and without sorting algorithm 2 in 18 cases of delay cell variations.

TDC circuit is widely used for timing measurement, for example, DDR memory test at factory line.

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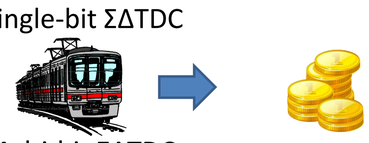
Multi-bit ΣΔTDC is faster test than Single-bit one.
Fast test realizes COST DOWN !!

Single-bit ΣΔTDC



Multi-bit ΣΔTDC

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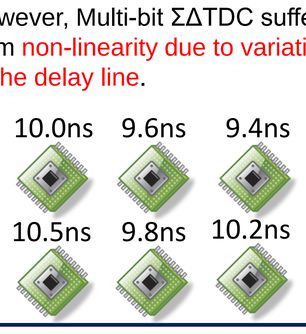
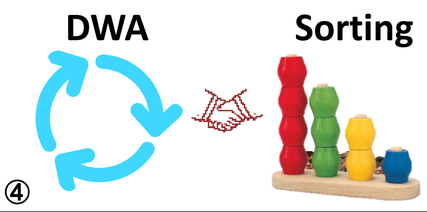
However, Multi-bit ΣΔTDC suffers from non-linearity due to variation of the delay line.



③

DWA & Sorting algorithm make Multi-bit ΣΔTDC possible to test fastly with high-resolution !!



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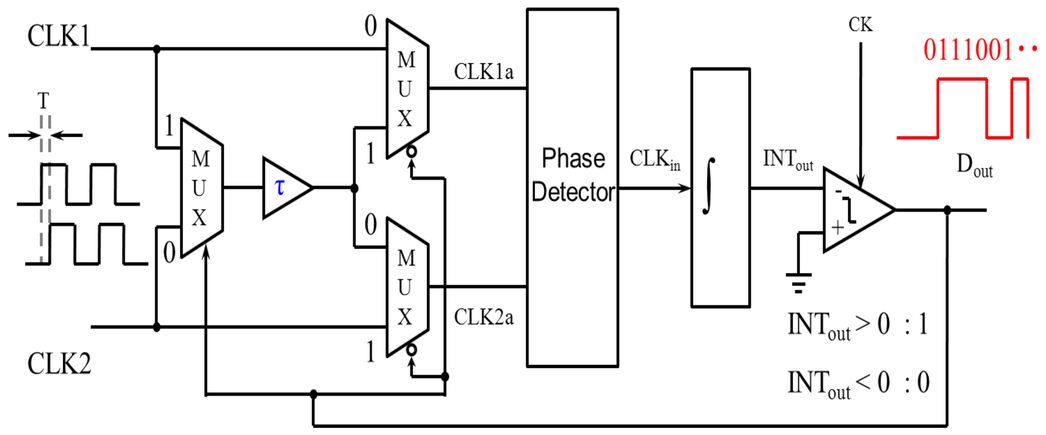
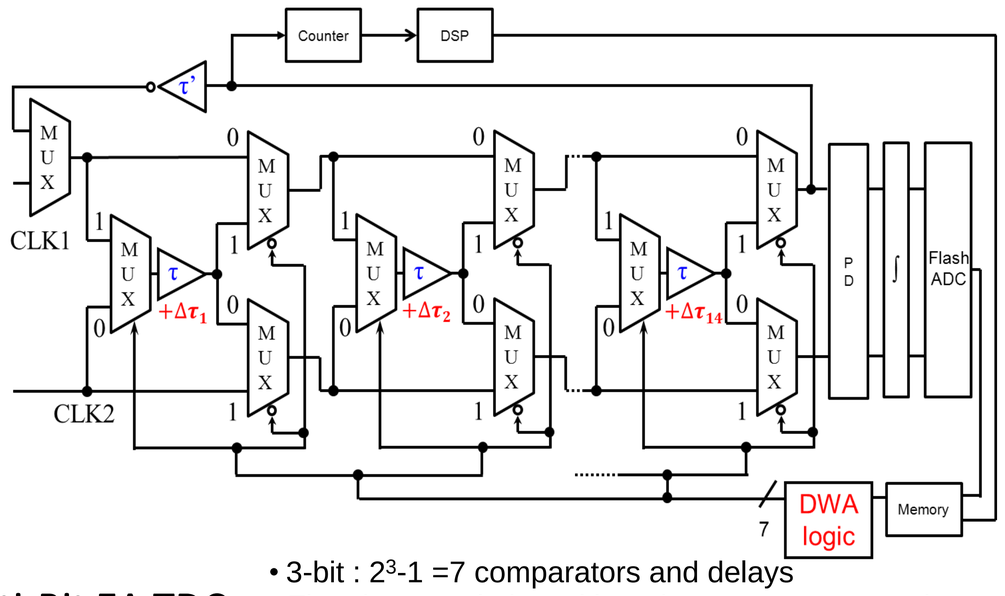
Structure of ΔΣTDC



Single-Bit ΣΔ TDC



Multi-Bit ΣΔ TDC

- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

⇒ Shorter measurement time with a given time resolution

Conclusion

	Flash TDC	1-bit ΣΔ TDC	Multi-Bit ΣΔ TDC (w/o correction)	Multi-Bit ΣΔ TDC (w/ correction)
Area	×	◎	○	○
Resolution	×	◎	◎	◎
Accuracy	△	◎	×	◎
Time	◎	×	○	○

- We propose to use ΣΔ TDC for digital signal timing measurement
- Multi-bit ΣΔ TDC
  - ➢ Short measurement time
  - ➢ Fine time resolution
  - ➢ Non-linearity due to mismatches among delay cells
    Three techniques to improve linearity
    - DWA
    - Self-Calibration (signal is "time")
    - Sorting

Kobayashi Laboratory