Bias Temperature Instability Dectection of Integrated Circuit

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In this paper, we explain the influence of Bias Temperature Instability (BTI) in circuit operation and propose a method for detecting BTI degradation of circuit in order to design a robust system. Negative BTI takes place when transistor is negative-biased, which is a usual biasing for PMOS. Intuitively, Positive BTI is caused when the transistor is positive-biased, usual biasing for NMOS.

Although many physical details are still under investigation, it has been widely accepted[2][4] that the electrical field across the oxide causes continuous trap generation in Si-SiO_2 interface of transistor. These traps usually originate from Si-H bonds in gate oxide layer [1][4]. These bonds can easily break with time and generate positive interfacial traps (donor-like state). This understanding is described by Reaction-diffusion (R-D) analytical models[1] [2][4].

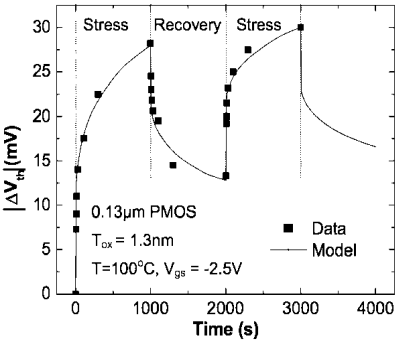

Fig. 1.ΔV_{th} during dynamic NBTI.

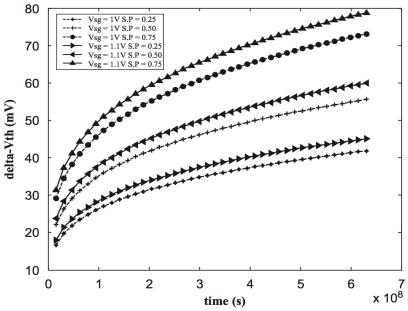

Fig. 2. V_{th} increase due to BTI.

Amongst of all consequences of generated traps, transistors threshold voltage shift has been most dominant. During the time transistor is under the stress V_{th} increases, while in the recovery time this V_{th} shift shrinks, but is never nullified, as shown in the Fig1. Due to these V_{th} shift (Fig.2), circuit operation faces a significant operational delay as depicted in Fig.3 for a comparator circuit.

Fig.3 shows, a comparator circuit without BTI degradation has a delay of 25ns, whereas, with 10 years of BTI degradation the output delay rises up to 112ns, which is almost 4 times the initial delay with a significant slew rate degradation compare to a fresh circuit. Utilizing this slew rate degradation characteristics we can detect BTI degradation, using a transition-time comparator (TTC). TTC circuit will measure and compare delay with the fresh condition to detect degradation condition. Therefore feeding this value into a Dynamic Voltage Scaling system (as it is possible to reduce oxide trap by scaling gate voltage[5]) we can reduce the effect of BTI degradation.

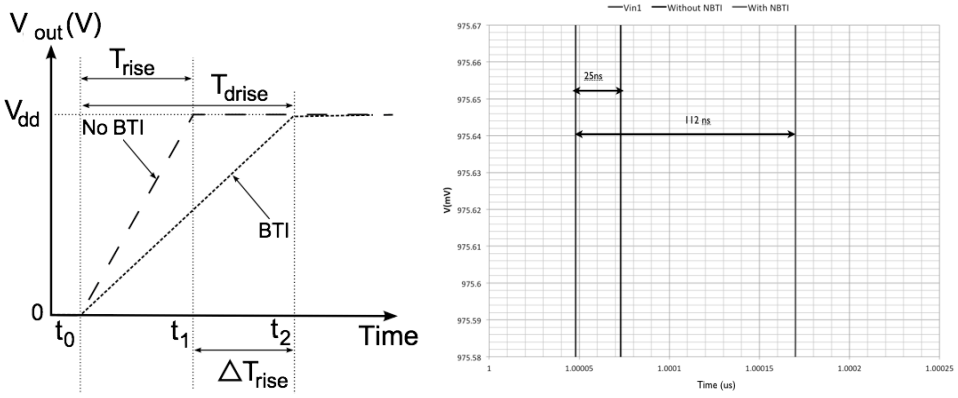

Fig. 3. Degradation in slew rate due to BTI.

[1] Biswas Sumit Kumar, Kamiyama Toru , Takai Nobukazu , Kobayashi Haruo, "Impact of NBTI Reliability Degradation on Nano-scale MOS Transistor and Efficacy of NBTI Mitigation Techniques,"(2013). [2] M. A. Alam, S. Mahapatra, "A comprehensive model of PMOS NBTI degradation, Microelectronics Reliability," V45, I1, (2005). [3] Porto Alegre, Dr. Renato Perez Ribas, Dr. André Inácio Reis, "CMOS Digital Integrated Circuit Design Faced to NBTI and Other Nanometric Effects," (2010).[4] R. F. Pierret, "Semiconductor Device Fundamentals," Addison Wesley (1996). [5] Tuck-Boon Chan, John Sartori, Puneet Gupta and Rakesh Kumar, "On the Efficacy of NBTI Mitigation Techniques," EDAA(2011).