Paper ID 28
SFDR Improvement Algorithm for Current-Steering DACs

Shaiful Nizam Mohyar*,
H. Hassan, M. Murakami, A. Motozawa, H. Kobayashi,
O. Kobayashi, T. Matsuura, N. Takai, I. Shimizu,
K. Niitsu, M. Tsuji, M. Watanabe, N. Dobashi,
R. Shiota, S. Umeda,T. J. Yamaguchi
†

Gunma University, Japan
Universiti Malaysia Perlis, Universiti Teknologi MARA, Malaysia
Nagoya University, STARC, Japan

Outline

- Introduction
- Switching-Sequence Post-Adjustment (SSPA)
- One-Element-Shifting (OES)
- SSPA & OES Combination
- Simulation Result
- Conclusion

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Introduction

- **Background**
  - Telecommunication devices
    - Mobile phones, wireless modems & avionics
    - **High-speed, high-accuracy DAC!!!**

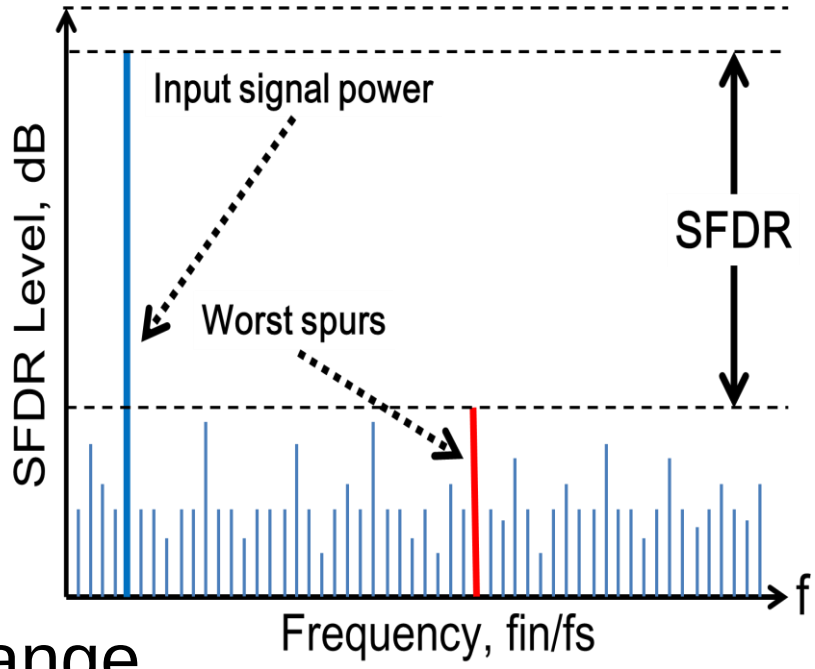
- **Application**
  - Transmitters
    - Interference reduction
    - High SFDR performance

- **Our approach**
  - **Digital rich for high SFDR DAC**

DAC – Digital-to-Analog Converter
SFDR – Spurious Free Dynamic Range

Spurious Free Dynamic Range (SFDR)

- **Degradation sources**
  - Data-dependent switching transients
    - ➔ Temporal disturbance
  - Data-dependent output load variations
    - ➔ Output impedance change



Objective & Investigated Method

- **Objective**
  - High SFDR
    - Mismatch effect reduction
    - Low glitch
- **Proposed method**
  - Current source mismatches
    - ➔ Switching-Sequence Post-Adjustment (SSPA)
  - Glitch effect
    - ➔ **One-Element-Shifting (OES)**
  - **Dynamic nonlinearity**
    - ➔ **SSPA & OES Combination**

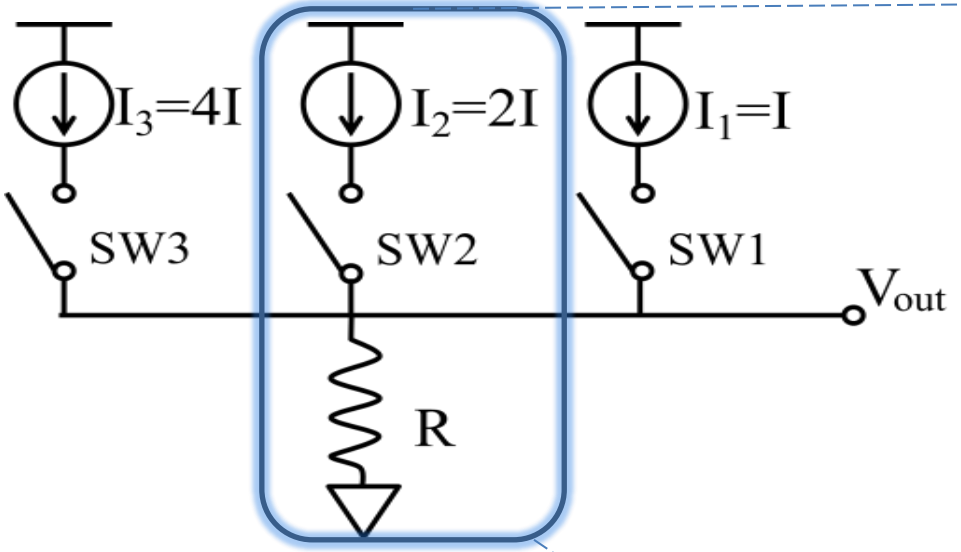
Design Approach

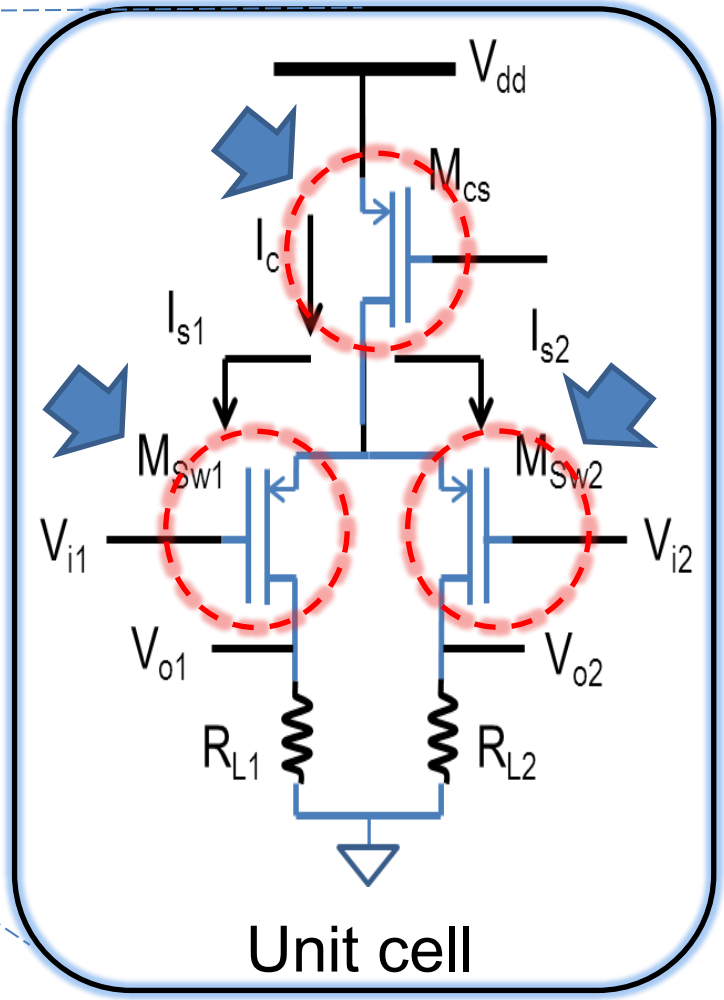
- **Analog**
  - Complex hardware
  - Not programmable
  - Expensive (production & testing)

- **Digital**
  - Simple
  - Programmable
  - Low-cost

➔ **Digital rich approach for fine CMOS implementation**

Current-steering DAC (CS DAC)





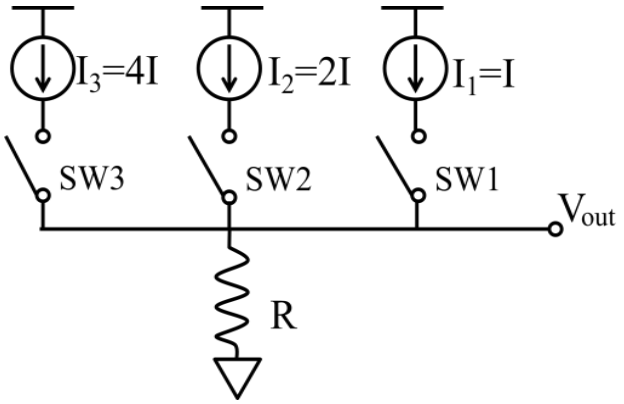
- High-speed
- Easy to integrate
- High-resolution
- Low-power
- Small chip area

CS DAC limitation

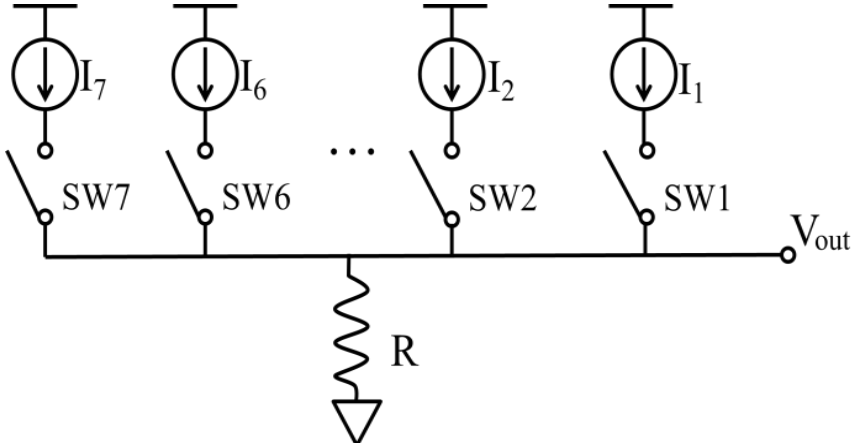
- **Transistor mismatch**
  - Current source mismatch
  - Source of timing errors
- **Mismatch among current cells**
  - Causing DAC static & dynamic non-linearity
- **Better transistor matching**
  - Big size ➔ Power loss
  - Laid out close to each other ➔ Complicated

Binary versus Unary CS DAC

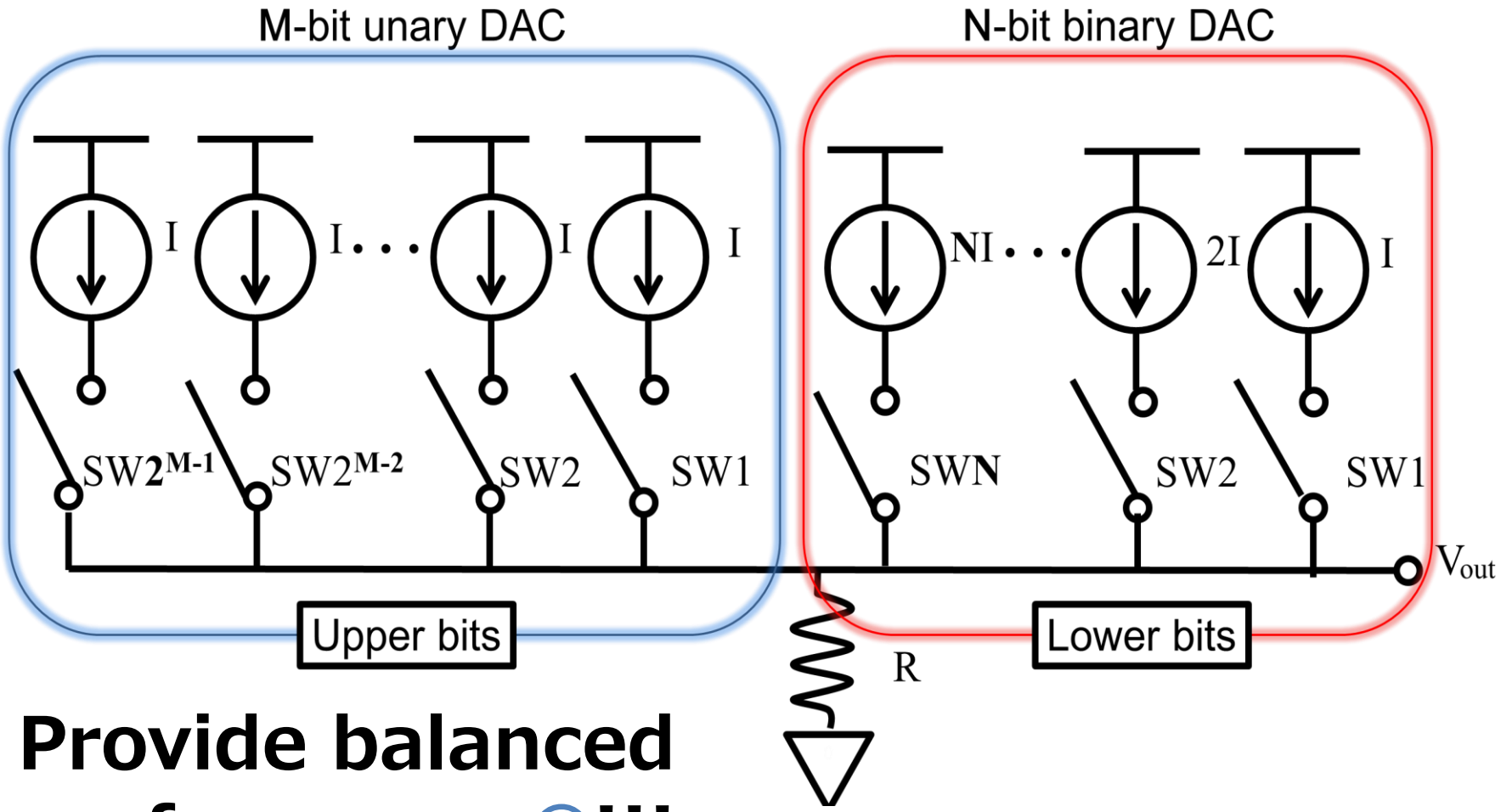
- **Binary**
  - Small silicon area ☺
  - High sampling speed ☺
  - Large glitch energy ☹
  - No redundancy ☹



- **Unary / Thermometer-coded (TC)**
  - Small glitch energy ☺
  - Redundancy ☺
  - Large silicon area ☹

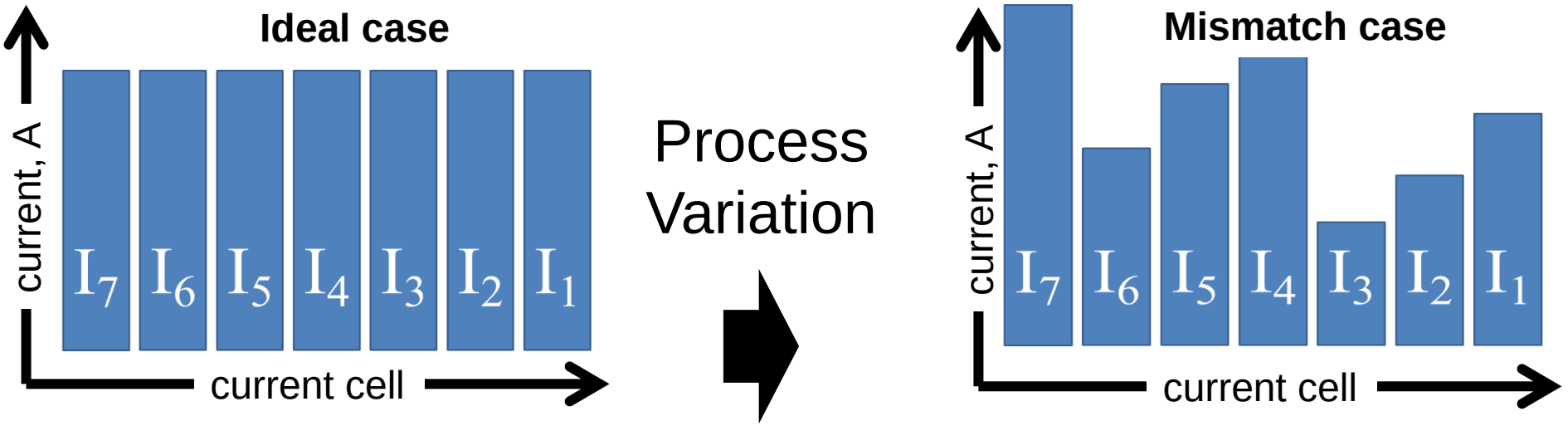


Segmented CS DAC



Provide balanced performance 😐!!!

Current Source Mismatch

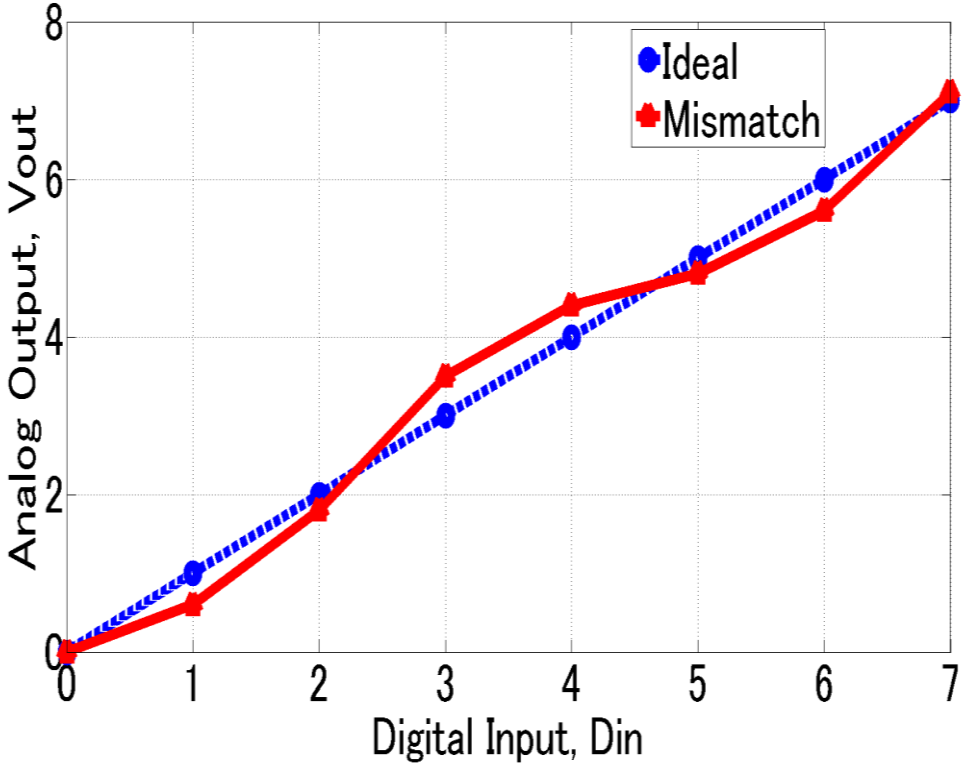


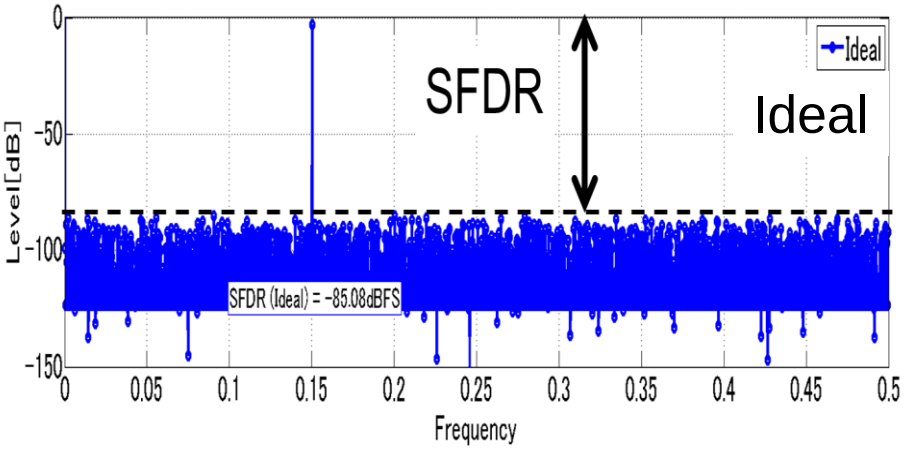
$$I_1 = I_2 = I_3 = I_4 = I_5 = I_6 = I_7 = I$$

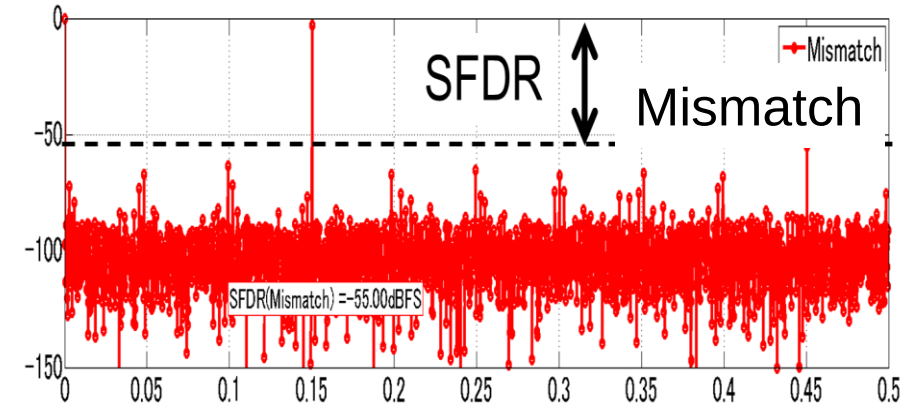
$$I_{ave} = (I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)/7$$
$$I_k = I_{ave} + dI_k \quad (k = 1, 2, .. , 7)$$

➔ **DAC nonlinearity ☹!!!**

Nonlinearity & SFDR degradation







Mismatch ➔ Nonlinearity

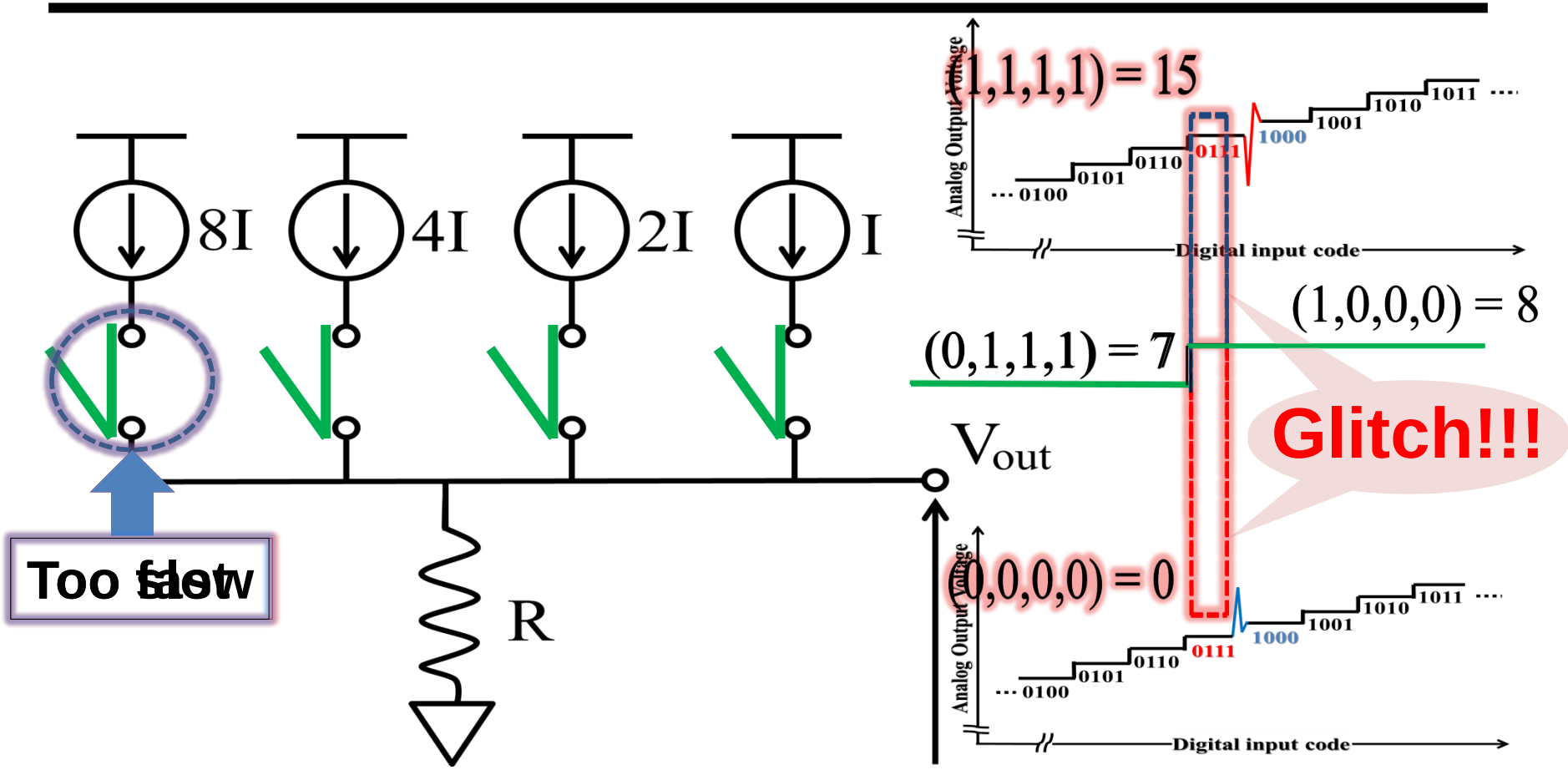
SFDR degradation

SFDR – Spurious Free Dynamic Range

What is Glitch?

- **Main causes**
  - Non-ideal switching behavior
    between two consecutive update steps
    ➔ **MAJOR!!!**
  - Signal feedthrough
    gate-drain capacitances
  - Static timing uncertainty
    between two different current cells
  - Asymmetric up & down output characteristics

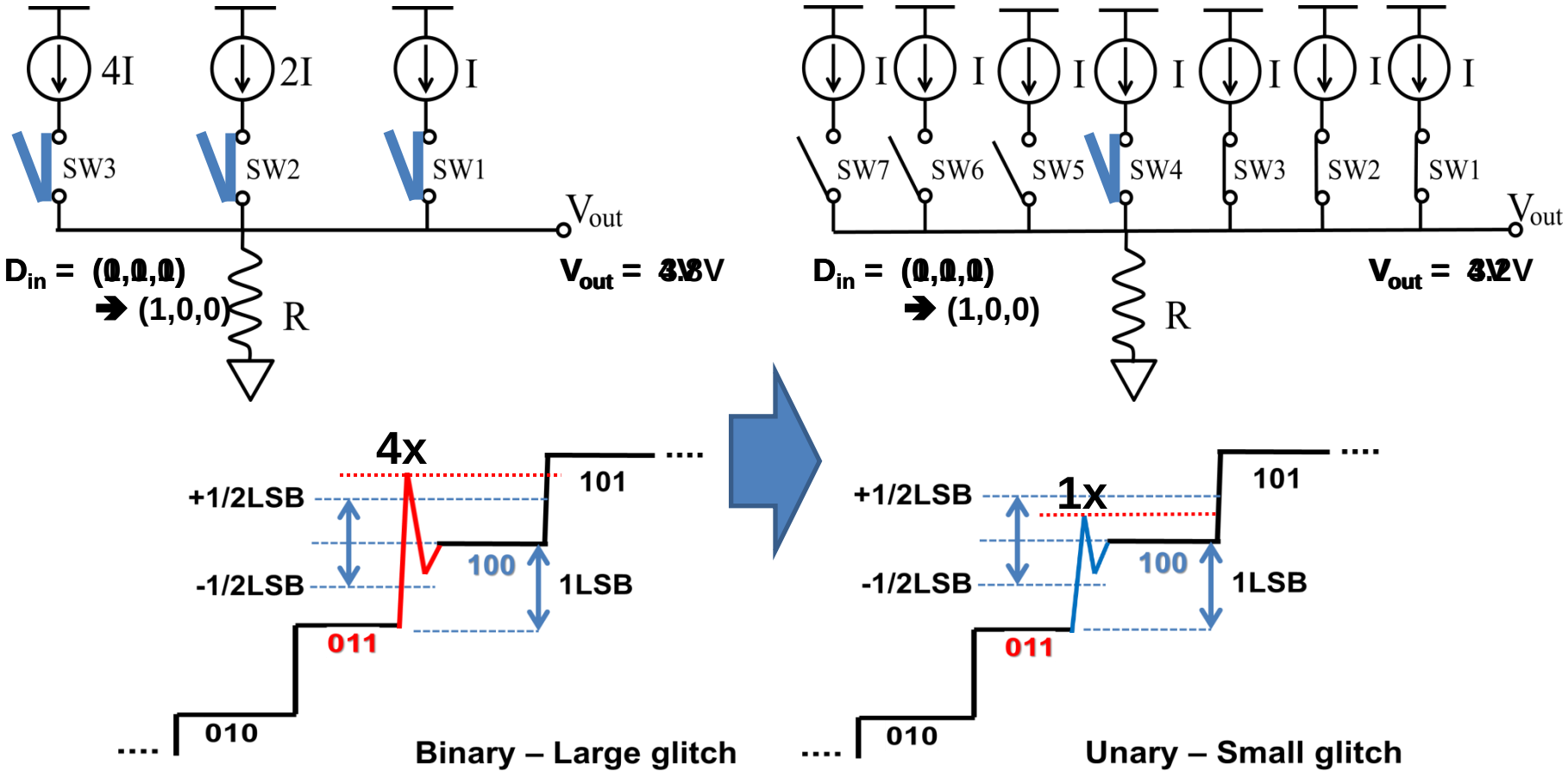
Glitch by non-ideal switch



D_{in} = (0,1,1,1) ➔ (1,0,0,0)

V_{out} = 7.5V

How glitch reduce by Unary?



Unary ➔ Small glitch ☺, Current source mismatch ☹

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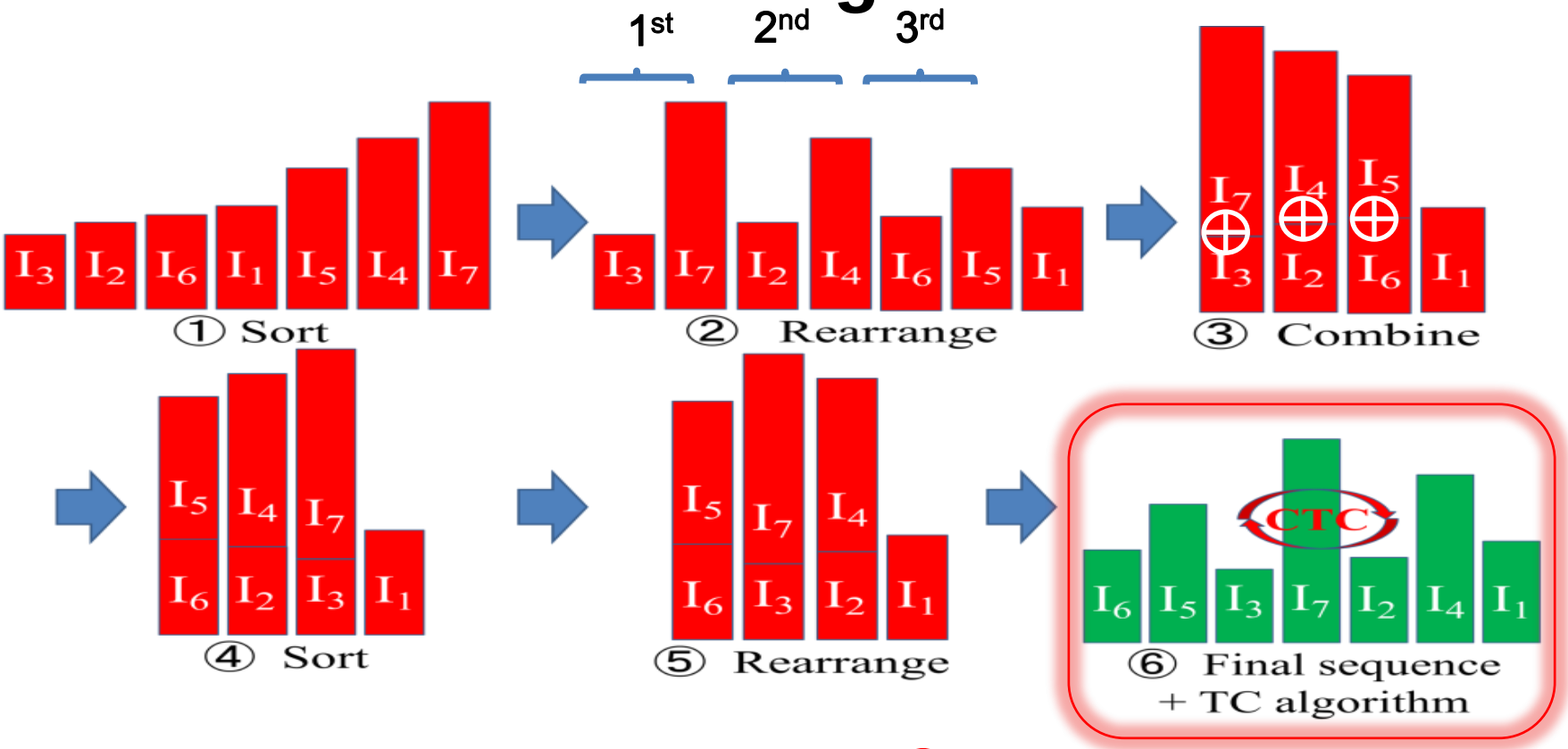
Why SSPA

- **Post-fabrication non-linearity improvement**
- **Small additional circuits**
  - Current comparator (DSP inside SoC)
- **Simple implementation**
- **Require extra current sources**
  - Replacement → defect / worst mismatch
- **Complicated wiring**

SSPA Operation

- **Current source sorting**



Data-dependent output ☹!!!

SSPA – Switching-Sequence Post-Adjustment
TC – Thermometer-code

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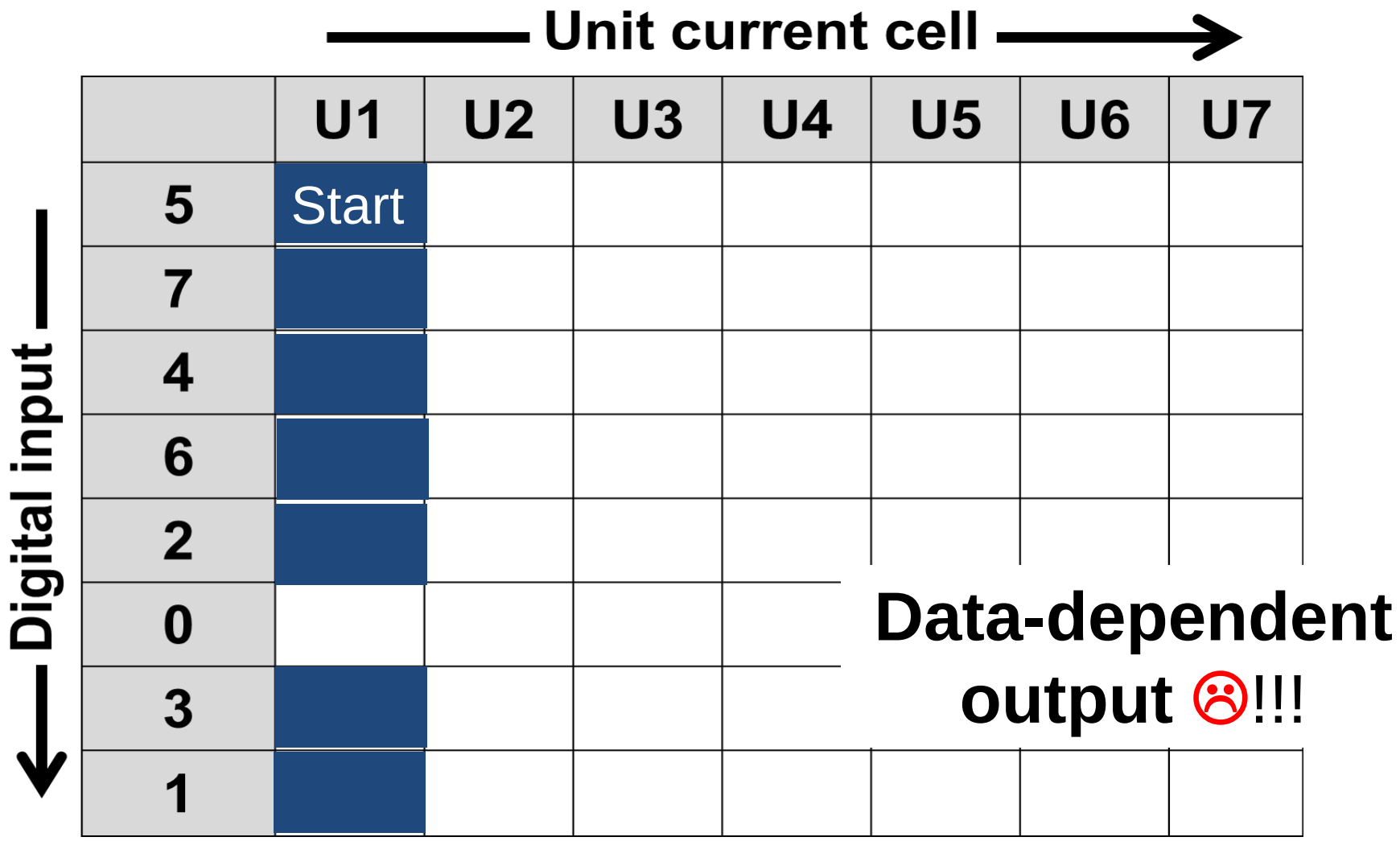
TC Operation



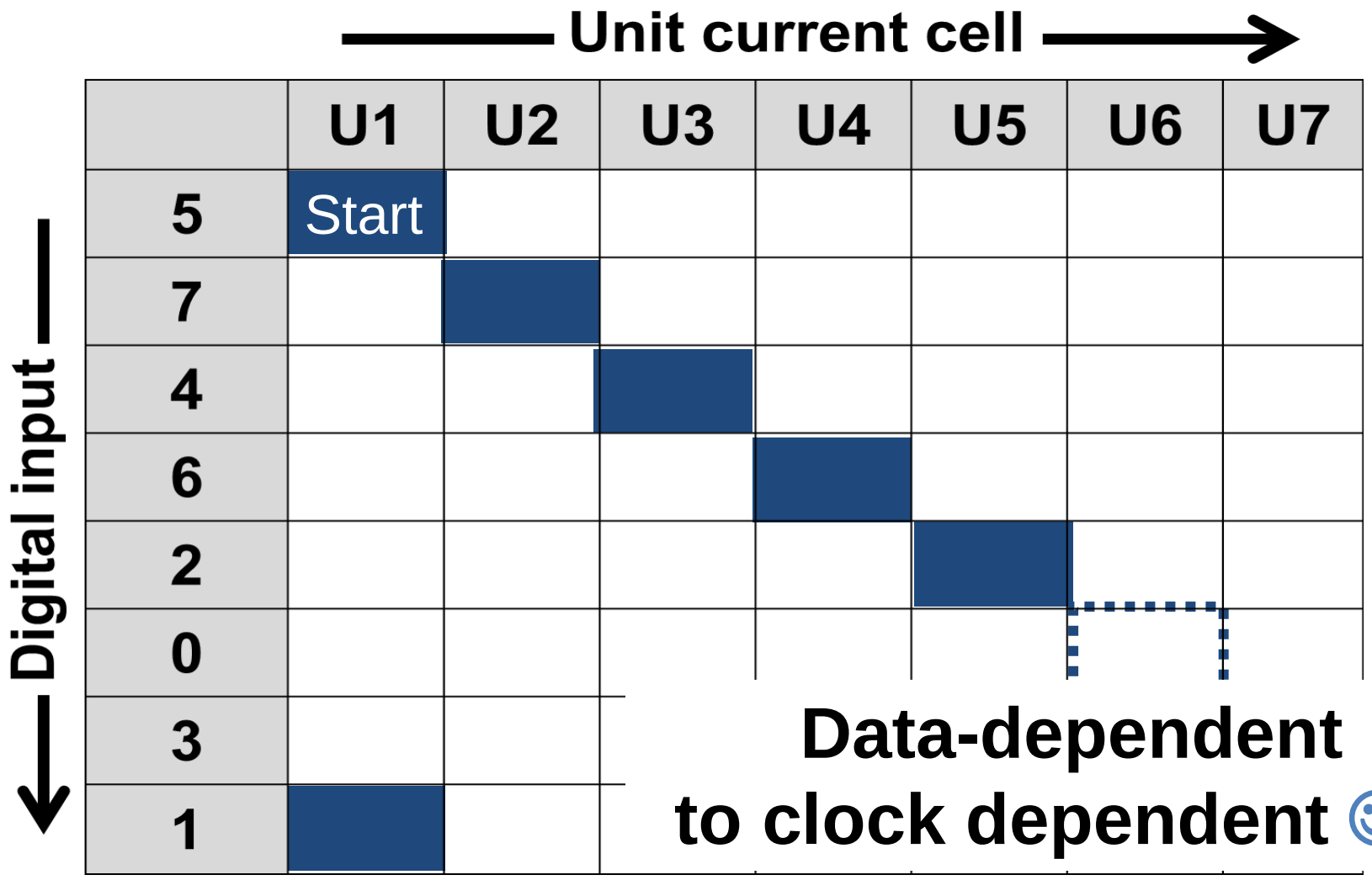
Why OES

- **Change data-dependent to data-independent**

  ➔ Disturbance reduction
- **Glitch as small as in TC**

  ➔ Low-power
- **Simple implementation**

OES Operation



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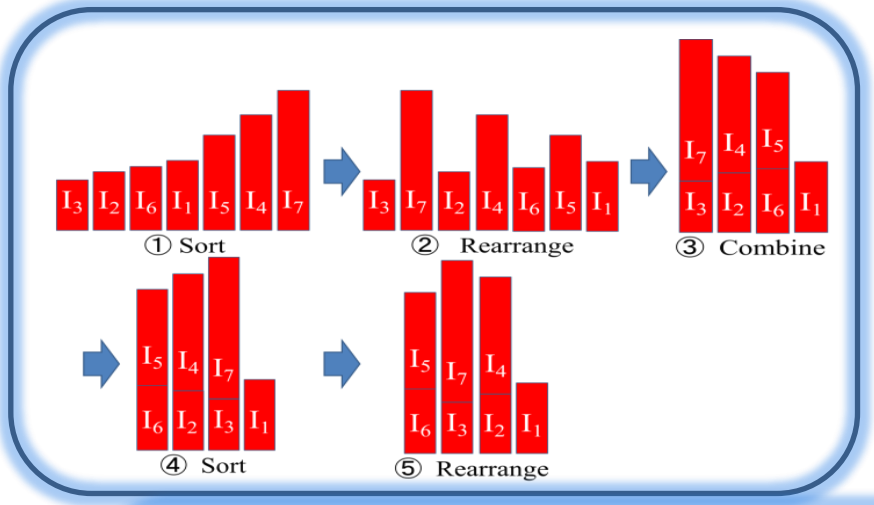
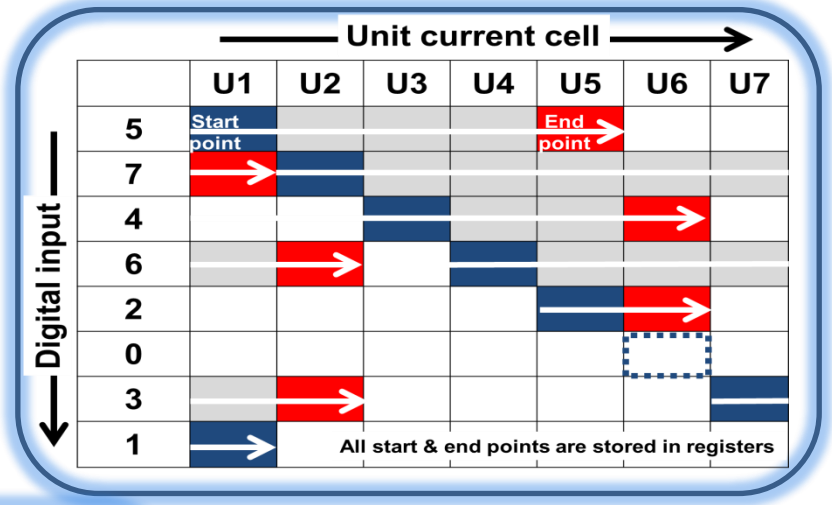
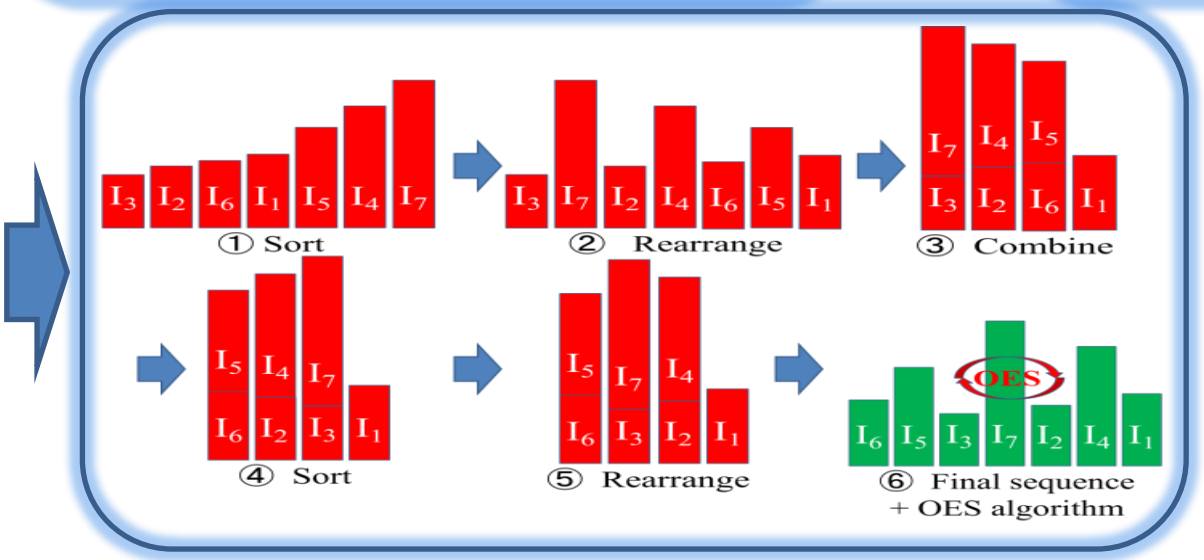
SSPA & OES Combination







Aims:

① Mismatch induced distortion reduction

② Output-dependent distortion suppression

SSPA – Switching-Sequence Post-Adjustment
OES –One Element Shifting

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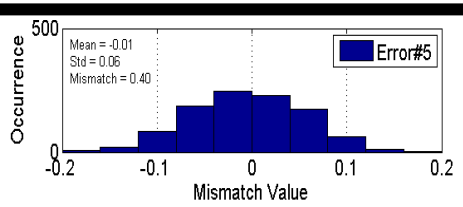
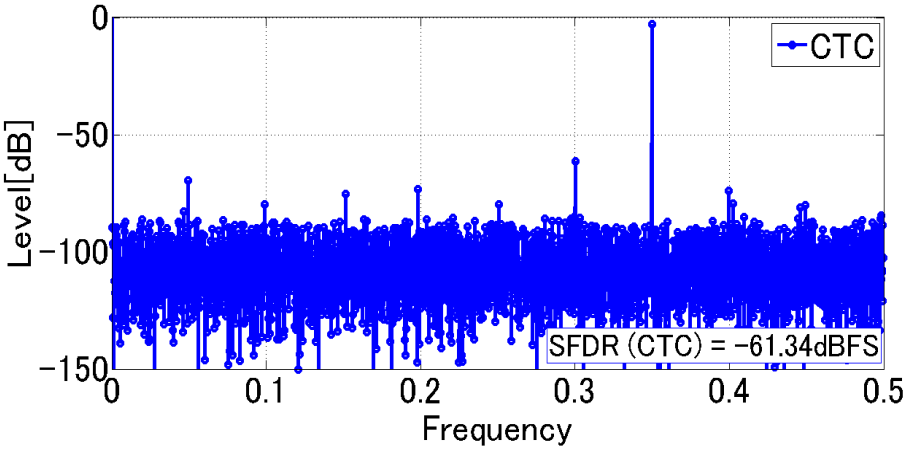
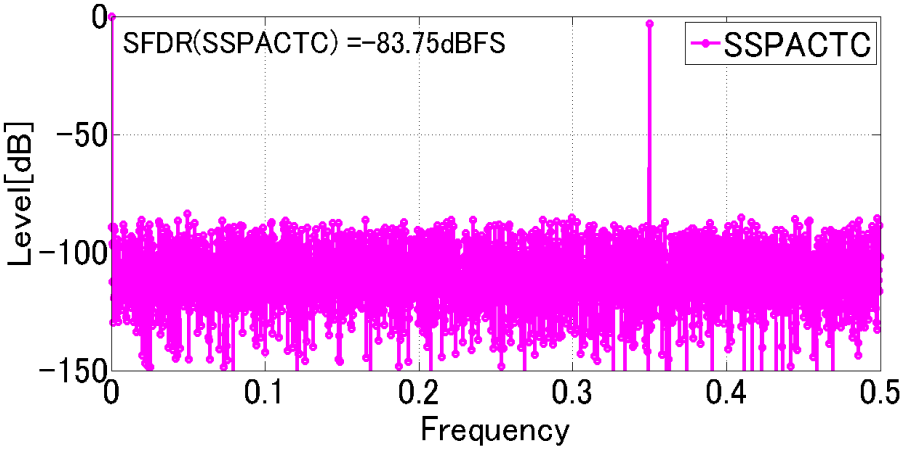
SFDR Performance

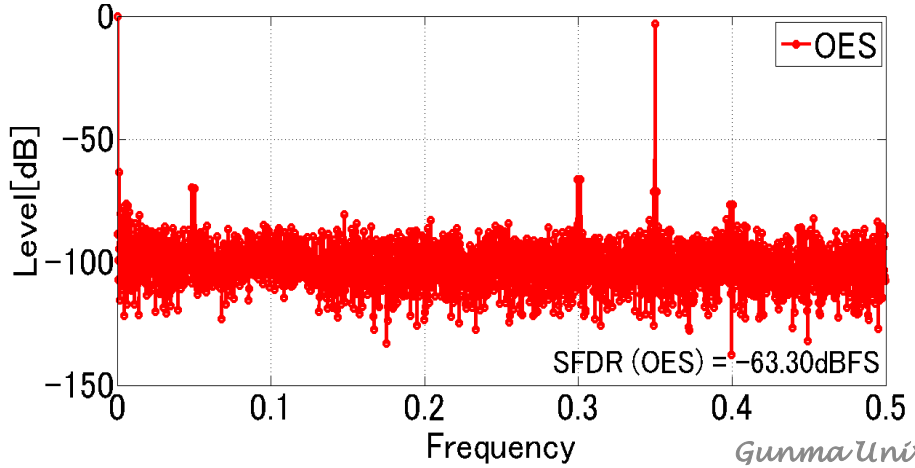


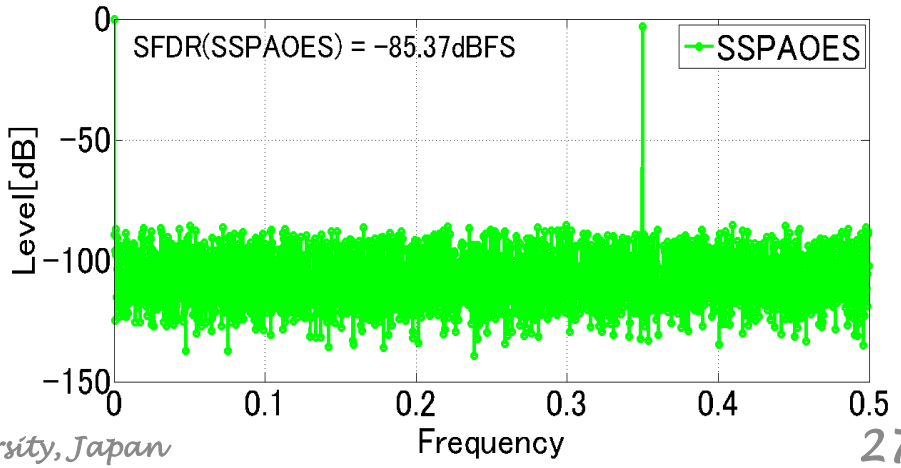
fin = 1.433MHz, fs = 4.096MHz, 10-bit

σ: 6% , min:-20%, max:-20%



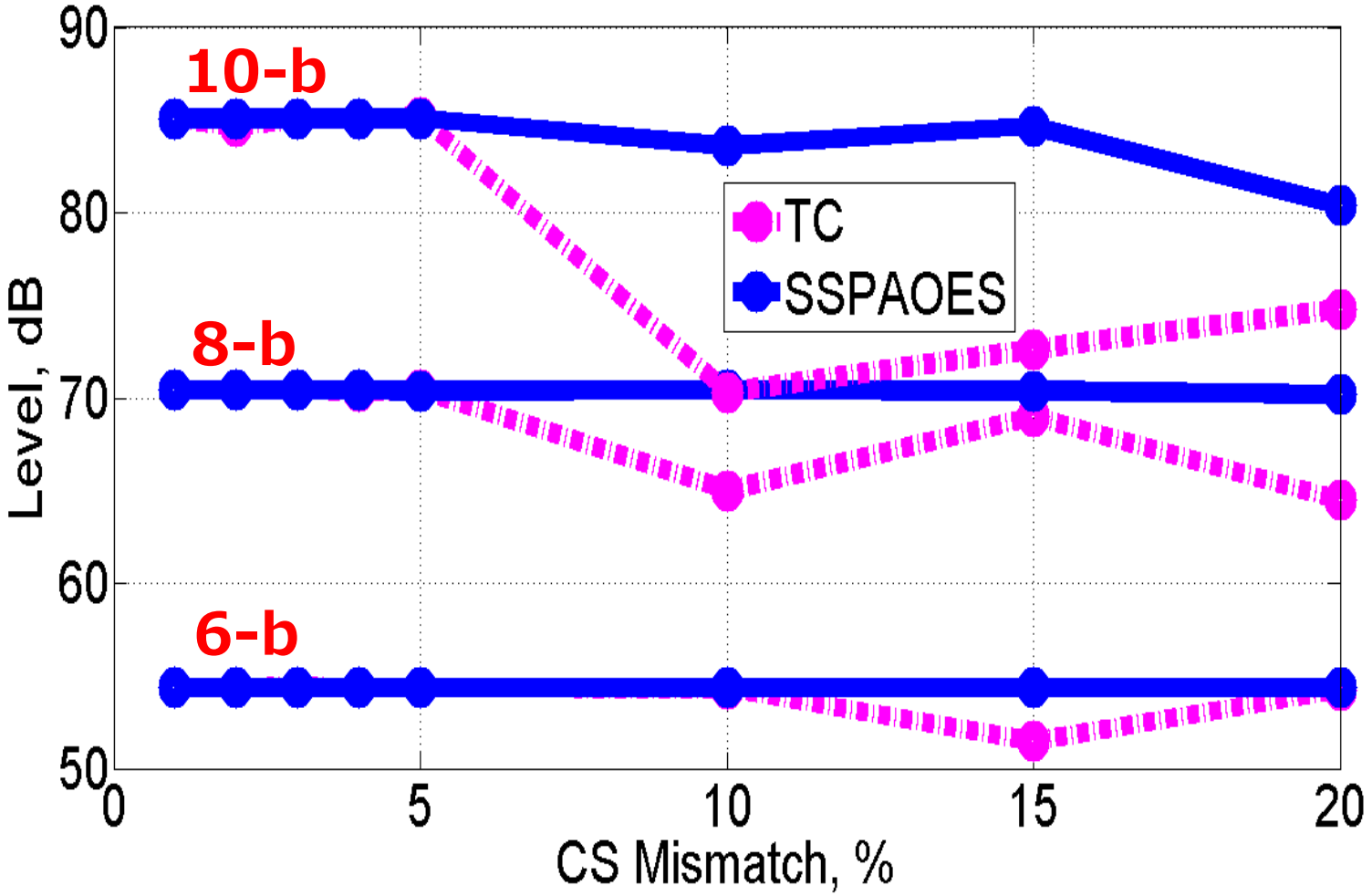






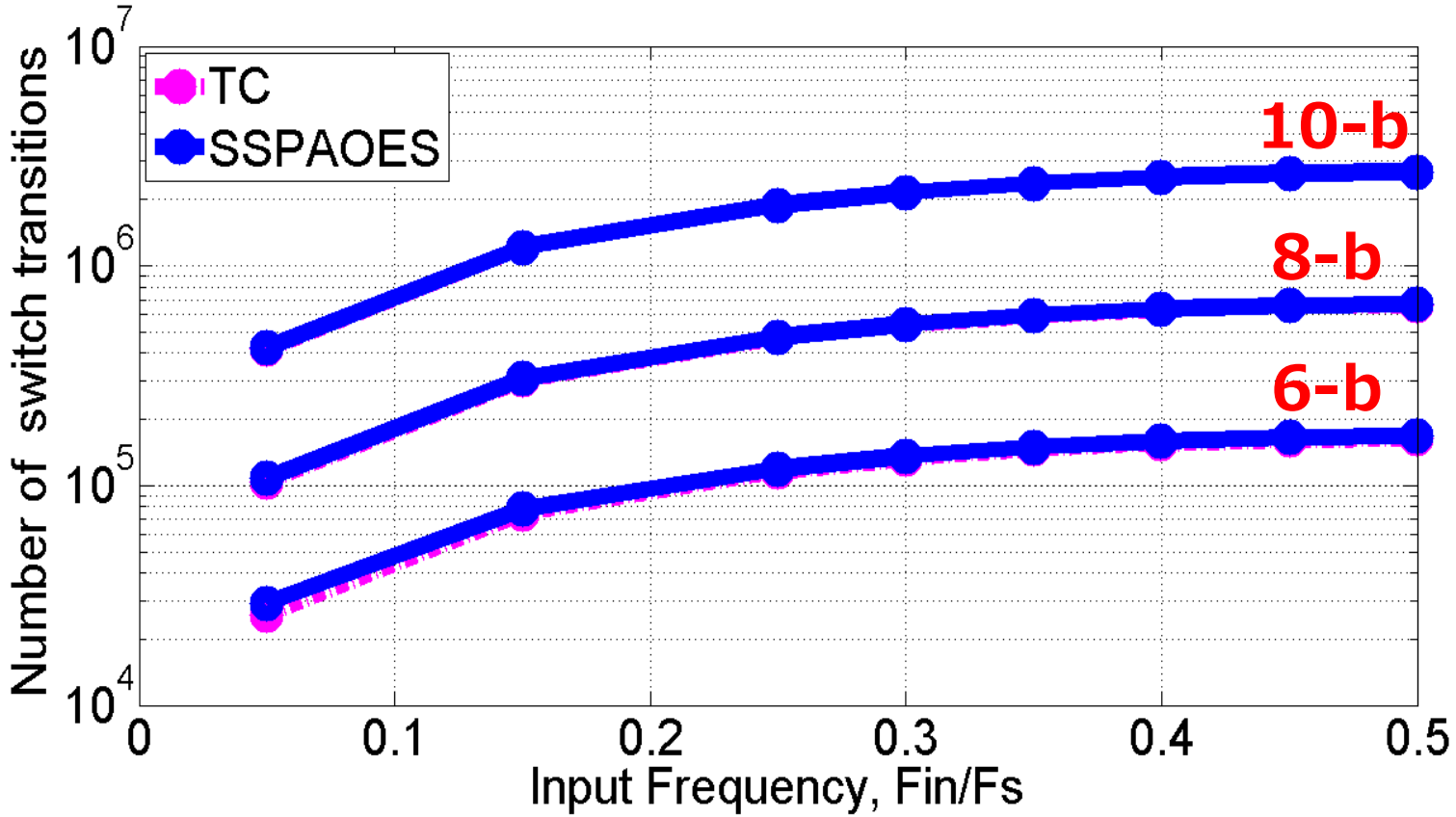
SSPA – Switching-Sequence Post-Adjustment OES –One Element Shifting CTC – Conventional Thermometer-code

SFDR Performance vs Mismatch



SSPAOES — Switching-Sequence Post-Adjustment & One Element Shifting Combination TC –Thermometer-code

Glitch



Switch transitions : SSPA&OES ≈TC

➔ Glitch minimized ☺!!

SSPAOES — Switching-Sequence Post-Adjustment & One Element Shifting Combination TC –Thermometer-code

Comparison

fin = 1.433MHz, fs = 4.096MHz, 10-bit
σ: 6% , min:-20%, max:-20%

Algorithm	SFDR (dBFS)	SFDR (dBc)	Diff (dB)	Switching Occurrences	Diff (%)
CTC	61.3	58.3	+ 24.0	2376311	+ 0.18
OES	63.3	60.3	+ 22.1	2380181	+ 0.02
SSPACTC	83.8	80.7	+ 1.6	2376311	+ 0.18
Proposed (SSPA+OES)	85.4	82.4	-	2380692	-

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Conclusion

- **Proposed method**
  - SSPA ➔ Mismatch-induced distortion reduction
  - OES ➔ Data-dependent distortion suppression
- **Simulation result SSPAOES combination**
  - >20 dB SFDR compared to conventional TC
  - Comparable small glitch energy to conventional TC

Thank you
very much
for your kindly
attention

Presented by Shaiful Nizam Mohyar

Question & Answer