

Typical NMOS Modeling Using a Skewing Method

- An NMOS Modeling Method
for RF Analog Circuit Design Centering -

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Outline

- Research Background
- Typical Target Skewing Flow
- Calculations of
 - Theoretical Target Specifications
- Target Device Selection and Its Modeling
- Model Parameter Skew
 - to Typical E-Test Parameters
- Verifications of RF Circuit Simulations
- Conclusions

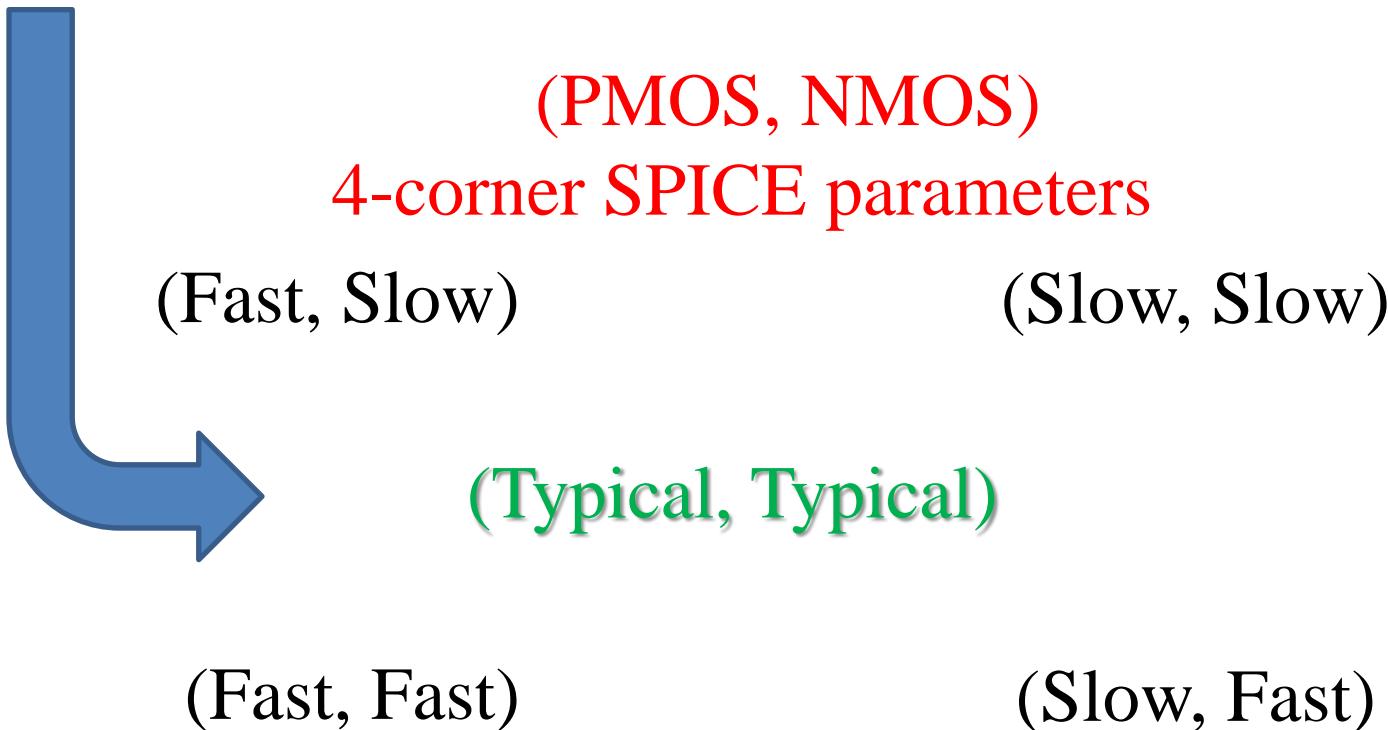
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Research Background

- For better integrated circuit design,
design centering is one of the important issues !



Initial design:

Typical models are used.

Next design step:

Worst/best models are used.

Conventional Method and Problem

- Most semiconductor manufacturers do NOT pay enough attention to extract “Real Typical Models”.
- Conventional methods to define typical target specification are
 - based only on process specifications and conditions
 - without using test results of fabricated devices.



Not very accurate typical model

Research Objective

Development of novel skewing method
for “typical model”

- based on process wafer test (E-Test)
- considers analog and RF circuit design
(both DC, AC characteristics)



Obtain accurate typical model

Our Work

DC, AC Electrical Test (E-Test)

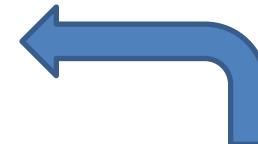


Our new algorithms

Ideal “typical” parameters



Select “typical-like” device



Skew



Extract BSIM4 model parameters

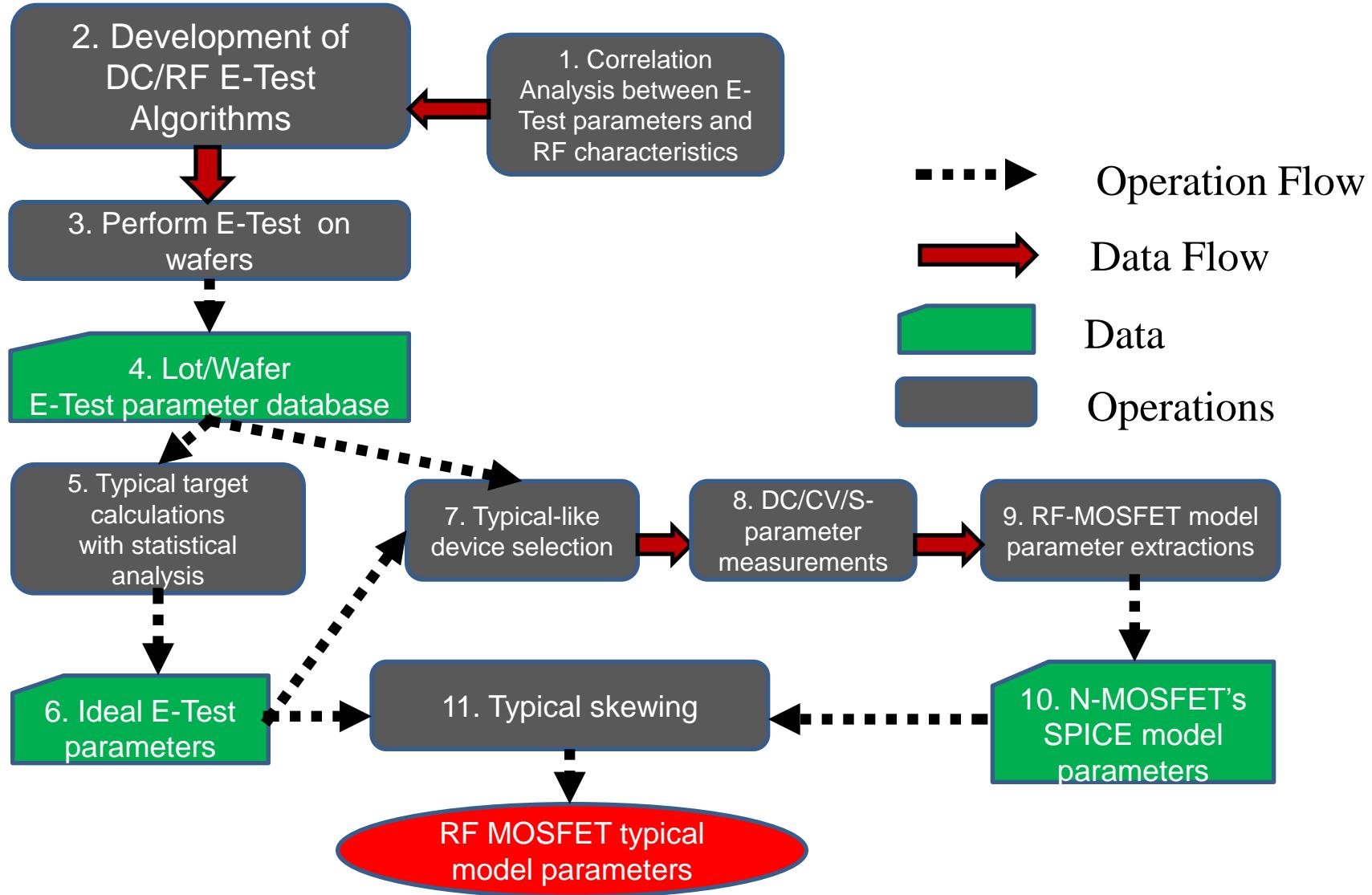


Obtain DC, AC “typical” BSIM4 model parameters

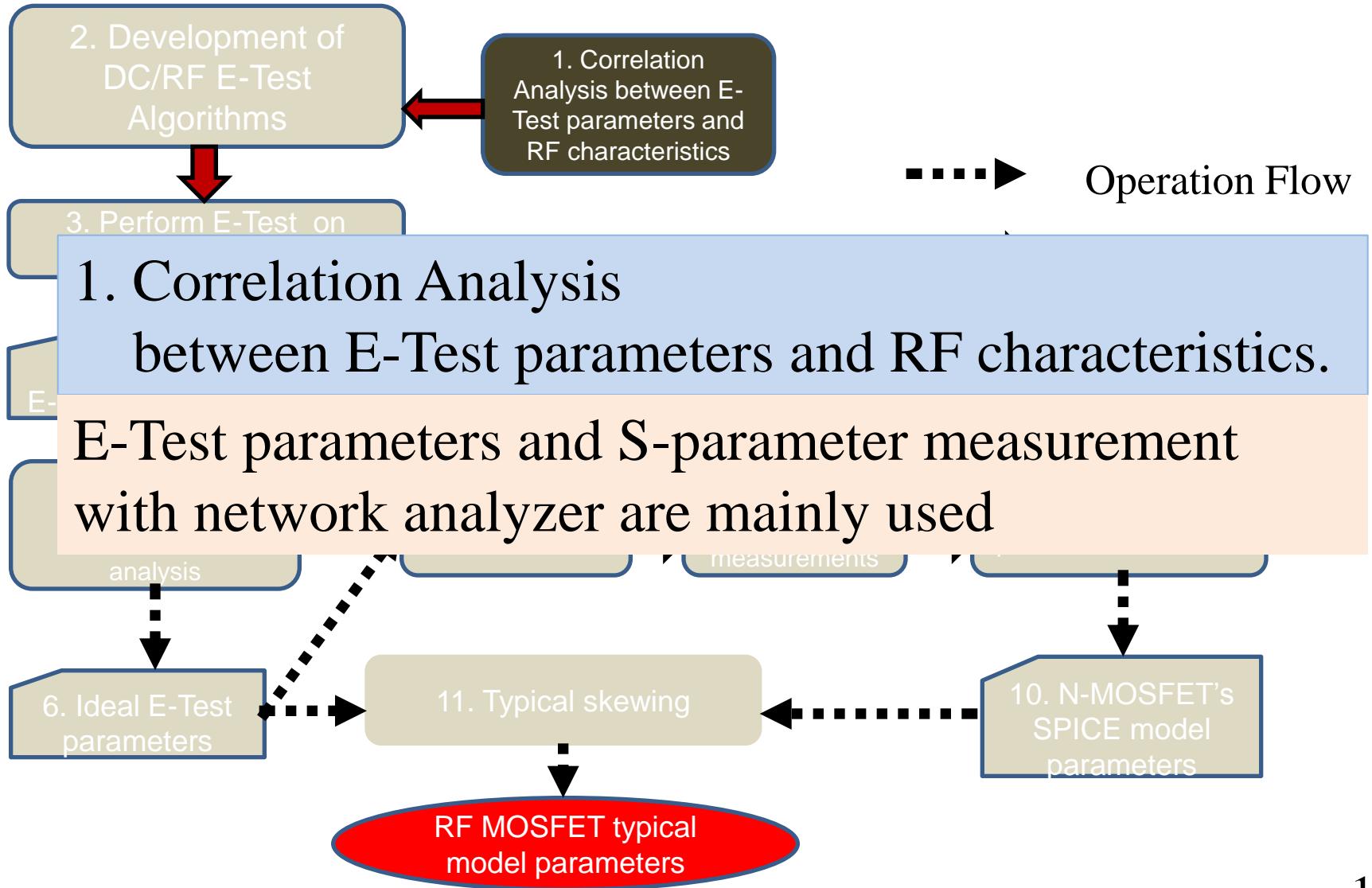
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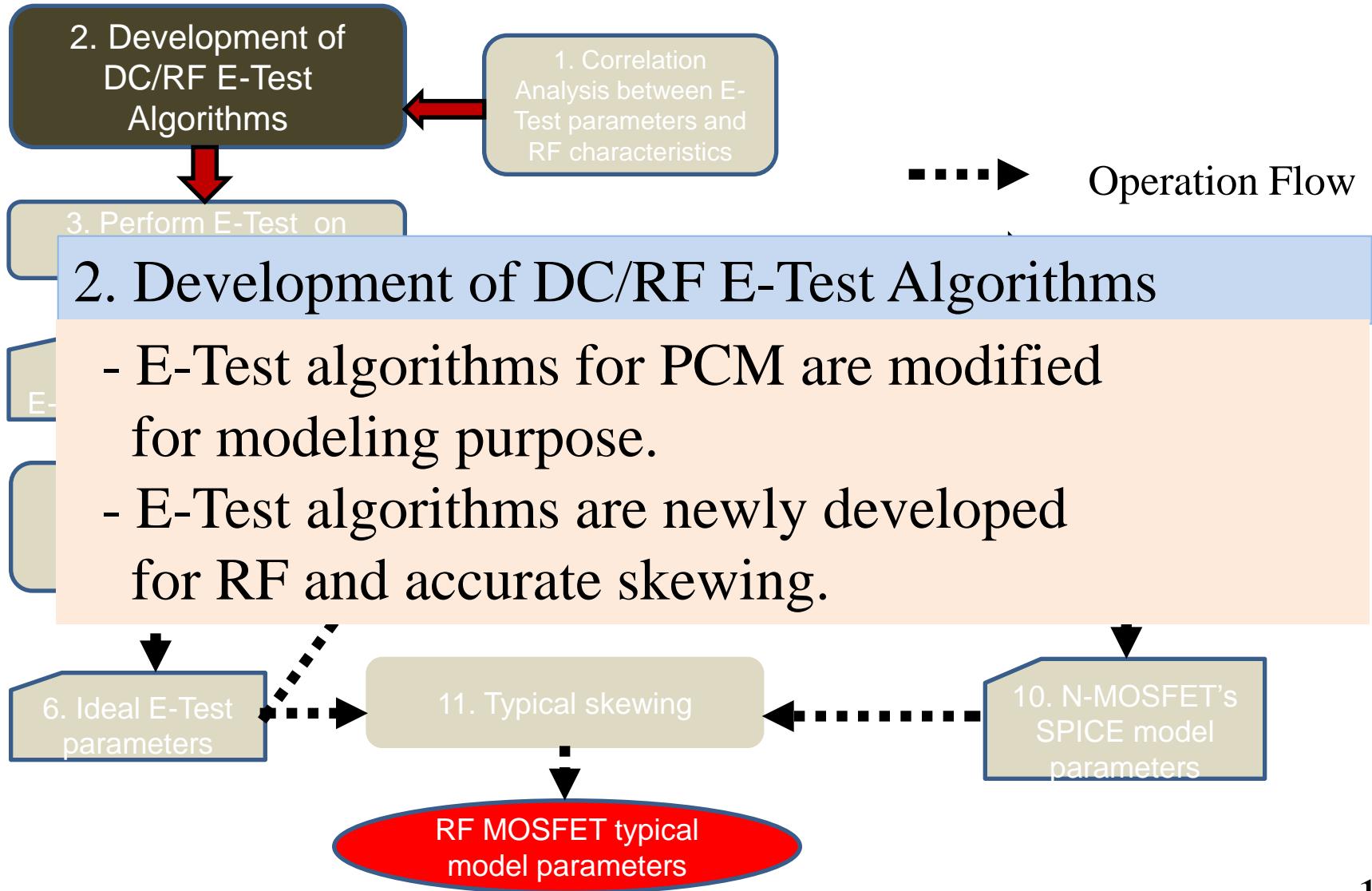
Typical Target Skewing Flow



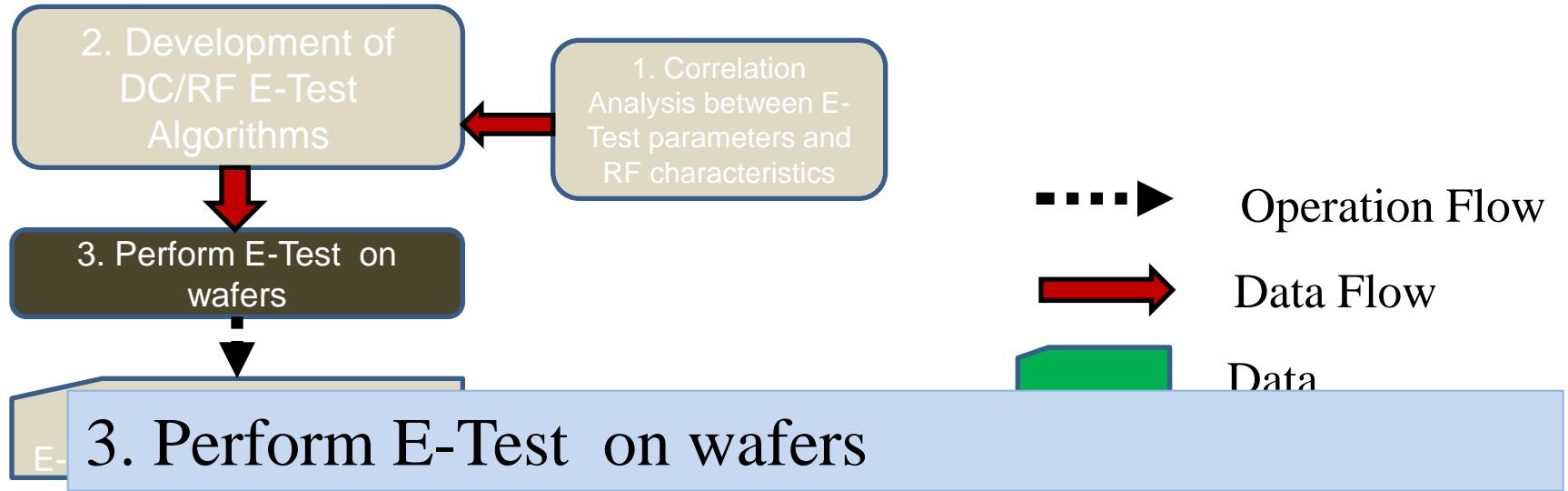
Typical Target Skewing Flow (1)



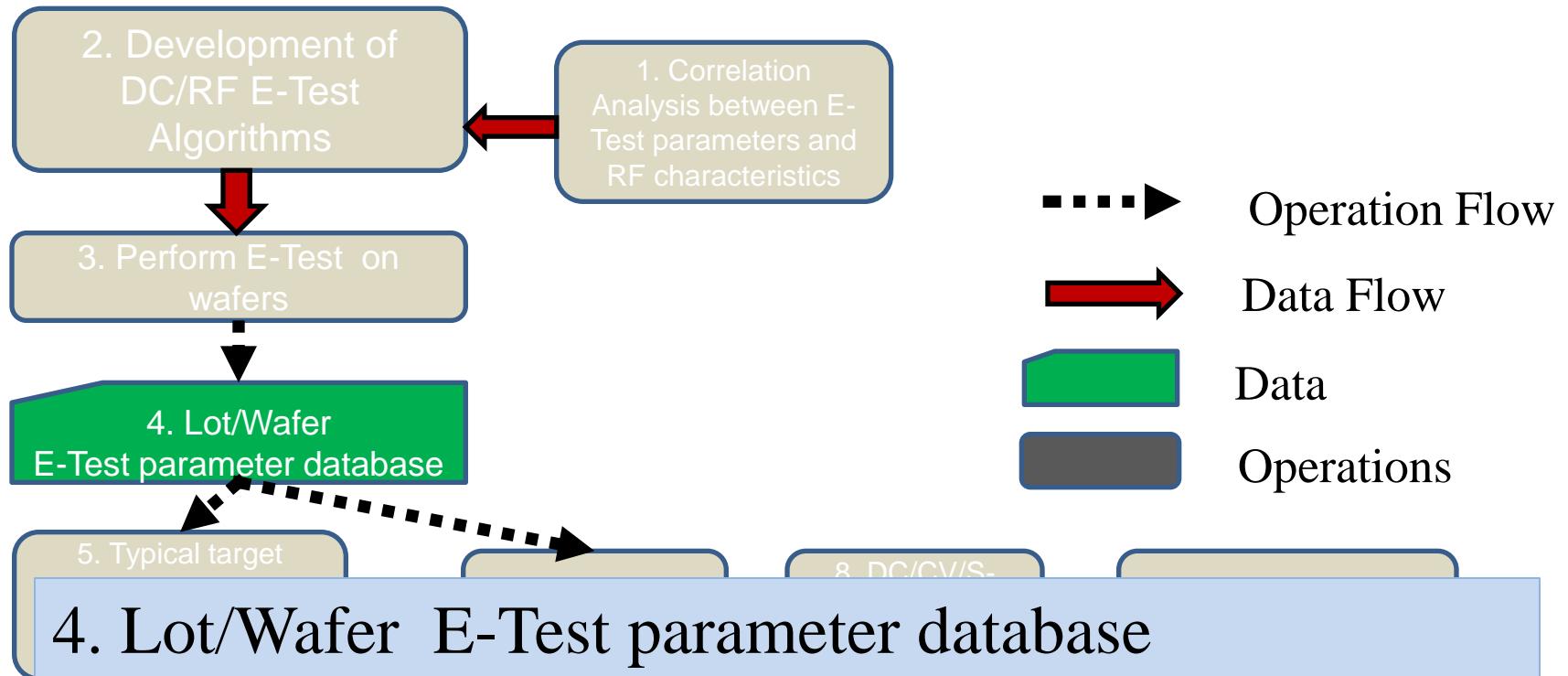
Typical Target Skewing Flow (2)



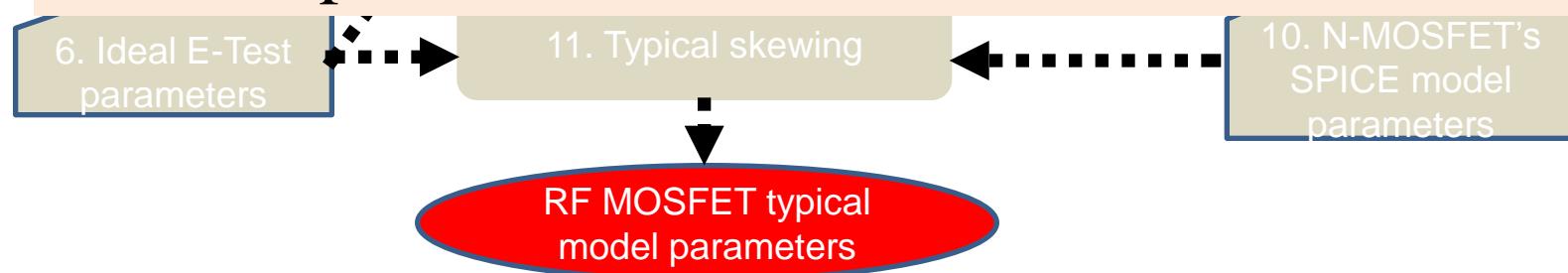
Typical Target Skewing Flow (3)



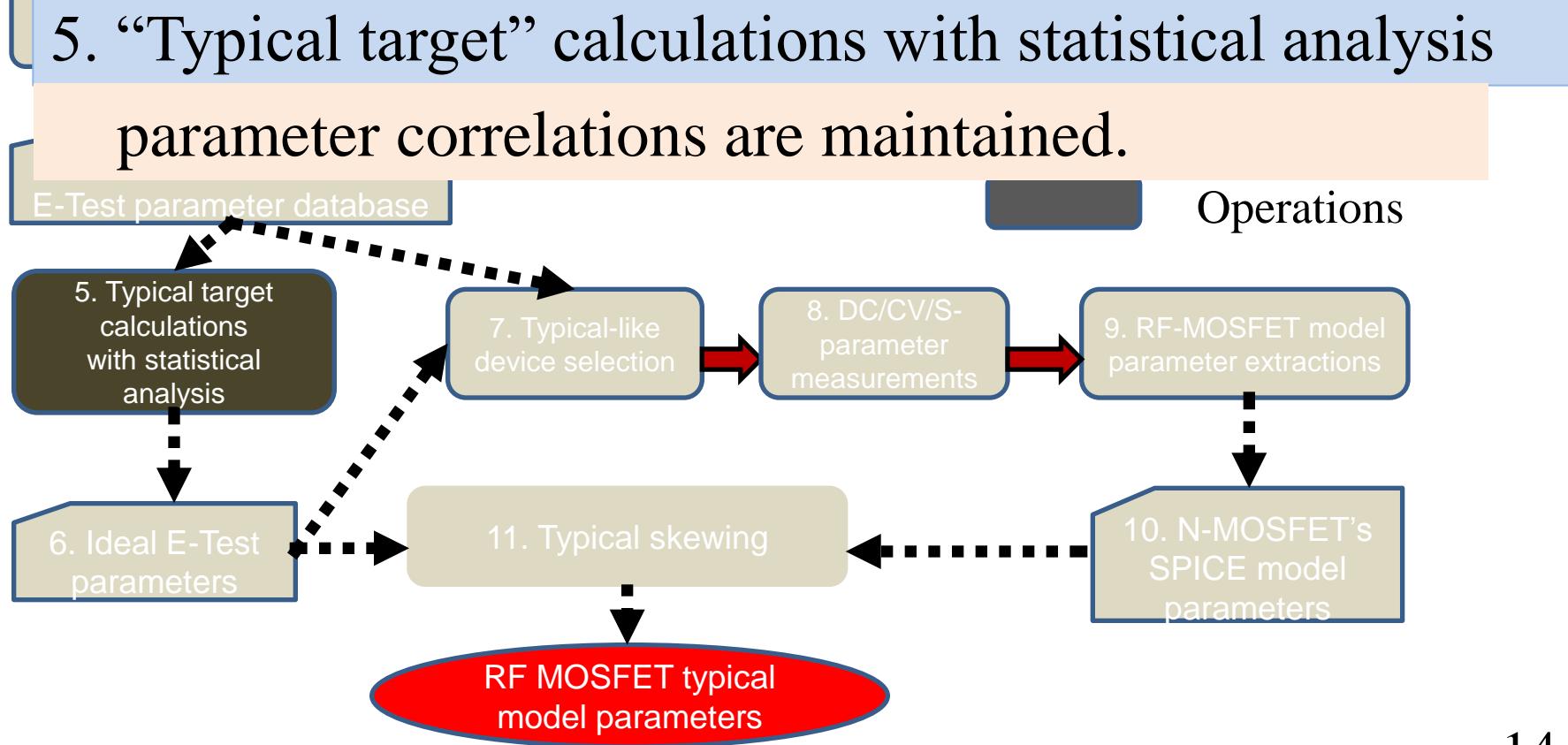
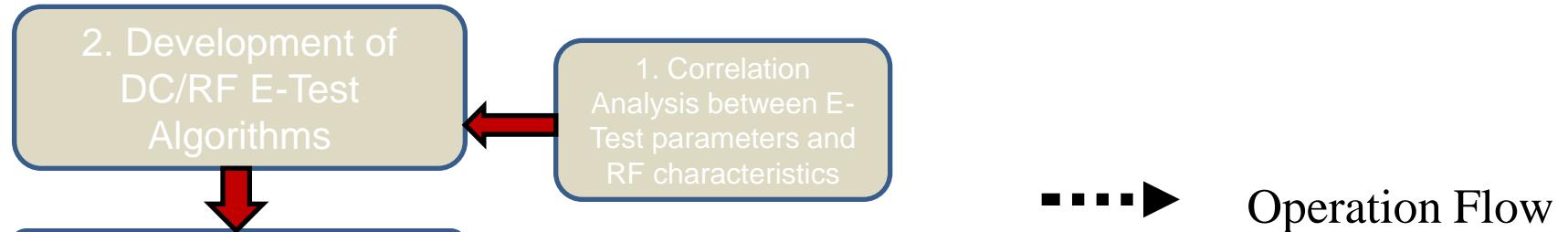
Typical Target Skewing Flow (4)



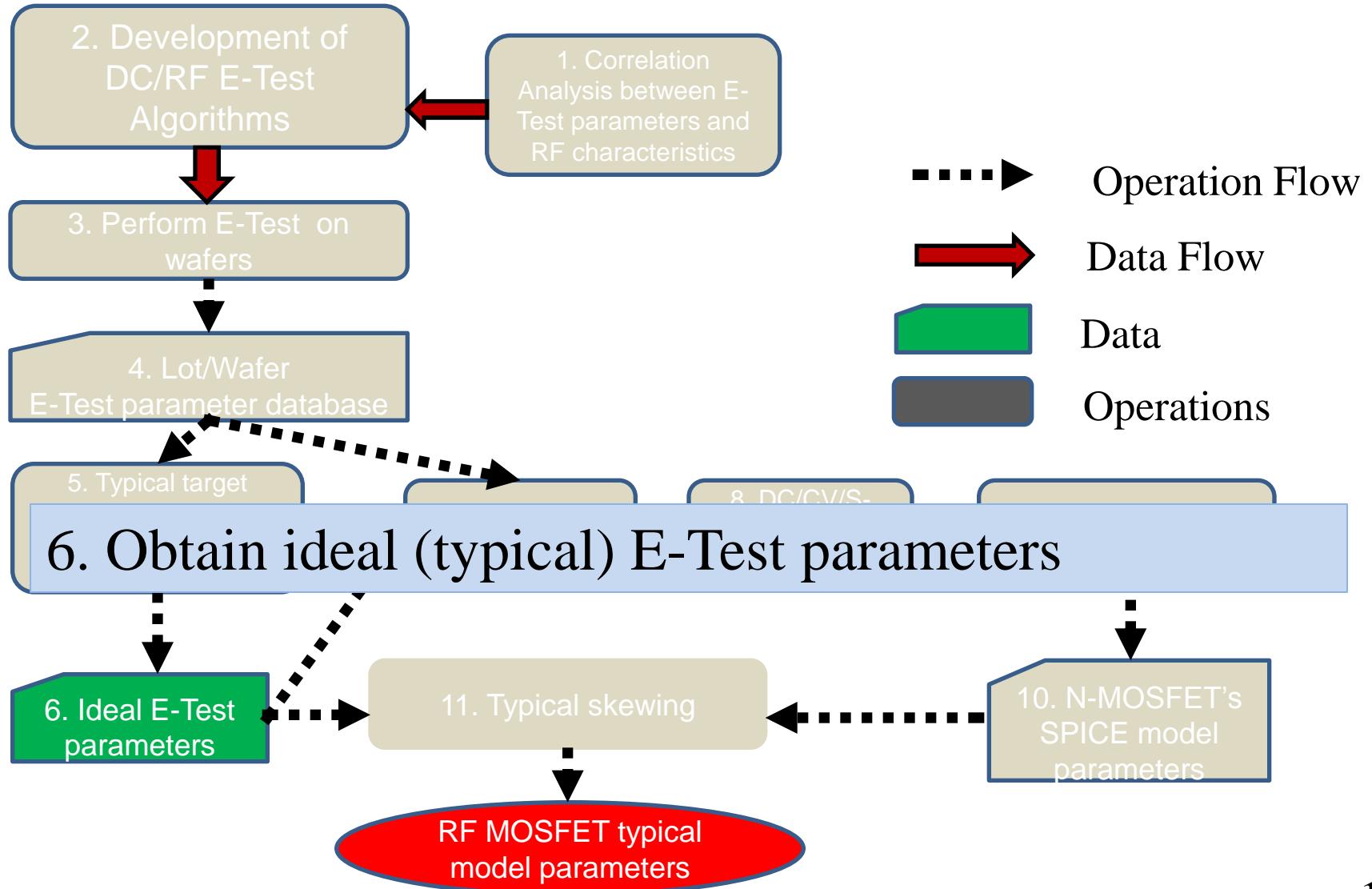
E-Test parameters are stored in.



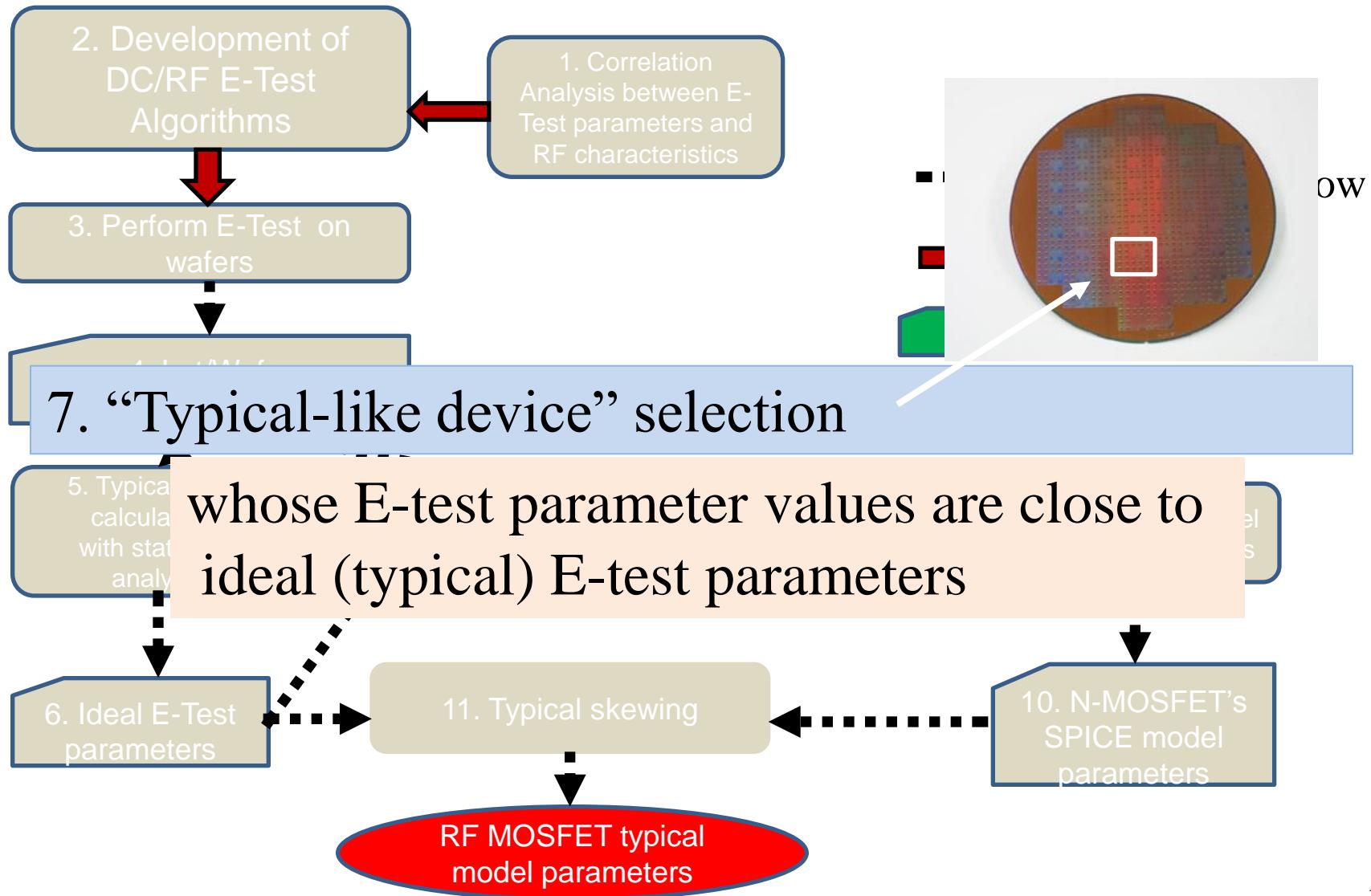
Typical Target Skewing Flow (5)



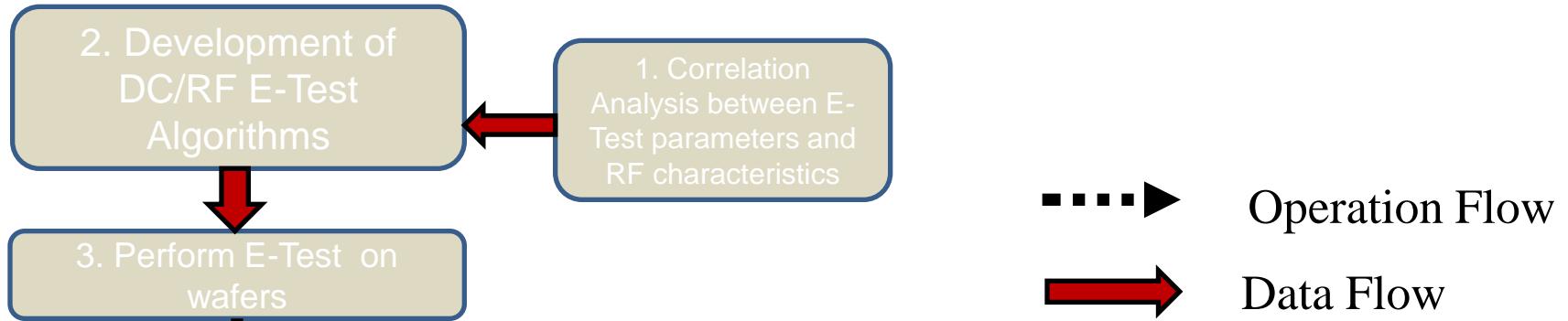
Typical Target Skewing Flow (6)



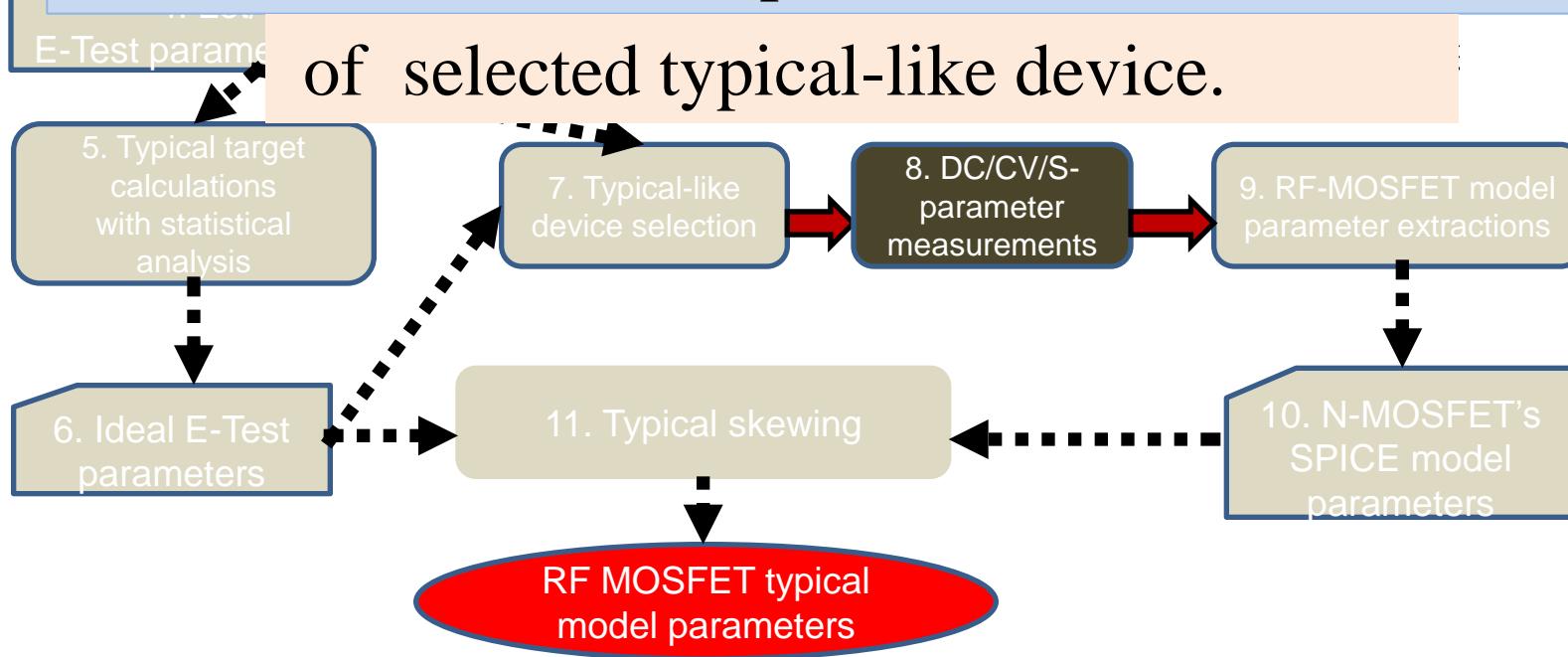
Typical Target Skewing Flow (7)



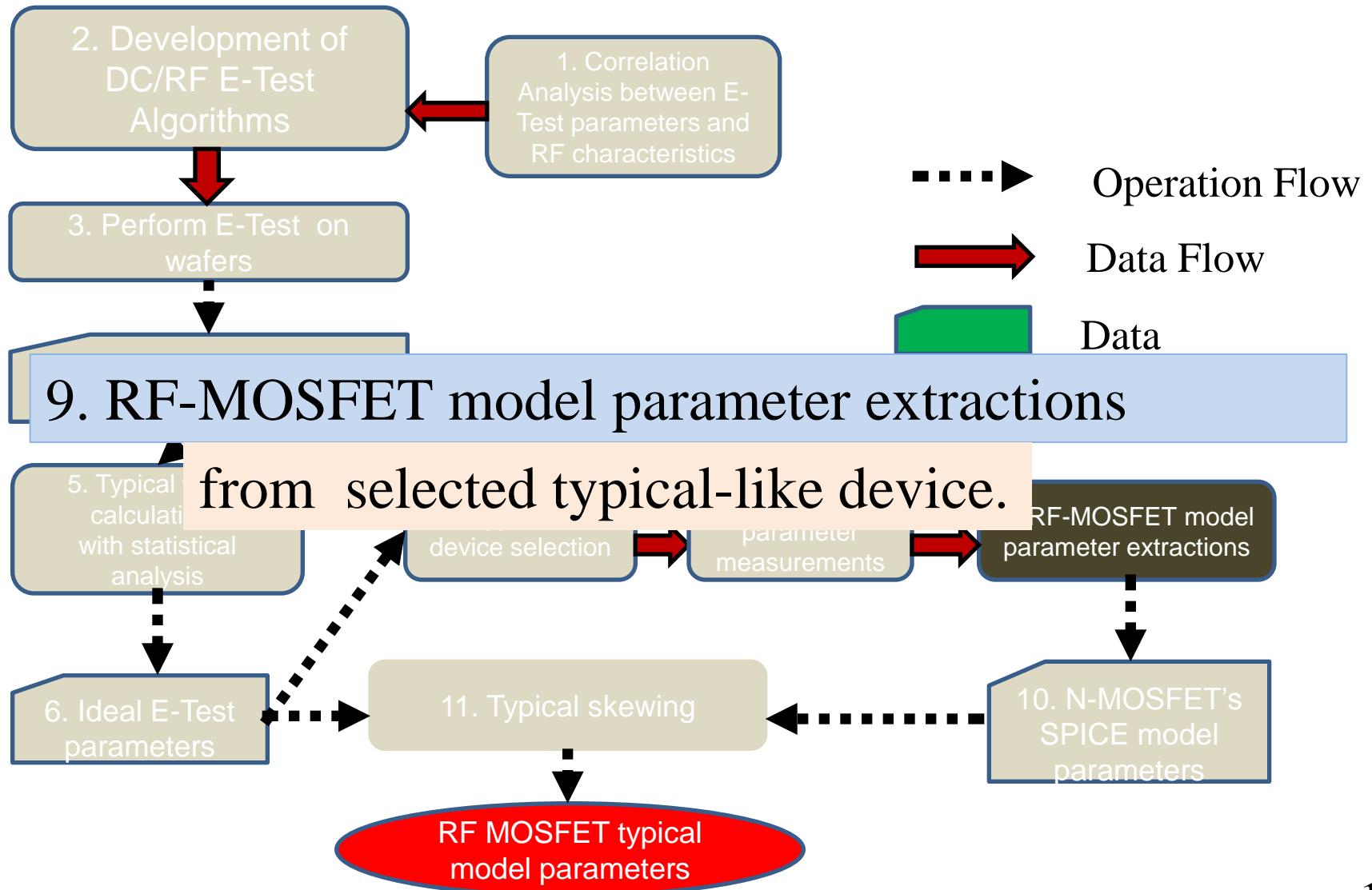
Typical Target Skewing Flow (8)



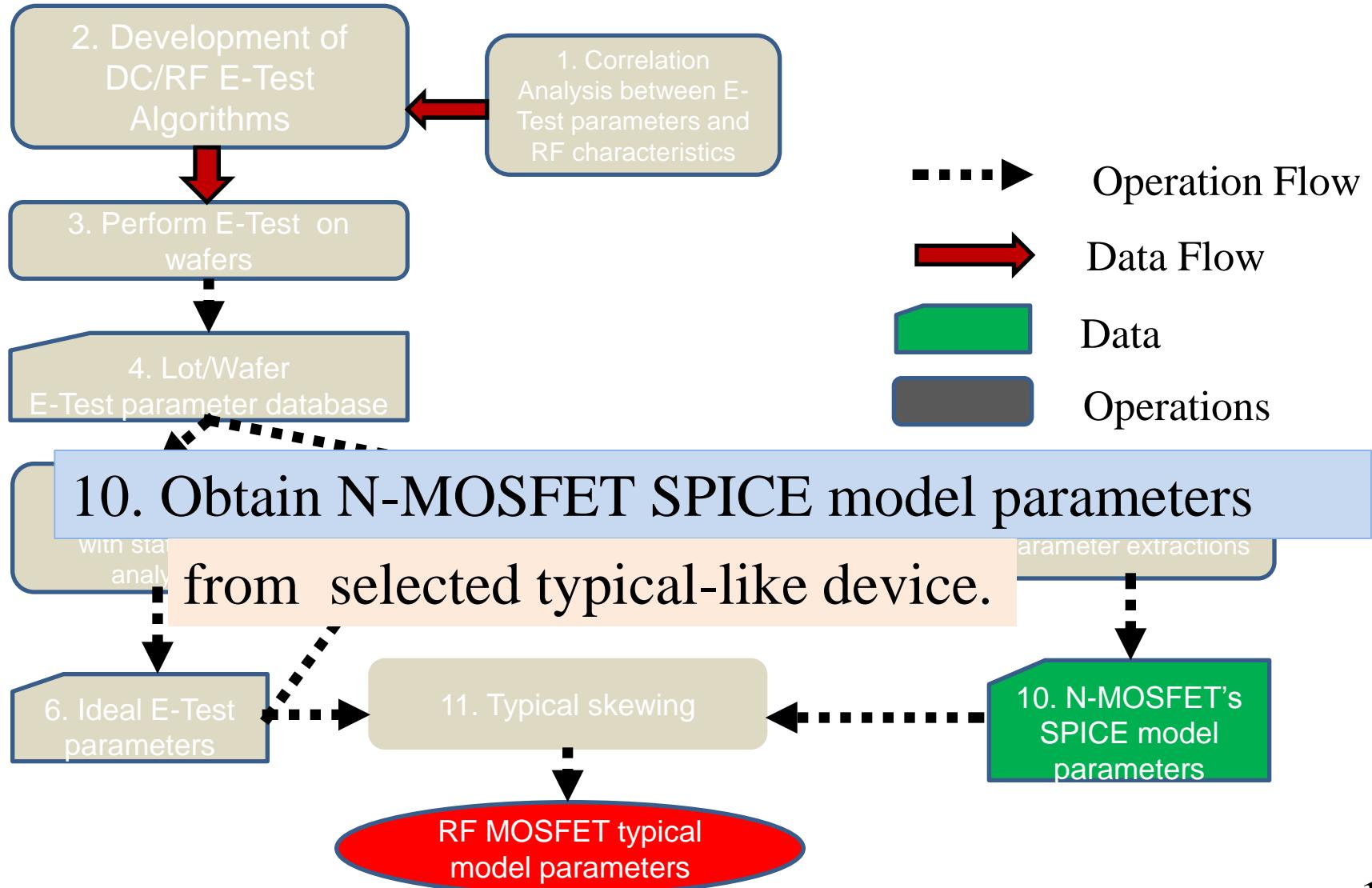
8. Detailed DC/ CV/ S-parameter measurements



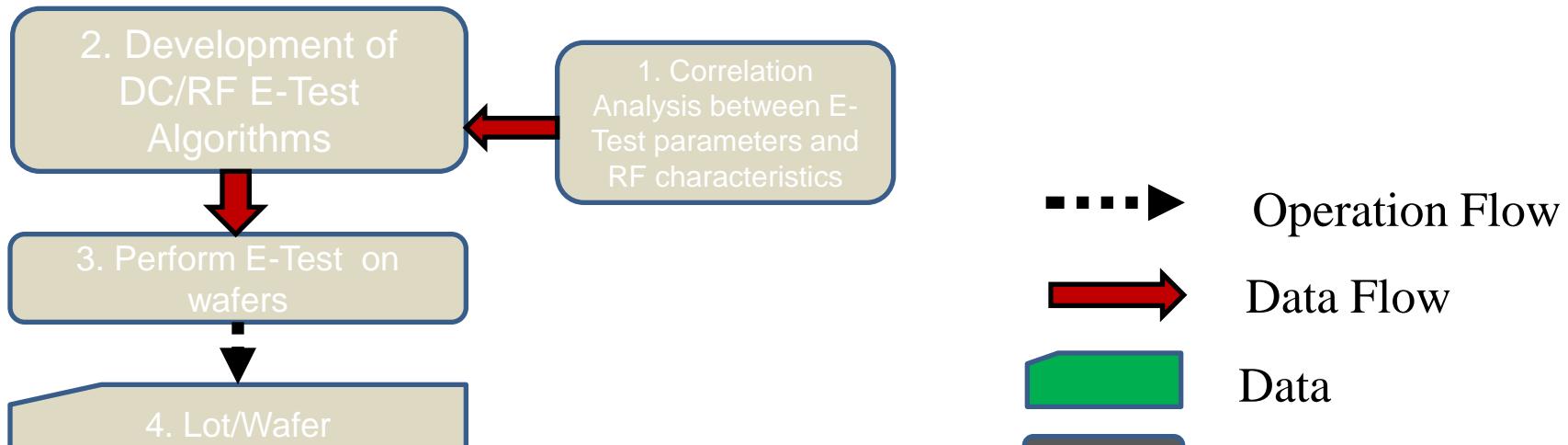
Typical Target Skewing Flow (9)



Typical Target Skewing Flow (10)



Typical Target Skewing Flow (11)

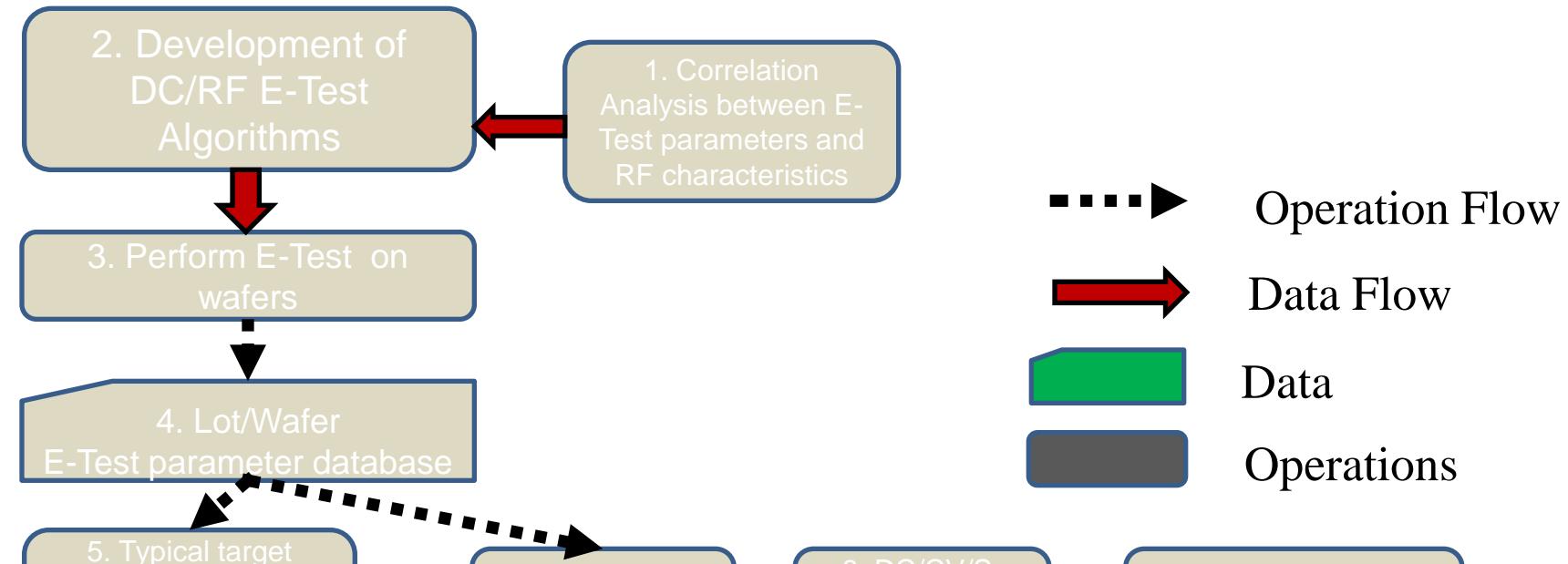


11. Typical skewing

- N-MOSFET SPICE model parameters of typical-like device are skewed to match ideal (typical) E-parameters.
- Correlation among parameters is maintained.

RF MOSFET typical model parameters

Typical Target Skewing Flow (Final)



RF MOSFET BSIM4 typical model parameters are obtained

Any submicron SPICE model as well as BSIM4
can be used for our skewing method.

parameters

RF MOSFET typical
model parameters

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Calculations of Theoretical Target Specifications

- Development of E-Test parameters
 - Modifications, additions of test specifications, algorithms from PCM (Process Control Monitor)
 - **RF model** definitions
 - RF E-Test parameter inclusions
- Statistical analysis for typical parameter calculations
 - E-Test executions, E-Test parameter screening with statistical functions
 - **Correlation analysis** to maintain the relationships between E-Test parameters

RF NMOS Model Definition and Parameters

- KAIST small signal equivalent circuit [1]

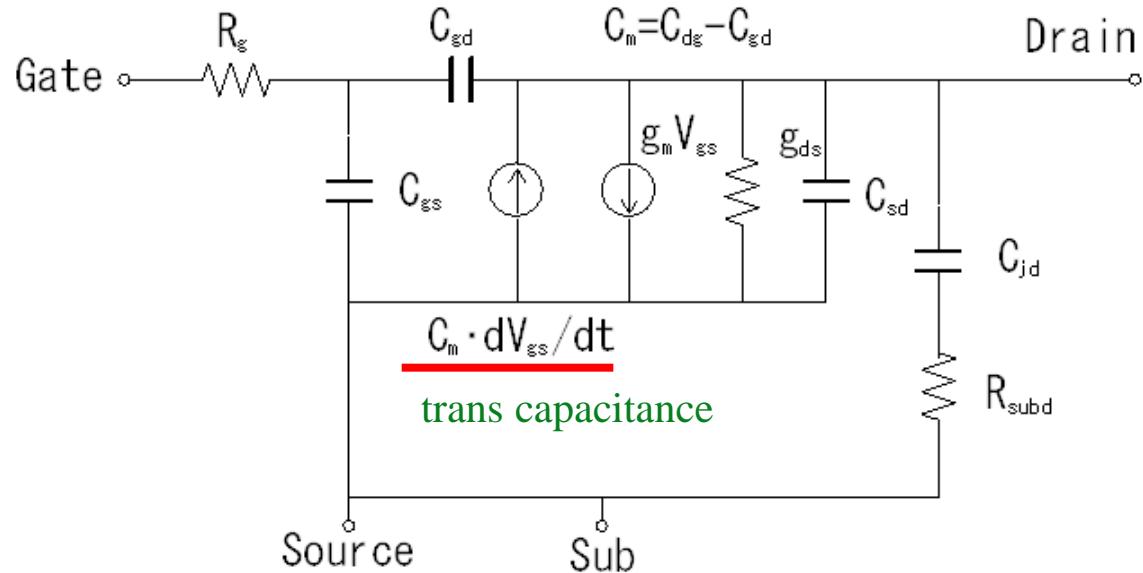
- S-parameters

↓
easy to convert

Y-parameters

$$Y_{11} = \frac{j\omega \left(\underline{C}_{gs} + \underline{C}_{gd} \right)}{1 + j\omega \left(\underline{C}_{gs} + \underline{C}_{gd} \right) R_g} \quad Y_{12} = -\frac{-j\omega \underline{C}_{gd}}{1 + j\omega \left(\underline{C}_{gs} + \underline{C}_{gd} \right) R_g} \quad Y_{21} = \frac{\underline{g}_m - j\omega \underline{C}_m - j\omega \underline{C}_{gd}}{1 + j\omega \left(\underline{C}_{gs} + \underline{C}_{gd} \right) R_g}$$

$$Y_{22} = \underline{g}_{ds} + \frac{j\omega \underline{C}_{jd}}{1 + j\omega \underline{C}_{jd} R_{subd}} + j\omega \underline{C}_{sd} + j\omega \underline{C}_{gd} + \frac{\omega^2 \underline{C}_{gd} R_g \left(\underline{C}_{gd} + \underline{C}_m \right) + j\omega \underline{g}_m \underline{C}_{gd} R_g}{1 + j\omega \left(\underline{C}_{gs} + \underline{C}_{gd} \right) R_g}$$



[1] I. Kwon, et.al., "A New Small Signal Modeling of RF MOSFETs including Charge Conservation Capacitances," ESSCIRC (Jul. 2000).

E-Test Parameters Used for Typical Device Targeting

New
algorithm
for
calculation

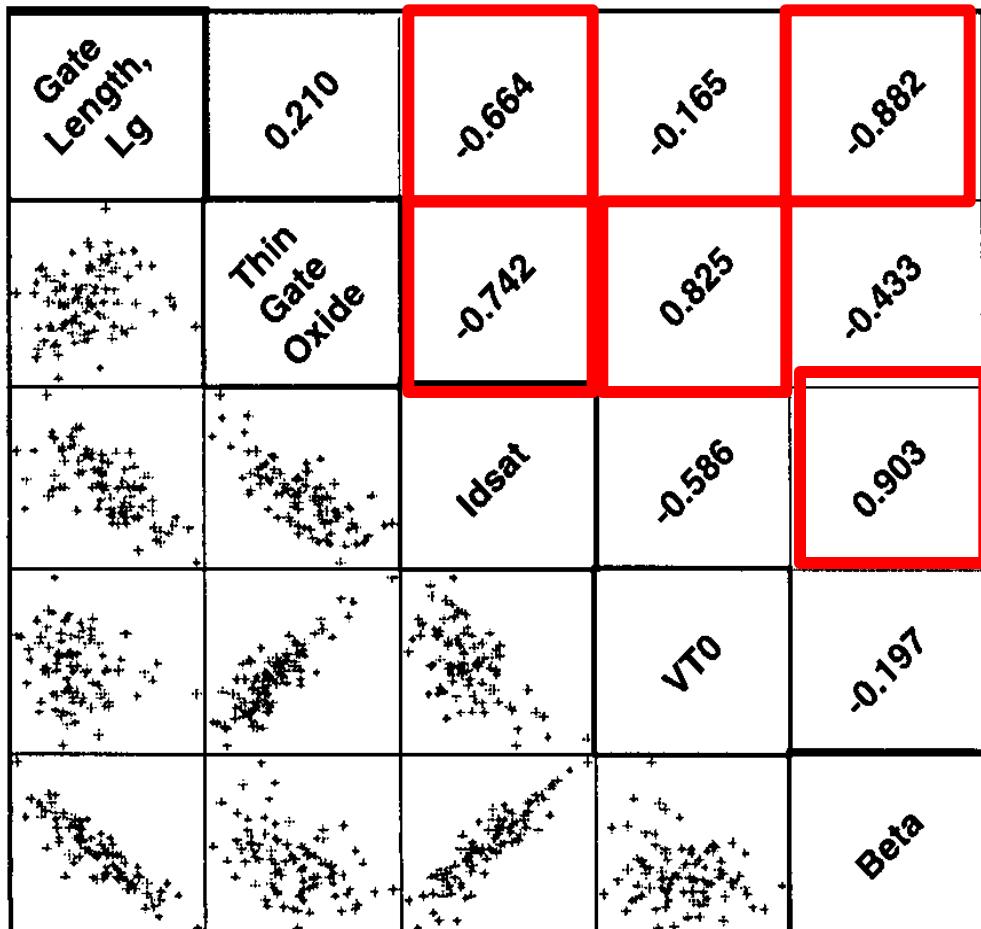
New
parameters
as E-Test

E-Test Parameter	Meanings
TOX	Oxide thickness
LD	Diffusion length
WD	Diffusion width
Idsat	Saturation current
Gmax	Maximum conductance
Beta	Slope of Ids-Vgs Plot
Rcon	Contact resistance
Rdiff	Diffusion resistance
VTO	Threshold voltage
COV	Overlap capacitance
CJ	Area Junction capacitance
CJW	Perimeter Junction capacitance

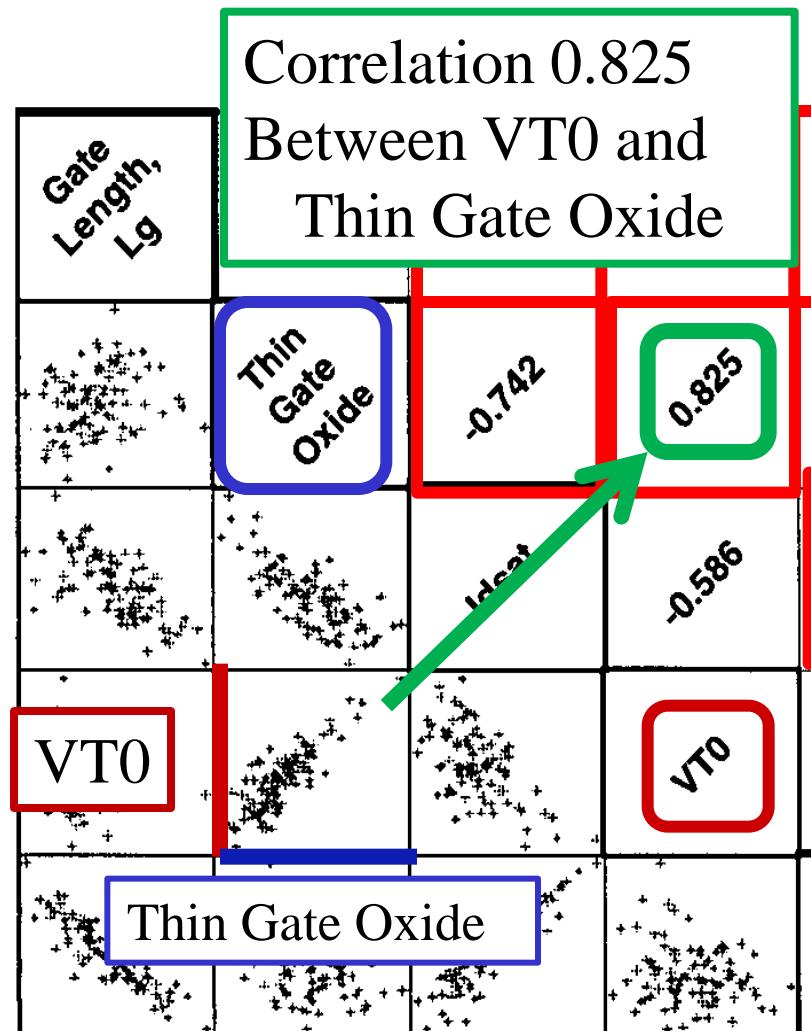
Conventional E-test parameters were only for DC.

Correlation Analysis of E-Test Parameters

Correlation Matrix



Correlation 0.825
Between VT0 and
Thin Gate Oxide



- Their correlation represents device process.
- Correlation > 0.6 should be maintained for statistical modeling. 26

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Target Device Selection and Its Modeling

Calculated ideal (typical)
E-Test parameters

Typical Target Parameters.

VT0.Short = 4.545e-001
BETA.Short = 1.369e+004
Idsat.Short = 6.109e-003
VT0.Large = 2.423e-001
BETA.Large = 2.833e+002
GMMAX.Large = 9.312-006
Idsat.Large = 2.612e-004
VT0.Narrow = 1.484e-001
BETA.Narrow = 5.766e+000
Idsat.Narrow = 6.127e-006
TOX = 2.751e-009
Rcon = 6.211e+000
Rdiff = 2.122e+000
DL = 7.6433e-008
DW = 8.7021e-008
COV = 2.453e-012
CJ = 3.812e-012
CJW = 5.146e-012



Extracted BSIM4 parameters
of selected “typical-like device”

Typical-like Device

Device (No:12) --- wafer_no.: 5

shot_no.: 1 x: 7 y: 4

VT0.Short:	0.465	TOX:	2.711e-009
VT0.Short Error:	2.306211 %	TOX Error:	1.450000 %
BETA.Short:	13500	Rcon:	6.2e-006
BETA.Short Error:	1.382729 %	Rcon Error:	1.192038 %
Idsat.Short:	0.00599	Rdiff:	6.2e-006
Idsat.Short Error:	1.943933 %	Rdiff Error:	1.192038 %
VT0.Large:	0.242	DL:	7.5233e-008
VT0.Large Error:	0.125286 %	DL Error:	1.570000 %
BETA.Large:	283	DW:	8.7661e-008
BETA.Large Error:	0.088261 %	DW Error:	0.007400 %
GMMAX.Large:	9.300-006	COV:	2.491e-012
GMMAX.Large Error:	0.092261 %	COV Error:	1.549112 %
Idsat.Large:	0.000261	CJ:	3.805e-012
Idsat.Large Error:	0.075203 %	CJ Error:	0.183612 %
VT0.Narrow:	0.147	CJW:	5.124e-012
VT0.Narrow Error:	0.974377 %	CJW Error:	0.427532 %
BETA.Narrow:	5.79	*****	*****
BETA.Narrow Error:	0.408770 %	Average Error:	1.126090 %
Idsat.Narrow:	6.2e-006		
Idsat.Narrow Error:	1.192038 %		

There are discrepancies and skewing is needed.

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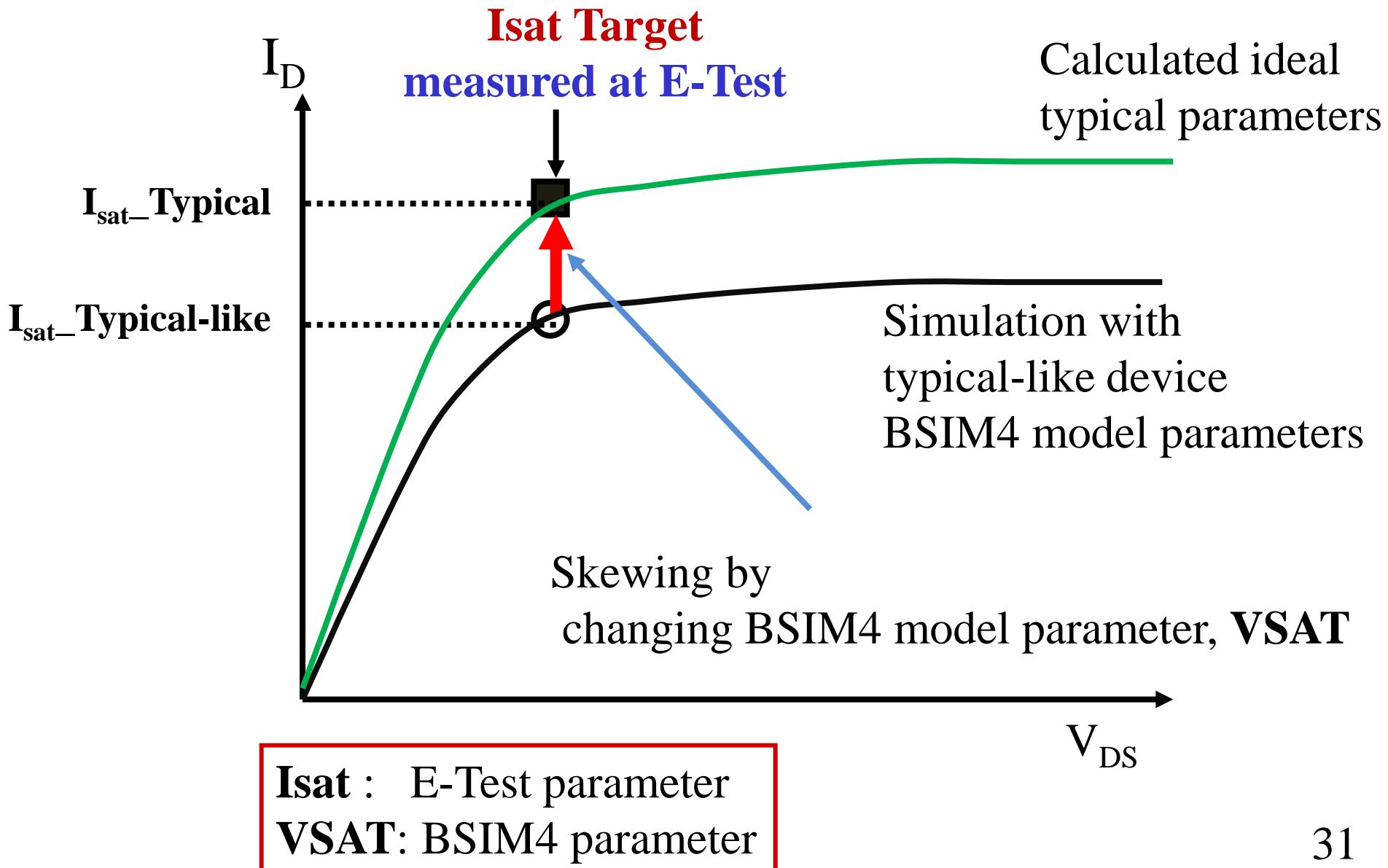
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BSIM4 Model Parameter Skew to Typical E-Test Parameters

Skewing Conditions

- Model parameters should be
 - physical
 - process oriented.
- Slope of I/V or CV should NOT be
 - changed drastically
 - by skewing model parameters

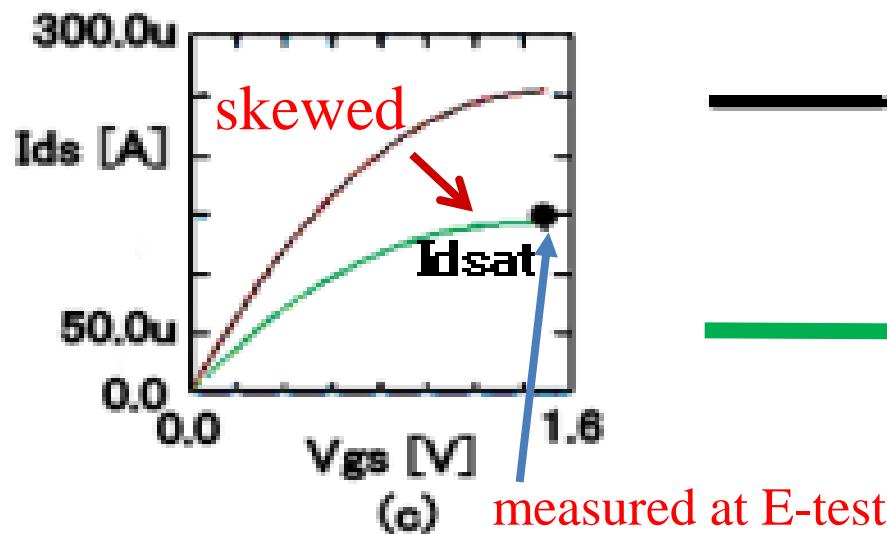
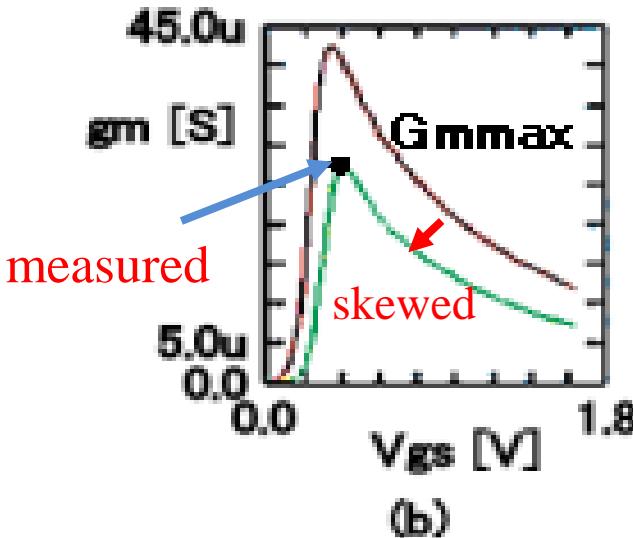
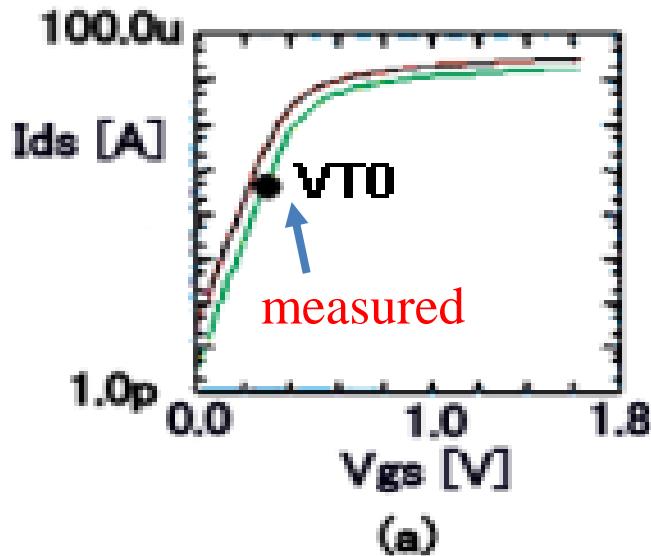
Skewing Concept with VSAT



E-Test Parameters for Target and BSIM4 Model Parameters for Skew

Type of the simulation	E-Test parameter as targets	BSIM4 Model parameters for skewing
I_{DS} vs. V_{GS}	VT0.Large	VTH0
g_m vs. V_{GS}	GMMAX.Large, BETA.Large	UA
I_{DS} vs. V_{GS}	VT0.Narrow	K3, WINT, DVT0W
I_{DS} vs. V_{GS}	VT0.Short	DVT0
I_{DS} vs. V_{DS}	Idsat.Large	U0
I_{DS} vs. V_{DS}	Idsat.Narrow	WINT
I_{DS} vs. V_{DS}	Idsat.Short	VSAT, LVSAT
C_{GC} vs. V_{GC}	COV	CGS0 (=CGD0), CGSL (=CGDL)
C_J vs. V_J	CJ.area	CJ0
C_J vs. V_J	CJ.perim	CJSW

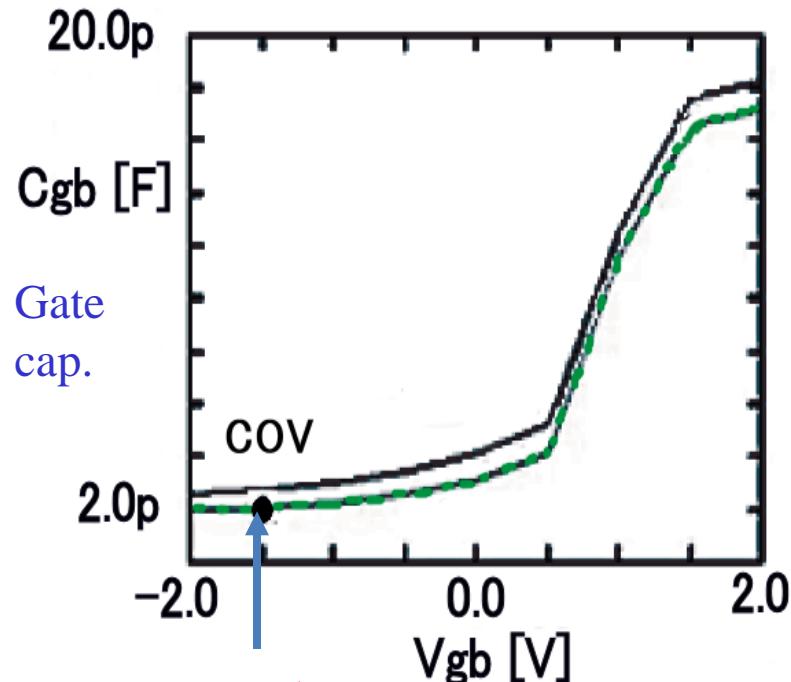
Examples of DC Parameters Skew



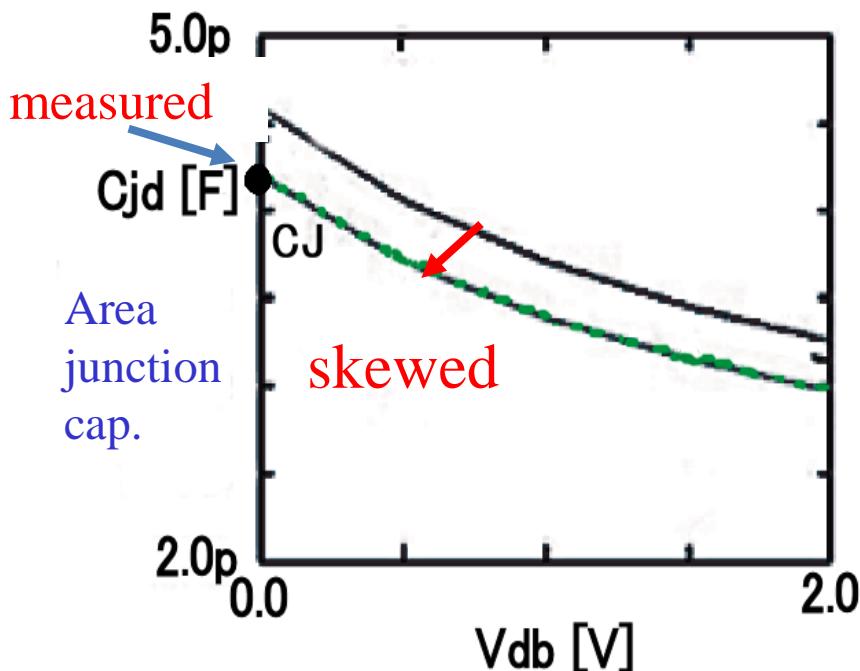
— Typical-like model
from selected device

— Skewed typical model

Examples of CV Parameters Skew



Measured
at E-test



Typical-like model
from selected device

Skewed typical model

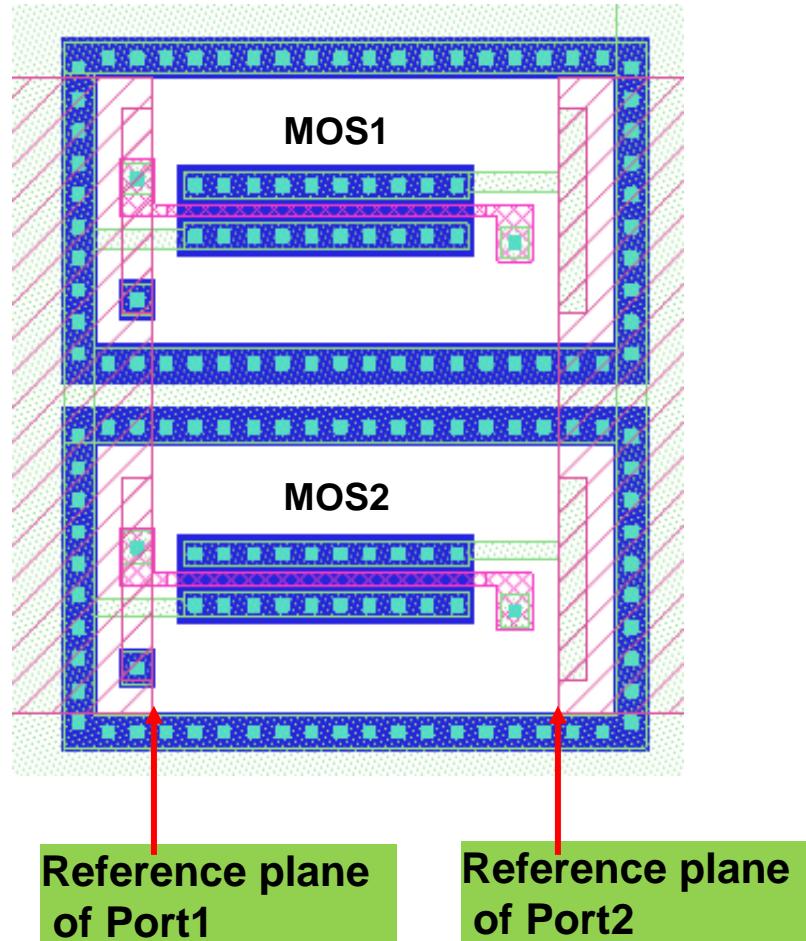
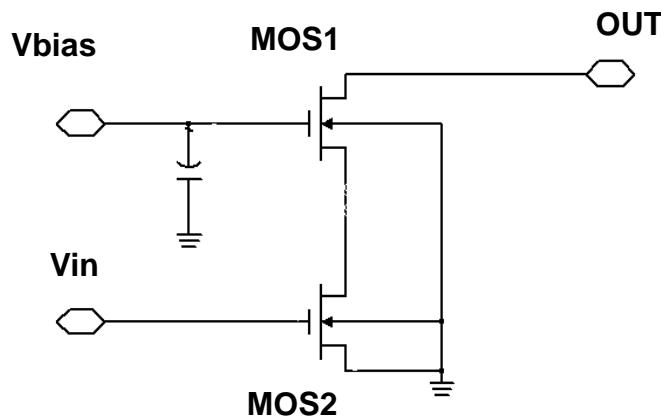
Useful for RF design

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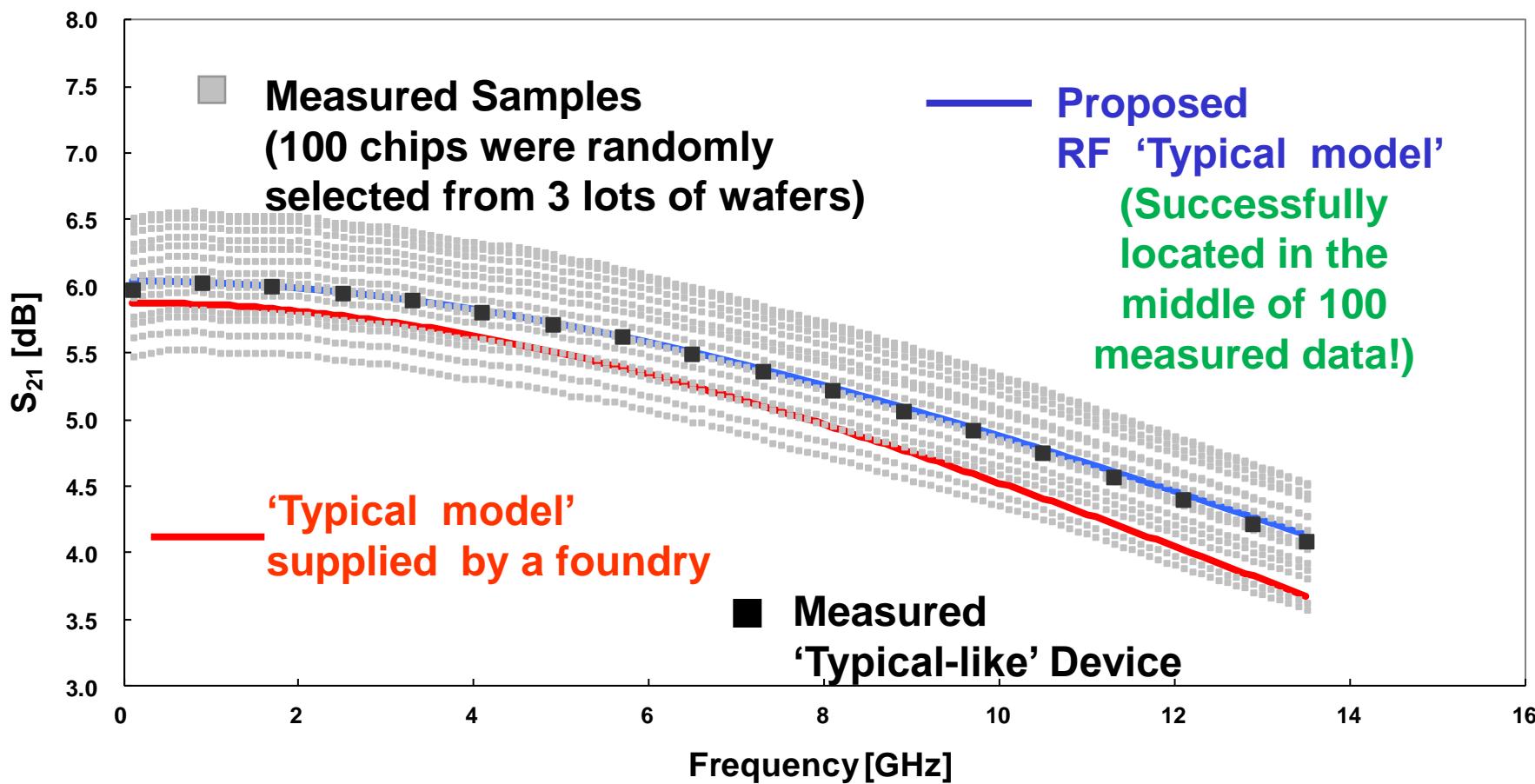
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Verifications of RF Circuit Simulations

A cascode amplifier
for verification



Measurement and Simulation Results of S_{21} Dependencies on Frequency of Cascode Amplifier



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Conclusions

- A new procedure of NMOS typical target and a skewing method for RF analog applications were demonstrated.
 - RF NMOS typical targeting results were examined with a simple cascode amplifier designed and fabricated in our TEG.
 - Skewed results were located in the middle of randomly measured 100 S_{21} data.
 - This typical model generation method practical, useful for CMOS circuit designer.
- 
- 