BRIEF PAPER *Special Section on Analog Circuits and Related SoC Integration Technologies*

A Feed-Forward Time Amplifier Using a Phase Detector and Variable Delay Lines

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SUMMARY This paper describes a high-speed, robust, scalable, and low-cost feed-forward time amplifier that uses phase detectors and variable delay lines. The amplifier works by detecting the time difference between two rising input edges with a phase detector and adjusting the delay of the variable delay line accordingly. A test chip was designed and fabricated in 65 nm CMOS. The measured resulting performance indicates that it is possible to amplify time difference while maintaining high-speed operation.
key words: *time amplifier, feed-forward, CMOS, integrated circuits, design for testability*

1. Introduction

Because of recent advances in VLSI fabrication, time resolution is improving faster than voltage resolution. This trend motivates the development of time-domain processing circuitry.

For instance, a time-domain analog-to-digital converter (ADC) based on the scaled CMOS technology has recently been reported [1]. This time-domain ADC is composed of analog-to-time converters, time amplifiers (TAs), and time-to-digital converters (TDCs). In this architecture, the TA tends to be a performance bottleneck.

There is much recent literature on TA design. Initial open-loop TAs were based on the meta-stability of the NAND SR-latch [2], and used the TA in an all-digital phase locked loop (ADPLL) as a preamplifier of high-resolution TDC [3] and high-resolution jitter measurement [4]. This open-loop structure is simple and has a small footprint; however, its robustness is quite low owing to its use of meta-stability. In order to improve the robustness, several types of TAs including a closed-loop TA [5], a TA with pull-down NAND [6], and a comparator-based TA [7] have been developed. The closed-loop architecture significantly improves robustness, but requires a large footprint. A TA with pull-down NAND has limitations in linearity. A comparator-based TA has large area consumption.

Our proposed technique can overcome these shortcomings. We propose a feed-forward TA comprising a phase frequency detector and variable delay lines (VDLs). A phase frequency detector detects the input time difference, and the detected results are fed forward to the VDL. The VDL is adjusted to achieve time amplification depending on the detected input time difference and designed gain. The latter signal is delayed by the VDL, leading to time amplification.

This paper is organized as follows. Section 2 introduces the design of the feed-forward TA. Test chip design and measurement setup are shown in Sect. 3. The measurement results are described in Sect. 4. Section 5 concludes the paper.

2. Design of Feed-Forward TA

Figure 1 shows a conceptual representation of the proposed feed-forward TA. The mechanism of time amplification is as follows.

1) Detect which input occurs earlier (*in1* or *in2*) and the input time difference, ΔT
2) Add a delay of $(\alpha - 1)\Delta T$, where α is the gain, to the signal path of the latter input

The above process leads to time amplification. There are two advantages of the proposed scheme: first, feed-forward control contributes to high-speed operation; second, the scheme is scalable because the gain can be easily adjusted by changing the length of the delay cell.

Figure 2 shows the schematic of the proposed feed-forward TA. First, two inputs are fed into the phase frequency detector. The phase frequency detector generates the pulse-width modulation (PWM) signal for controlling the VDL. The delay value of the VDL is set to $(\alpha - 1)\Delta T$. A fixed delay line (FDL) is also implemented for adjusting timing relationship between the input signals and the control signals. This structure has the advantage of scalability.

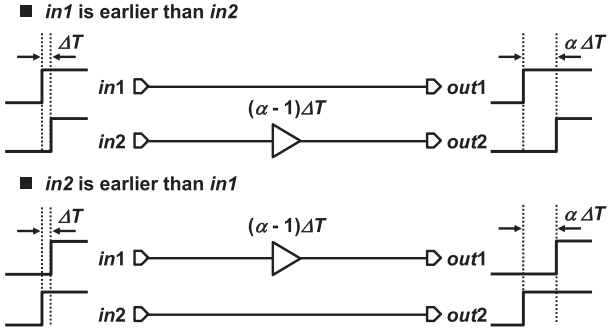

Fig. 1 Conceptual representation of the proposed feed-forward TA.

Manuscript received October 29, 2012.
Manuscript revised January 28, 2013.
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DOI: 10.1587/transele.E96.C.920

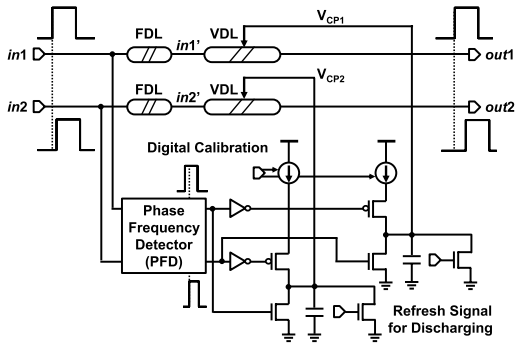

Fig. 2 Schematic of the proposed feed-forward TA.

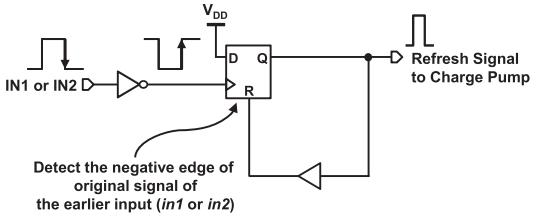

Fig. 3 Schematic of the circuit for generating refresh signal.

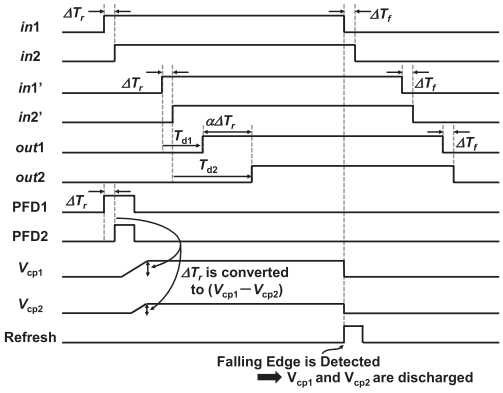

Fig. 4 Timing diagram of the proposed feed-forward time amplifier.

By changing the position of the VDL tapping, the gain can easily be reconfigured.

By adopting digital calibration in charge pumps, high robustness can be achieved. In order to change the control voltage of the VDL for each amplification, a refresh signal for discharging the capacitors is required. The refresh signal enables amplification of the time difference of only the rising edges.

Figure 3 shows the schematic of the circuit for generating the refresh signal. In this circuit, a flip flop detects the negative edge of the original signal (marked by arrows in Fig. 3) that arrives earlier (*in1* or *in2*) and generates the pulse signal for the input of the charge pumps.

Figure 4 shows the timing diagram of the proposed feed-forward time amplifier. Each signal corresponds to that in Fig. 2. Only the time differences of the rising edges are amplified. By refreshing the control voltages for VDLs, V_{CP1} and V_{CP2}, after amplification of the time difference of the rising edges, the time difference of the falling edges are not amplified.

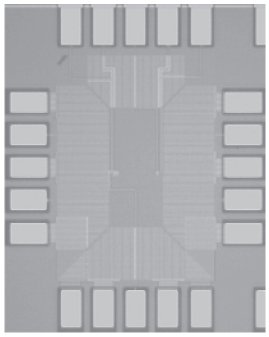

Fig. 5 Test chip microphotograph (65 nm CMOS technology, 1.2 V power supply).

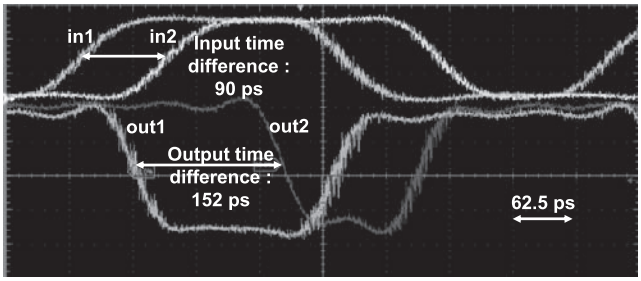

Fig. 6 Measured input and output waveforms demonstrating time amplification. Output signals were inverted due to measurement setup and chip implementation.

3. Test Chip Design and Measurement Setup

A test chip implementing the proposed TA was designed and fabricated in 65 nm CMOS process. Figure 5 shows a microphotograph of the chip. The chip occupies an area of 650 μm^2 (10 μm $\times$ 65 μm). Its power consumption is 6.38 mW when operating at 3.36 GHz operation with a 1.2 V power supply.

Measurement was performed by manual probing. A high-speed signal was provided by an AC probe (Cascade Microtech, Inc., Infinity Probe) and power and controls were provided by a DC probe (Cascade Microtech, Inc., Eyepass Probe).

4. Measurement Results

4.1 Measured Operational Speed

Figure 6 shows the measured input and output waveforms captured by a sampling oscilloscope. The signals demonstrate approximately 1.7$\times$ time amplification. Output signals were inverted due to measurement setup and chip implementation.

Figure 7 shows the measured input and output waveforms for high-speed operation. As shown in this figure, 3.36 GHz operation was successfully achieved. Output sig-

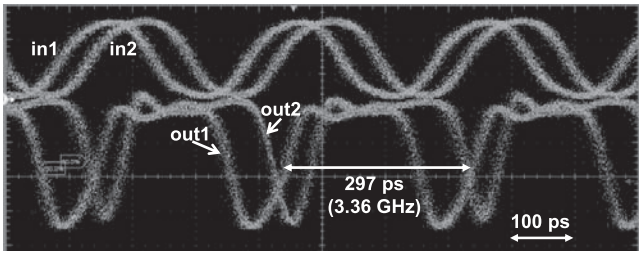

Fig. 7 Measured input and output waveforms demonstrating high-speed operation. Output signals were inverted due to measurement setup and chip implementation.

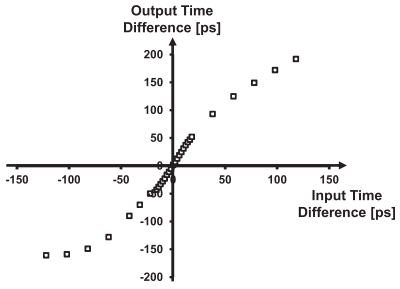

Fig. 8 Measured output time difference dependence on input time difference at full range.

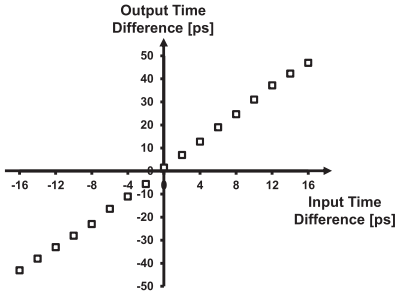

Fig. 9 Measured output time difference dependence on input time difference in linear region.

nals were inverted due to measurement setup and chip implementation.

4.2 Measured Gain and Linearity

The relationship between input and output time difference at 2 GHz across full range is depicted in Fig. 8. An input dynamic range of more than ±100 ps was successfully verified. Because of the device variations in the charge pumps and delay cells, the relationships for positive and negative input are not symmetric.

Figure 9 shows the relationship between input and output time difference in the linear region from −16 ps to +16 ps. The obtained gain is 2.89. The time offset is 1.5 ps, which is acceptably small. Maximum error and root mean square error values are 1.64 ps and 0.73 ps, respectively.

Table 1 Performance comparison.

	JSSC 08 [3]	VLSI 09 [5]	ISSCC 10[6]	ASSCC 11[7]	This Work
Process	90 nm	65 nm	180 nm	130 nm	65 nm
Area	N/A	112700 μm^2	N/A	16900 μm^2	650 μm^2
Gain	20	4.784	2	20.9	2.89
vs. PVT	Weak	Very Robust	Very Robust	Robust	Robust
Speed	10 MHz	100 MHz	1 GHz	550 MHz (2.5 GHz *)	3.36 GHz
DR	40 ps	300 ps	100 ps	2000 ps	50 ps

* : Calculated Result(@ Gain = 4, DR = 50 ps)

4.3 Comparison with Conventional TAs

Table 1 compares the proposed circuit with existing TAs. The proposed feed-forward TA is superior in both speed and size; its operational speed of 3.36 GHz is the highest among all reported TAs.

5. Conclusion

This paper demonstrated a new time amplifier design that lends itself to robust, high-speed operation, and low cost. Time amplification is achieved by detecting and feeding forward the input time difference. The proposed circuit was designed and implemented in a 65 nm CMOS process; the measured results successfully demonstrate 3.36 GHz operation with a gain of 2.89.

Acknowledgments

This work is supported by STARC and VDEC.

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