3rd IEEE International Workshop on Test and Validation of High Speed Analog Circuits
Anaheim, California, USA (Sept. 13, 2013)

Linearity Improvement Techniques of Multi-bit Sigma-Delta TDC for Timing Measurement

Yuta Arakawa, Yusuke Osawa, <u>Haruo Kobayashi</u>
Osamu Kobayashi [†]

Gunma University, STARC [†]
Japan

TDC: Time-to-Digital Converter

Outline

- ► Research Objective
- ► Single-Bit & Multi-bit ΣΔ TDCs
- ► Multi-Bit ΣΔ TDC with DWA
- ► Multi-Bit ΣΔ TDC with Self-Calibration
- ► Multi-Bit ΣΔ TDC with Sorting
- ► Conclusion

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- **Research Objective**
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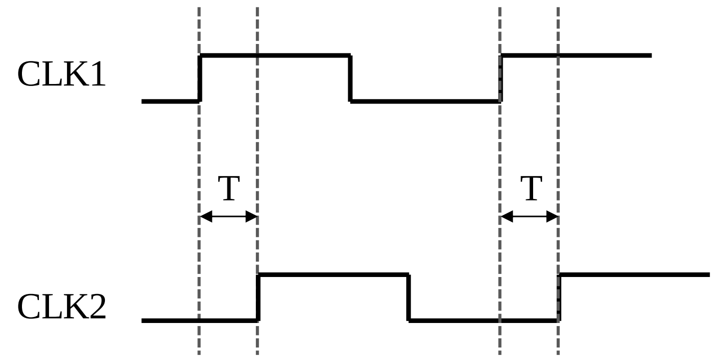
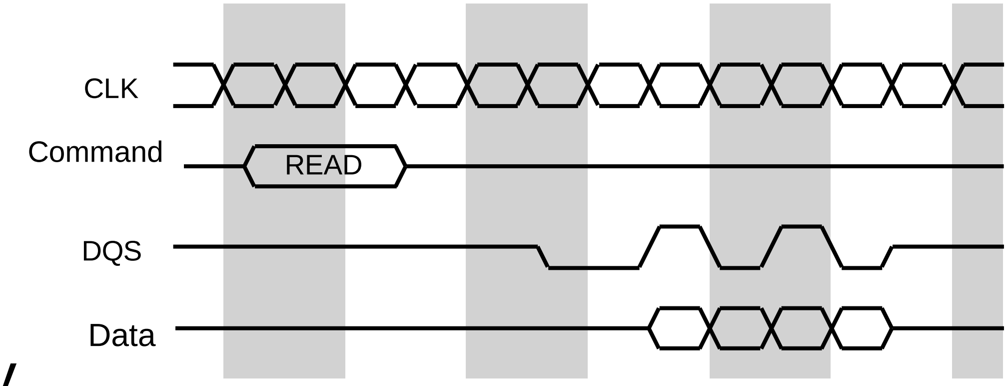
Research Objective

- Testing timing difference between two repetitive digital signals
  Ex.
  Data and clock
  in Double Data Rate (DDR) memory



- Short testing time
- Good accuracy

Implement with small circuitry



Our Work

Focus on Multi-bit ΣΔTime-to-Digital Converter (TDC)

- Repetitive digital signals
  ⇒ ΣΔ TDC can be used
- Simple circuit
- Fine resolution
- Testing time
  - Single-bit ΣΔ TDC Long
  - Multi-bit ΣΔ TDC Short
- Linearity
  - Single-bit ΣΔ TDC Good
  - Multi-bit ΣΔ TDC Bad due to delay elements mismatches

⇓

Three methods for their compensation

→ DWA, Self-calibration, Delay cell sorting

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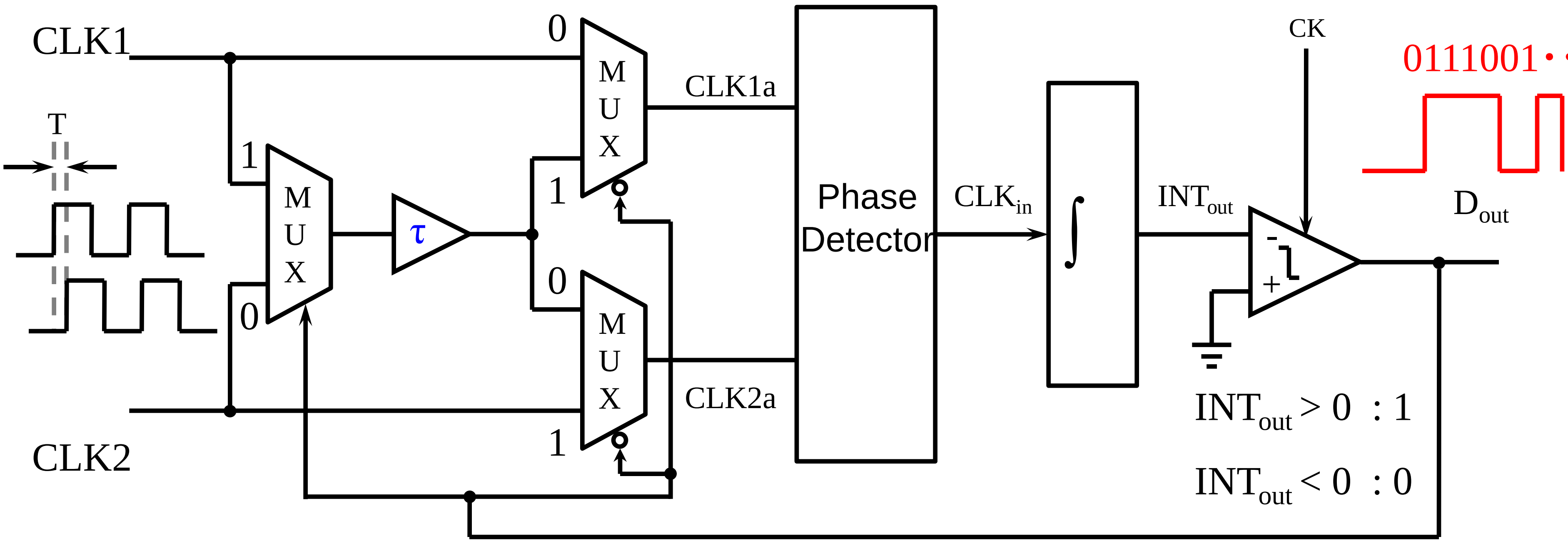
Single-Bit ΣΔ TDC



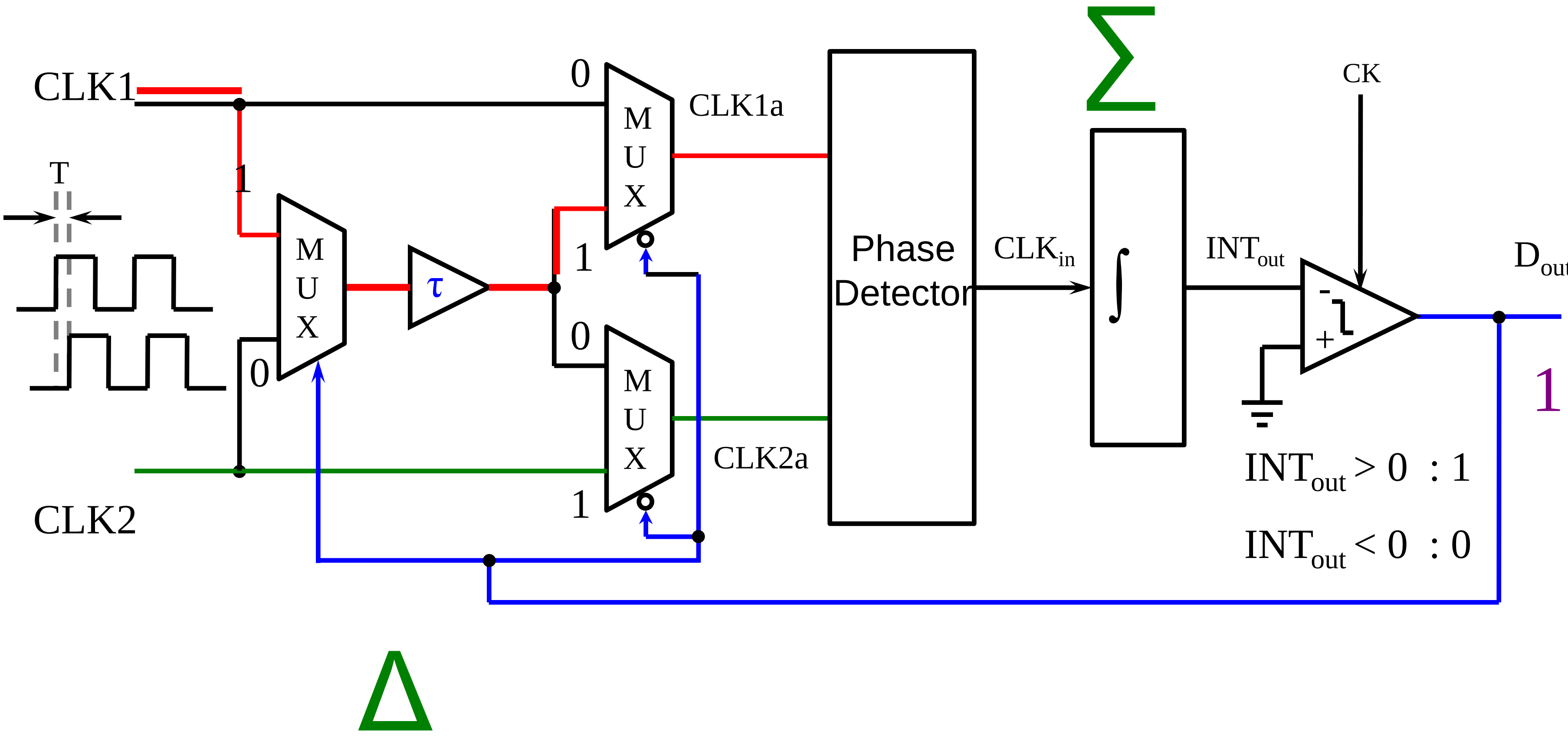
- Measurement of timing *T* between repetitive CLK1 and CLK2
- Number of 1's at *Dout* is proportional to *T*
- Time resolution becomes finer as measurement time becomes longer

Note: τ is not time resolution, but time measurement full range

The delay line with 1bit digital input is inherentlylinear because it is 1-bit.

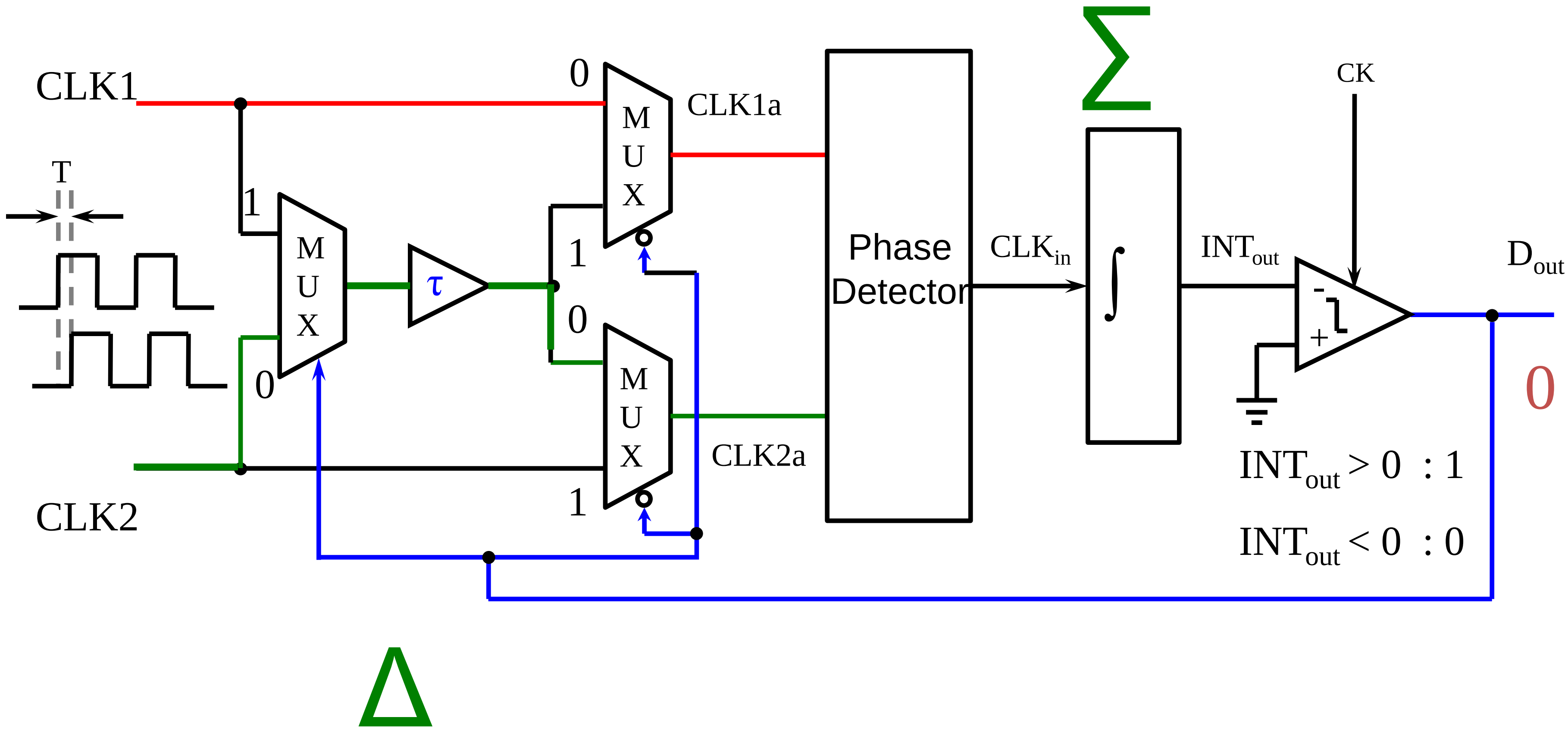
Operation of Single-Bit ΣΔ TDC

In case Dout =1

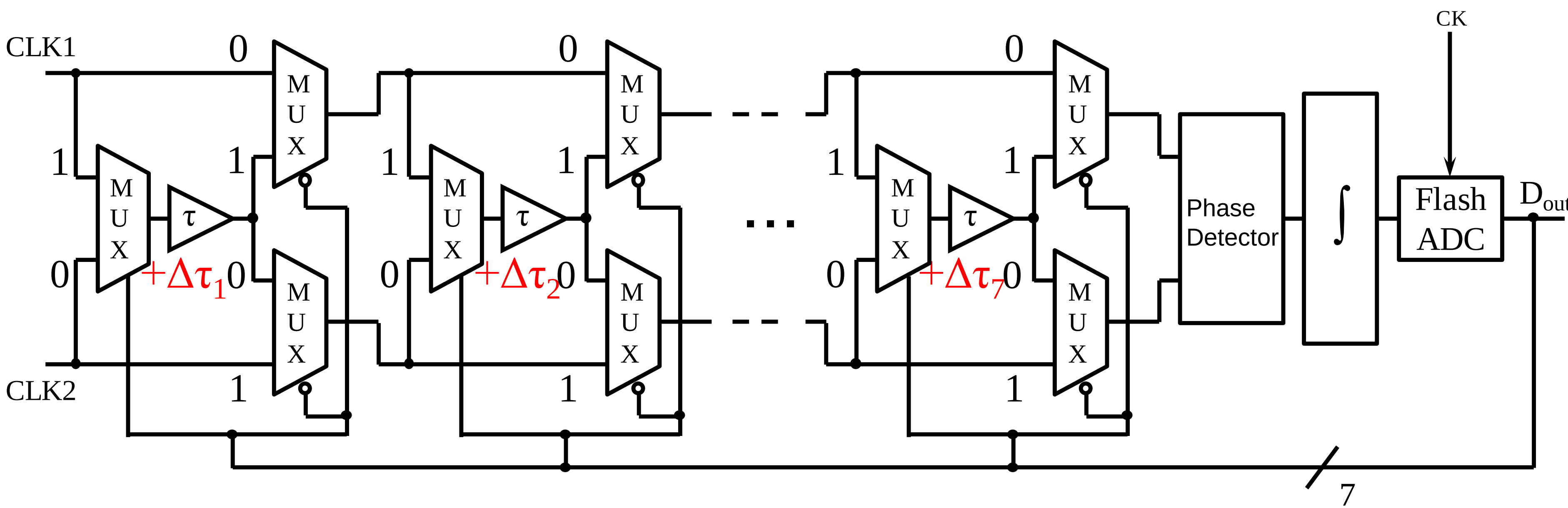


Operation of Single-Bit ΣΔ TDC

In case Dout =0



Multi-Bit ΣΔ TDC



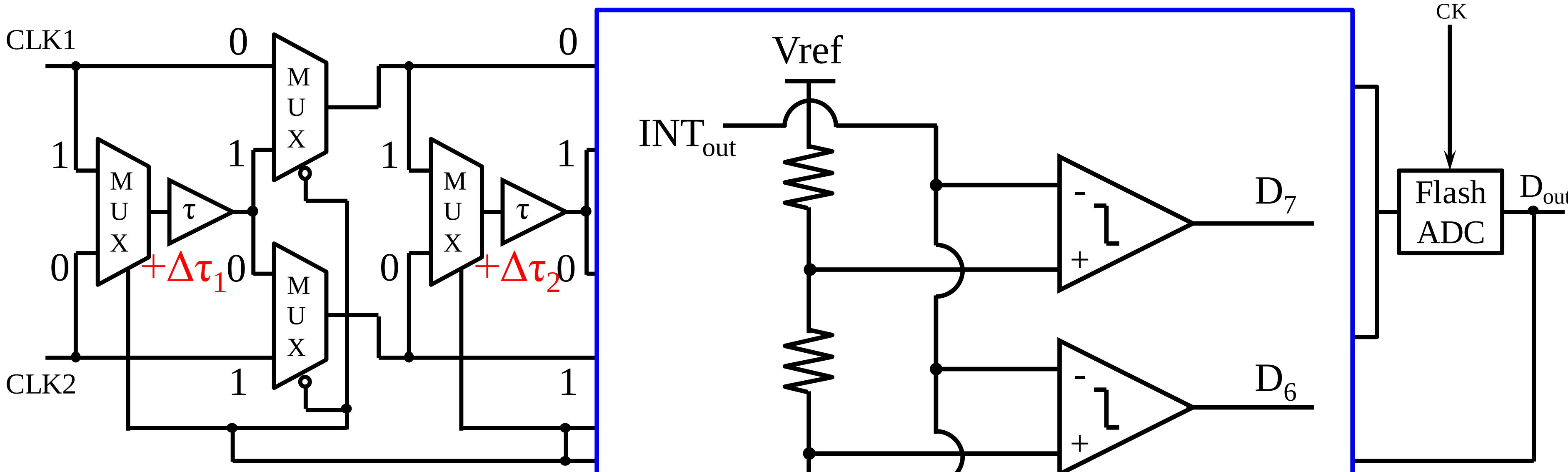
- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

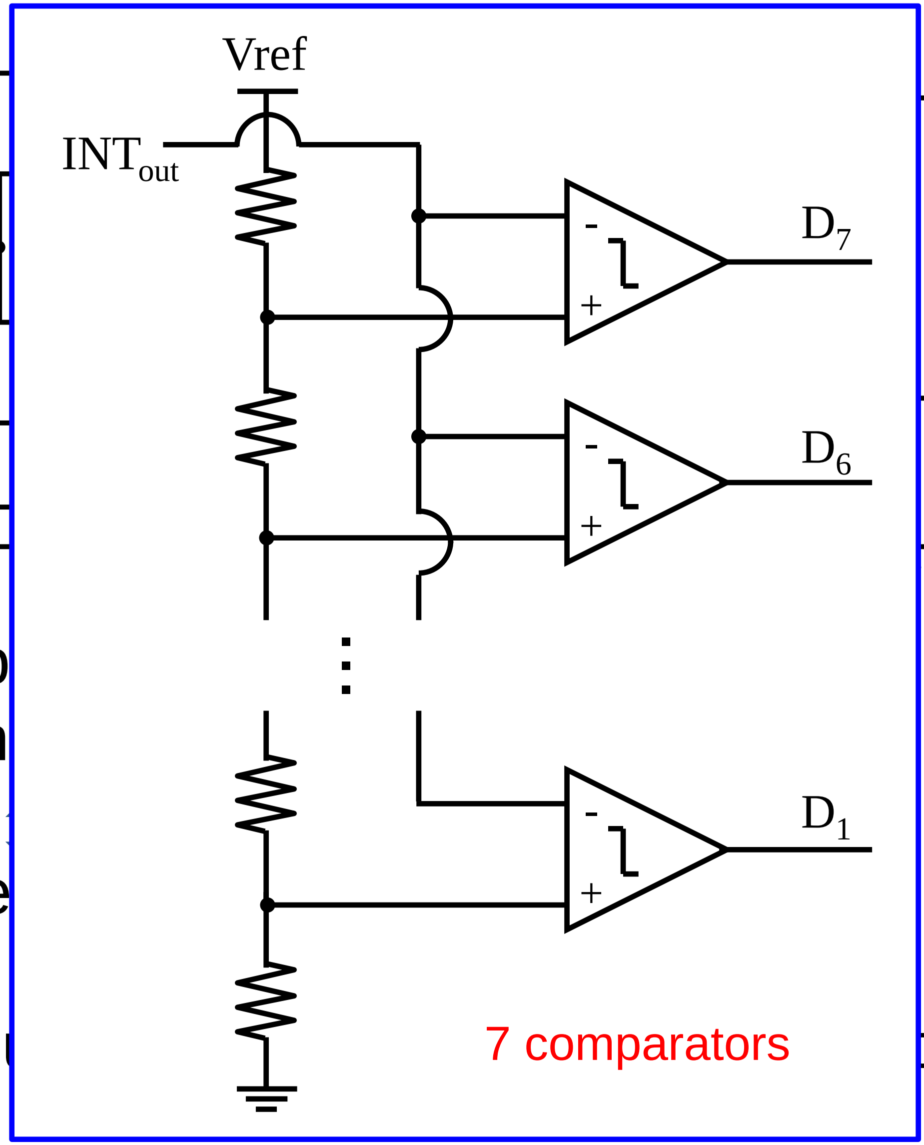
⇕

Shorter measurement time with a given time resolution

- TDC non-linearity due to mismatches among delay cells.

Multi-Bit ΣΔ TDC



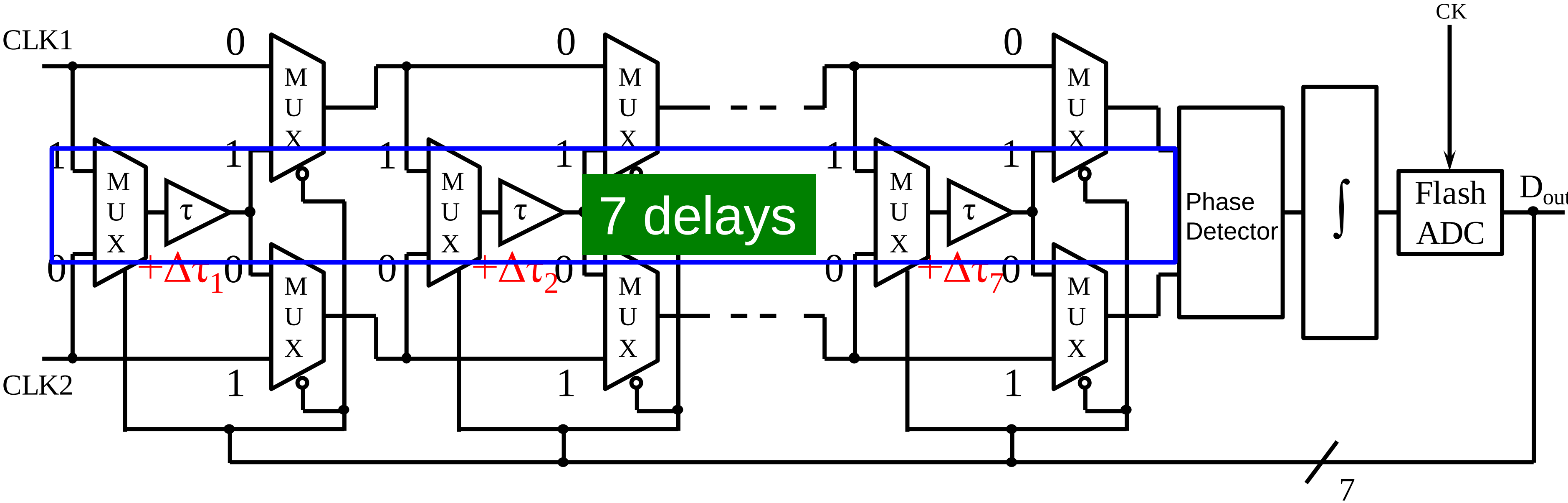


- 3-bit : 2^3-1 =7 comp
- Fine time resolution

  Shorter measureme … on

- TDC non-linearity d … cells

Multi-Bit ΣΔ TDC



- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

  Shorter measurement time with a given time resolution

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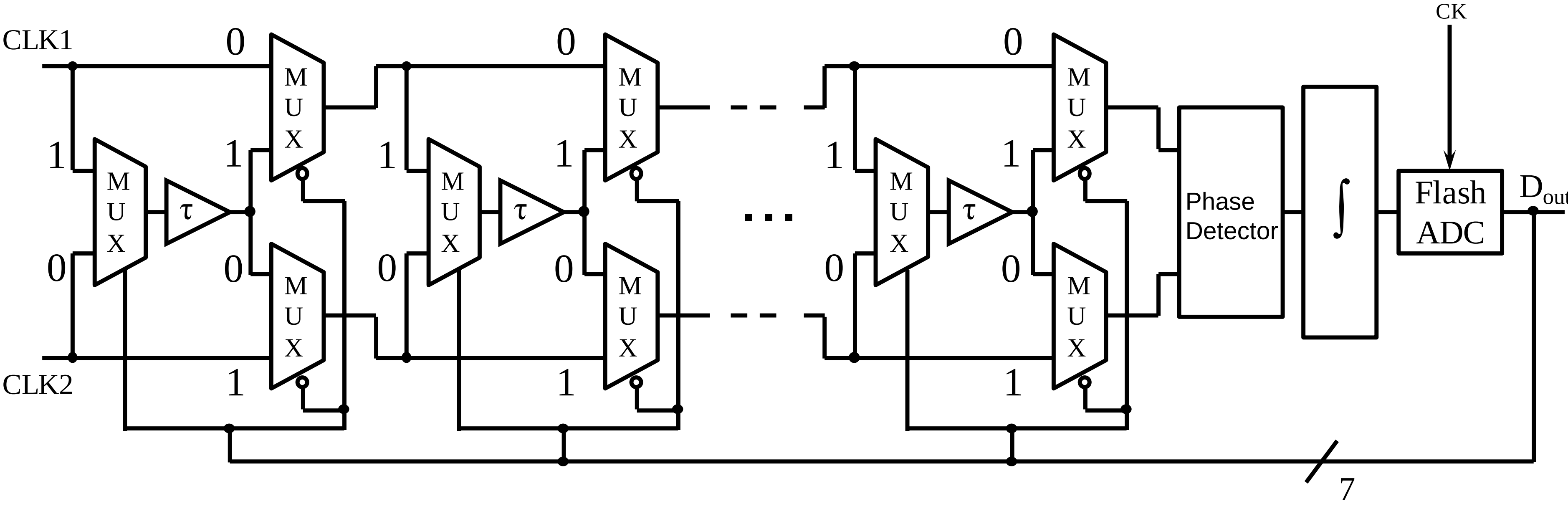
Multi-Bit ΣΔ TDC



- 3-bit : 2^3-1 =7 comparators and delays
- Fine time resolution with a given measurement time

⇕

Shorter measurement time with a given time resolution

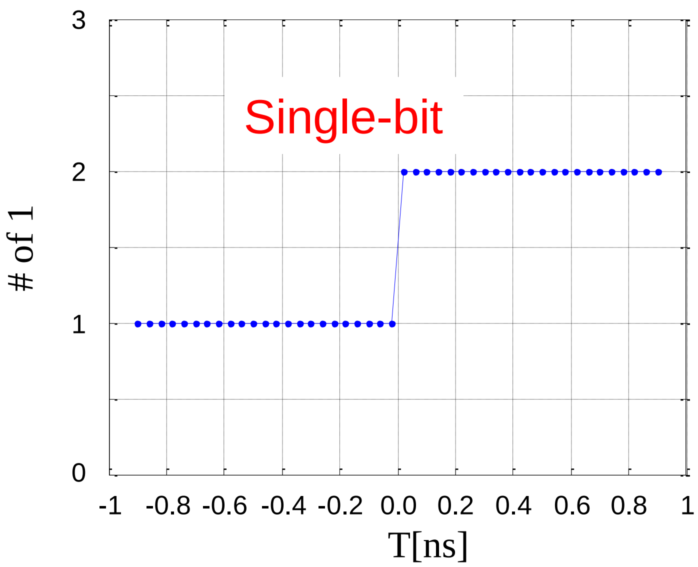
- TDC non-linearity due to mismatches among delay cells

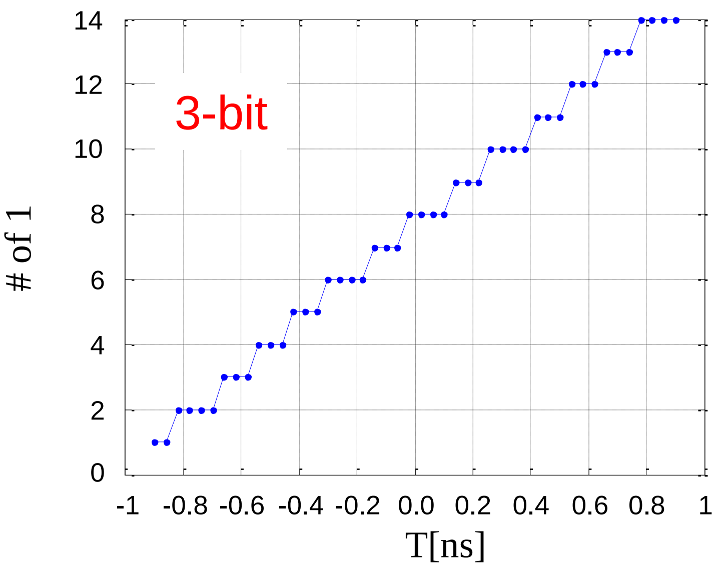
Time Resolution Comparison

- Simulation conditions

	1-bit ΣΔ TDC	3-bit ΣΔ TDC
Rising timing edge difference (T)	-0.9 ～ 0.9[ns] (Resolution : 0.04[ns])	-0.9 ～ 0.9[ns] (Resolution : 0.04[ns])
Delay time (τ)	1[ns]	0.145[ns]
The number of digital outputs	2	2

■ A rising number of outputs for the interval T



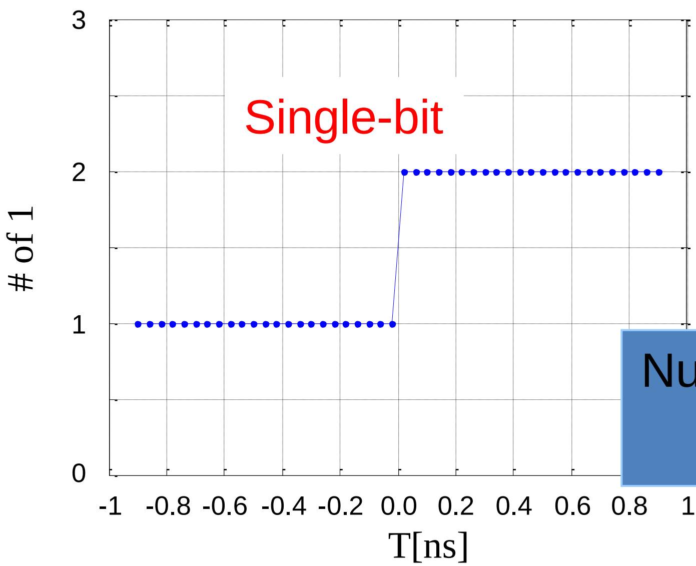


Measurement Time Comparison

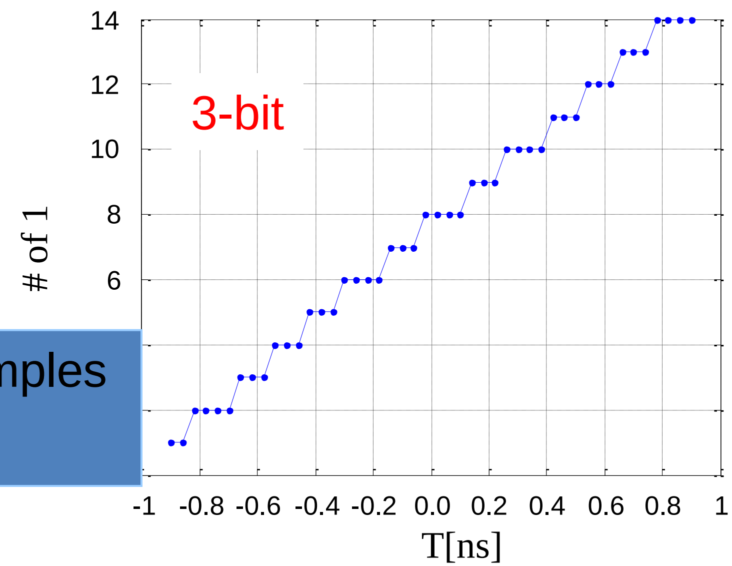
✓Multi-bit takes short measurement time for a given time resolution

Low cost testing

■ A rising number of outputs for the interval T



Number of samples
Is 2



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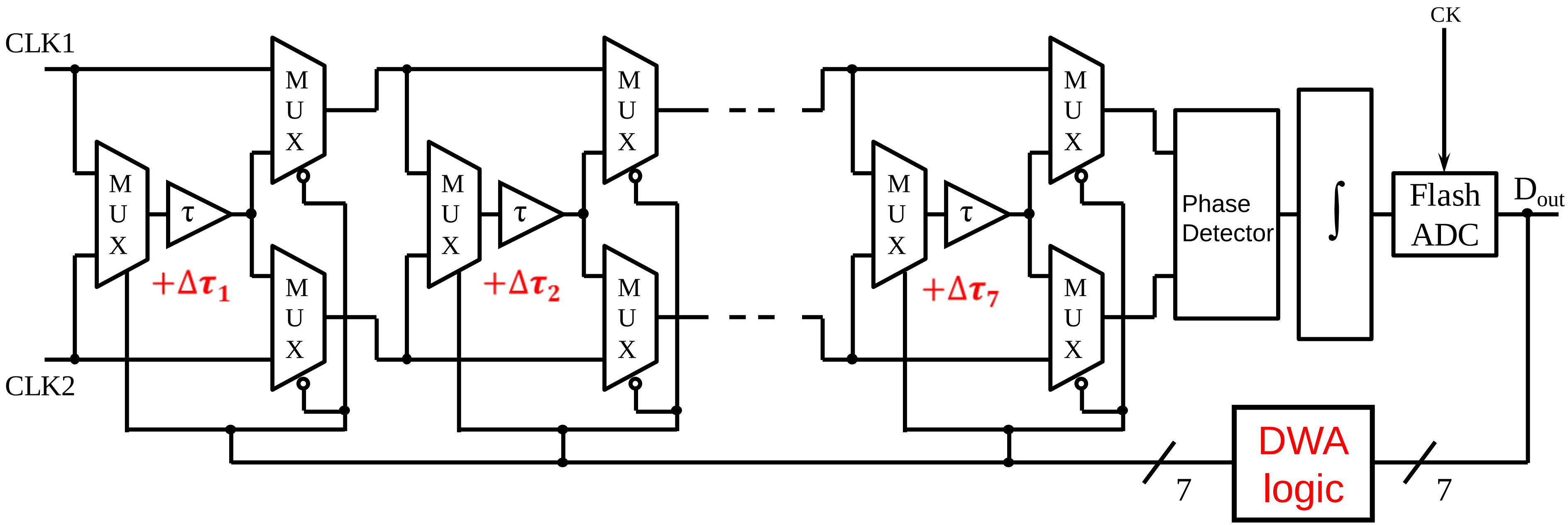
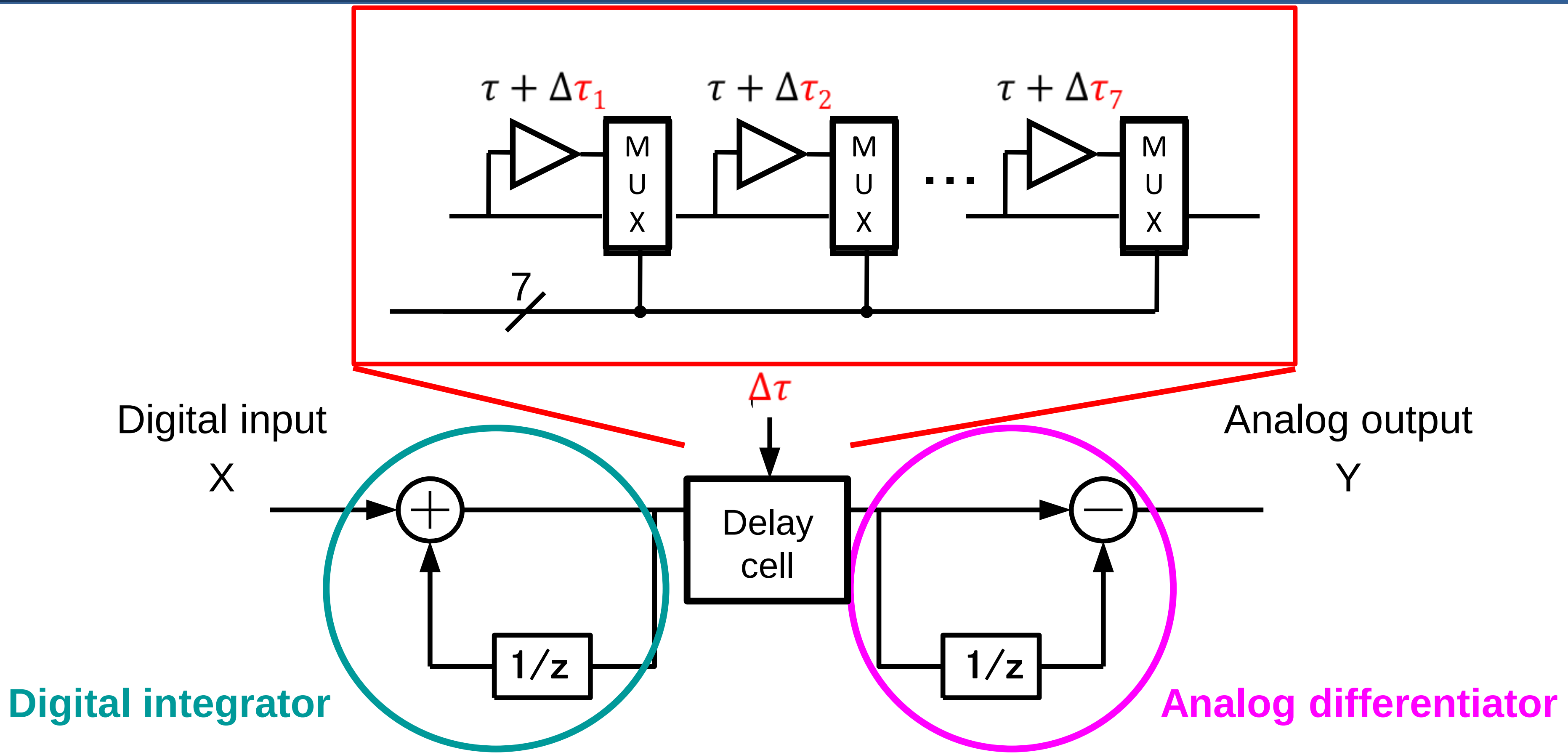
DWA (Data Weighted Averaging)



- Flash ADC outputs
  ➡ shuffled by DWA logic,
  fed into MUXs as select signals
- Delay mismatch effects
  ➡ moved to high-frequency (noise-shaping)

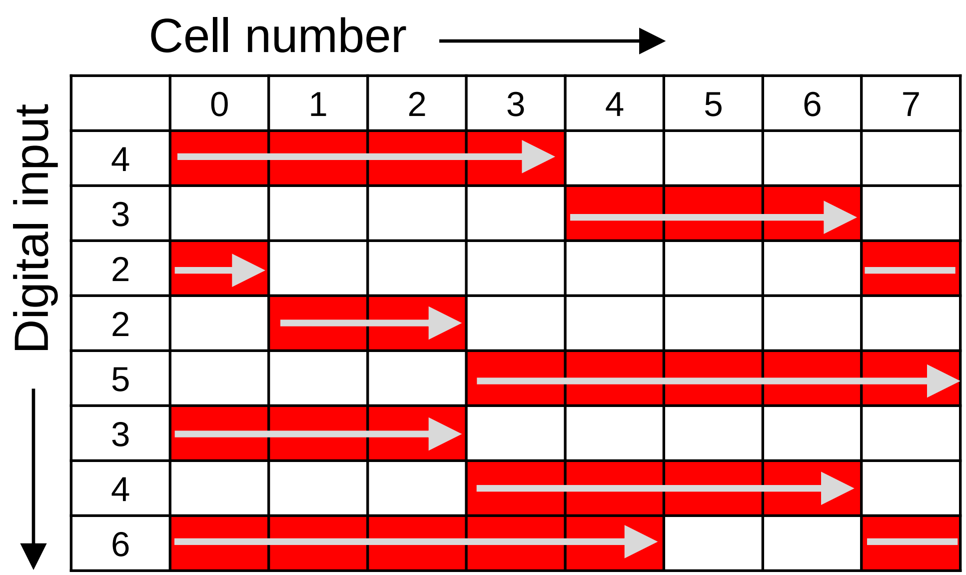
Noise-Shaping



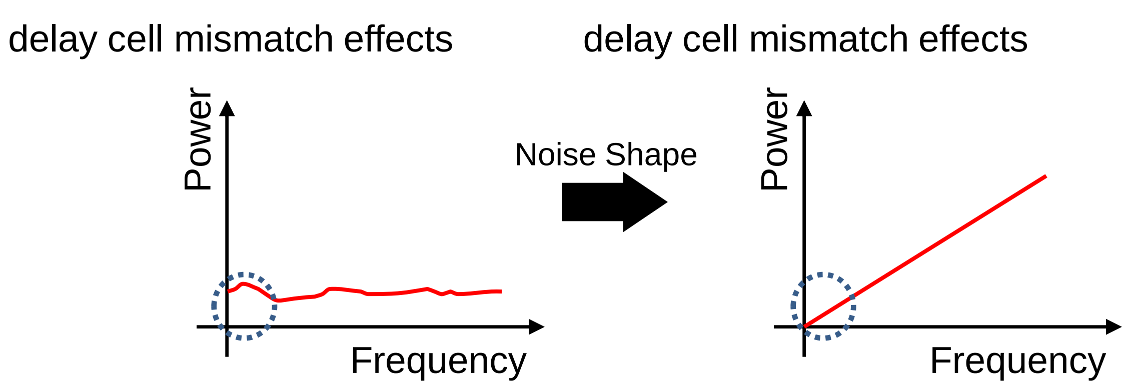
$$Y(z) = X(z) + (1 - 1/Z)\Delta\tau(z)$$

Delay mismatch $\Delta\tau$ is first-order noise-shaped.

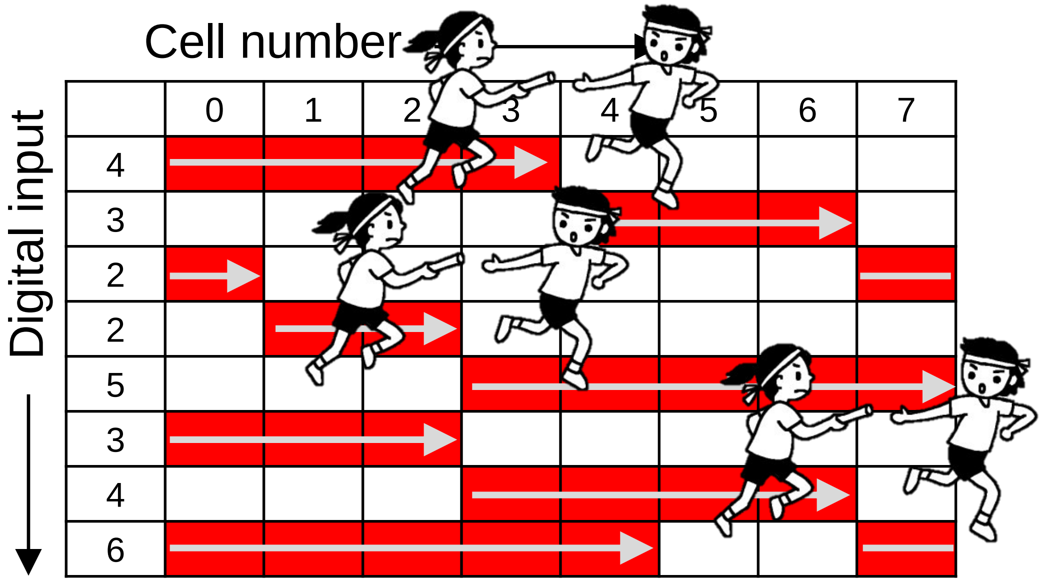
DWA & Noise Shaping



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation



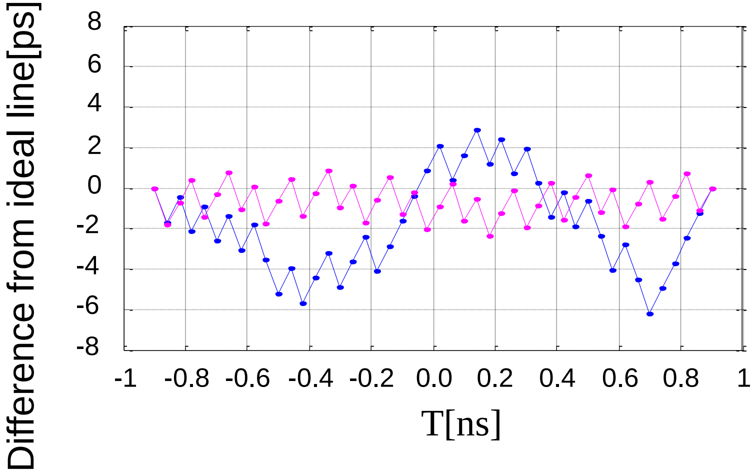
DWA Operation



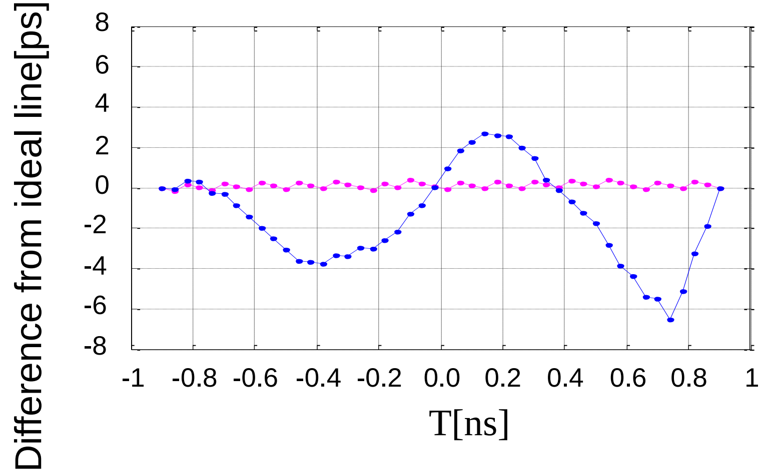
Pass a baton in relay race !

Simulation of ΔΣ TDC with DWA

- Output：99 points



- Output：599 points



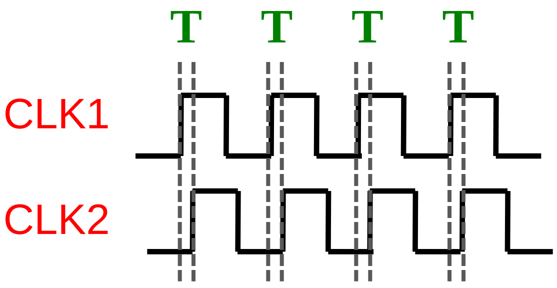
ΔΣ TDC(with DWA)

ΔΣ TDC(without DWA)

✓Reduce the effect of delay mismatches

ΣΔ TDC linearity is improved

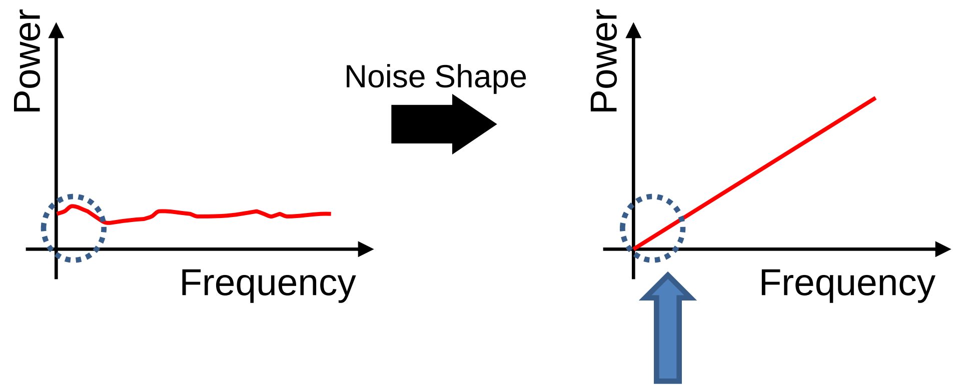
DWA Effectiveness



- Delay τ : integration & differentiation
- Delay mismatch $\Delta\tau$: differentiation

delay cell mismatch effects

delay cell mismatch effects



Measure **T**

T is DC signal.

Mismatch effects
reduction at DC

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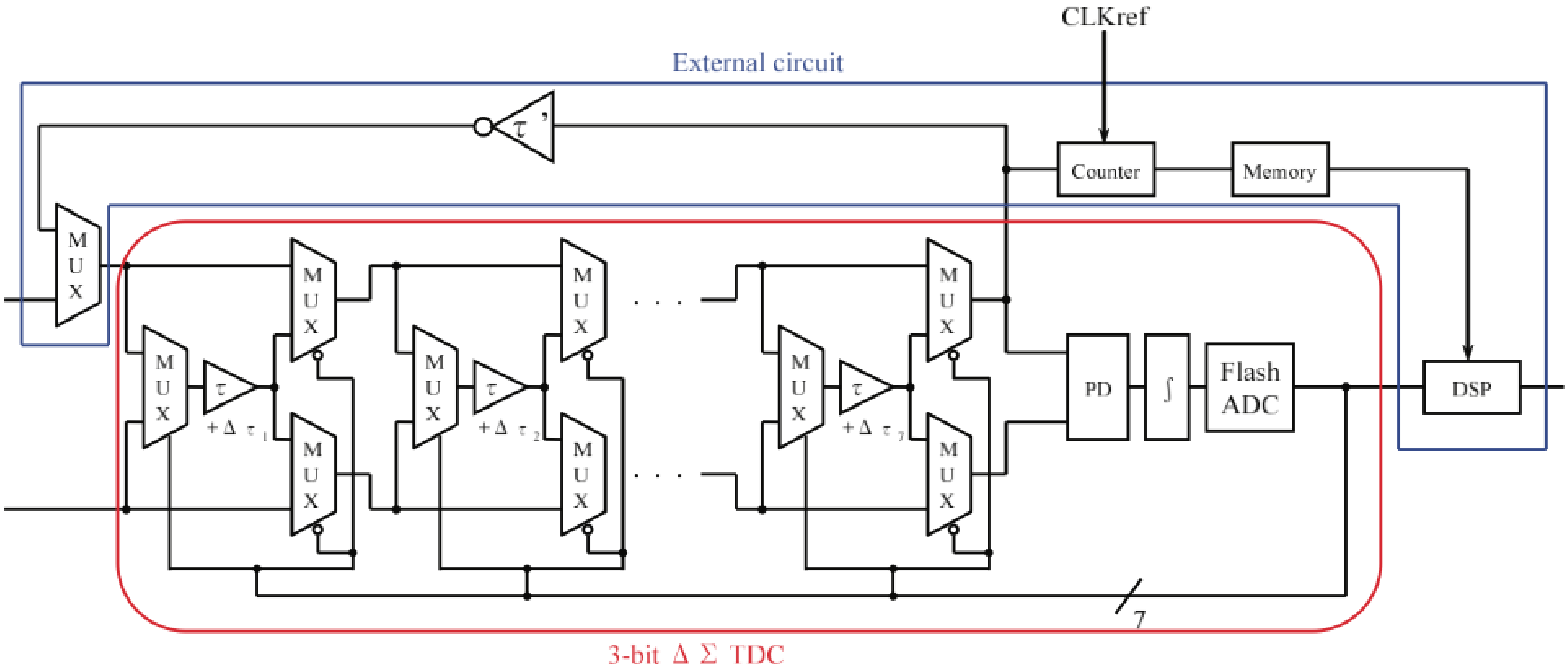
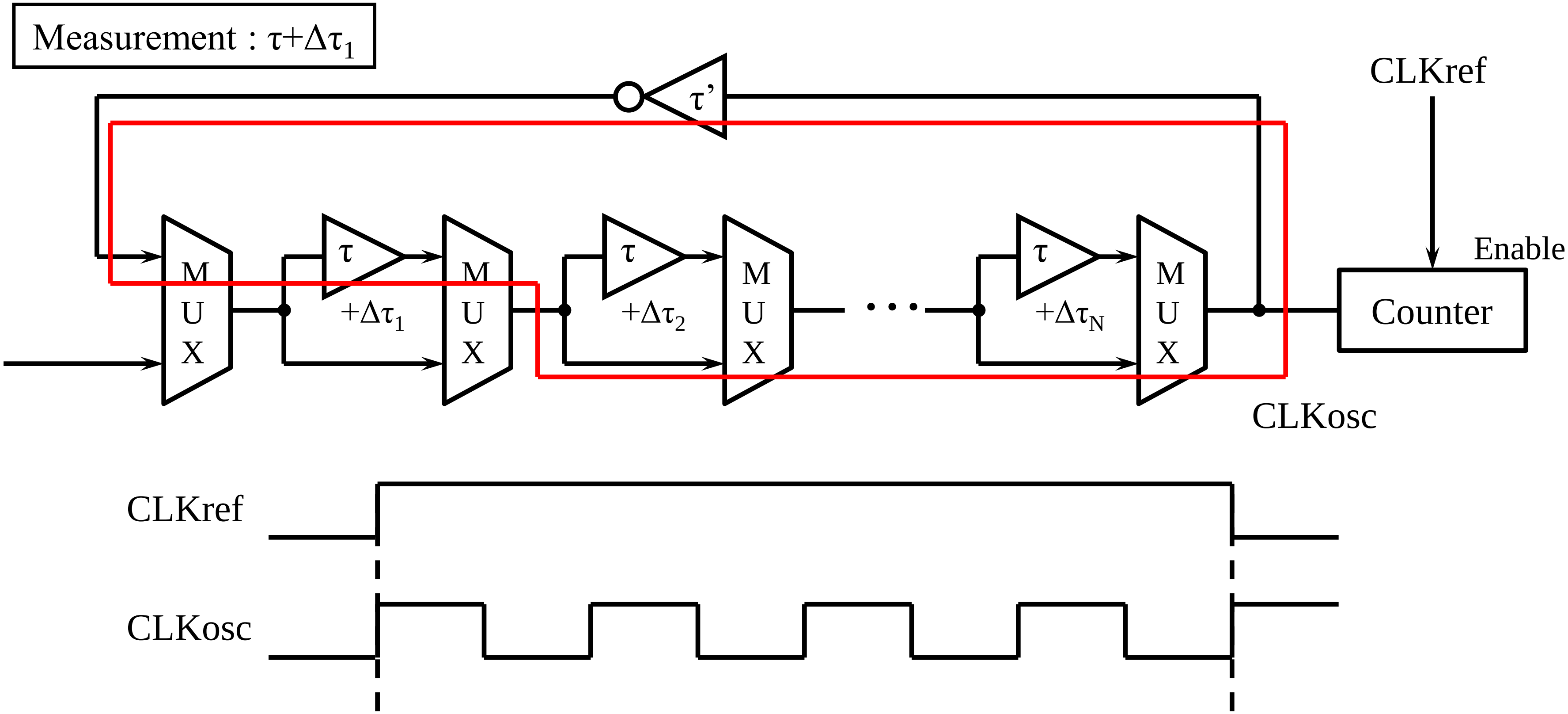
ΣΔ TDC with Self-Calibration



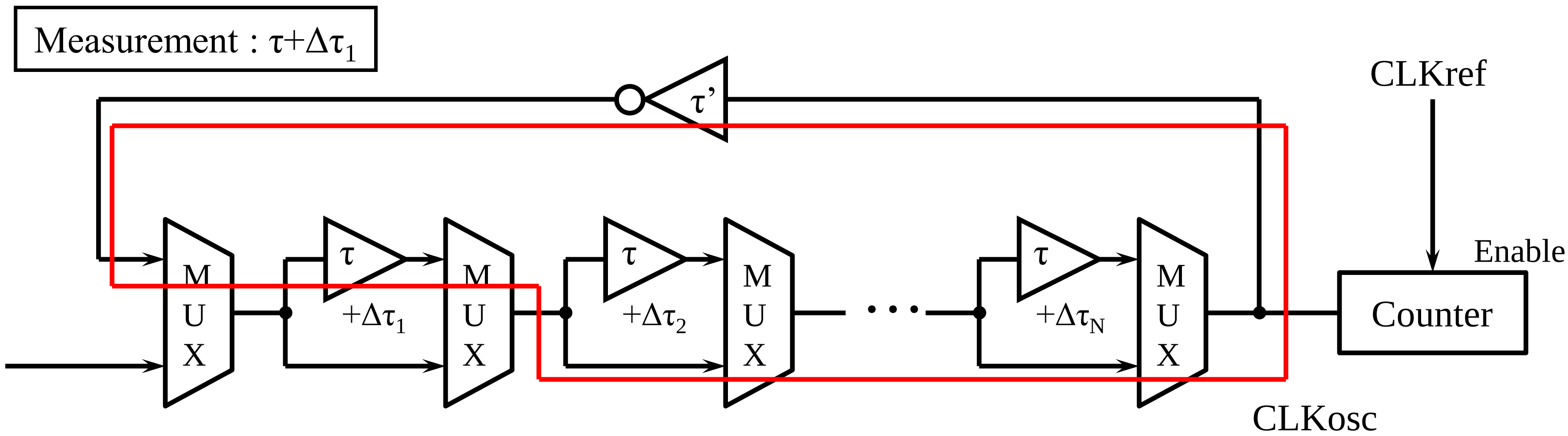
- Self-calibration circuit: inverter, MUX, counter, memory
- Measure delay values and store them in memory

Self-Measurement of Delay

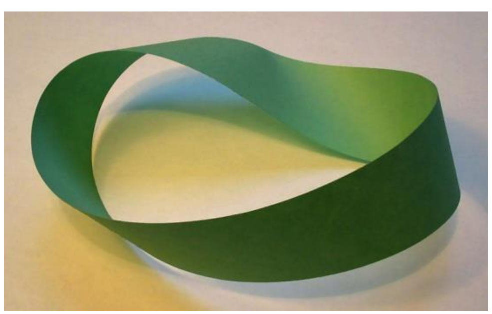


- Ring oscillator with a delay cell to be measured
- Counter measure the number of the pulses
- $\Delta\tau$ can be calculated
- Measured delay values are stored in memory

Time Signal & Ring Oscillator

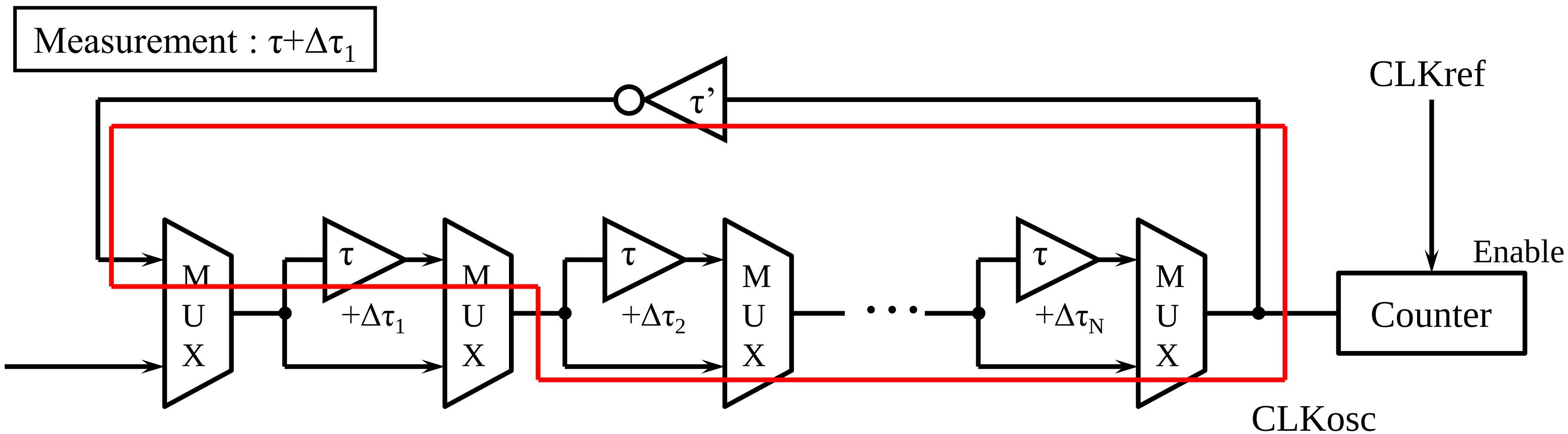


Ring oscillator



Möbius strip

Self-Measurement of Delay



Oscillation frequency

$$f = \frac{1}{2(\tau' + \tau + \Delta\tau_1)}$$

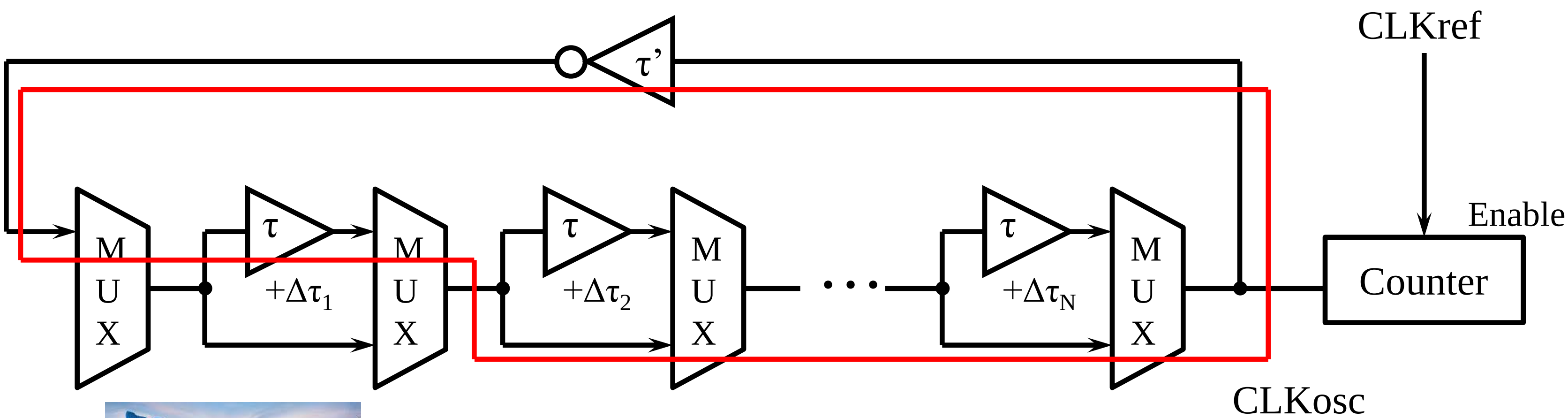
Measure $\Delta\tau_2$、$\Delta\tau_3$, $\Delta\tau_4$、....$\Delta\tau_N$ one by one.

$\Delta\tau_1$ can be calculated from the oscillation frequency

Essence of Proposed Method

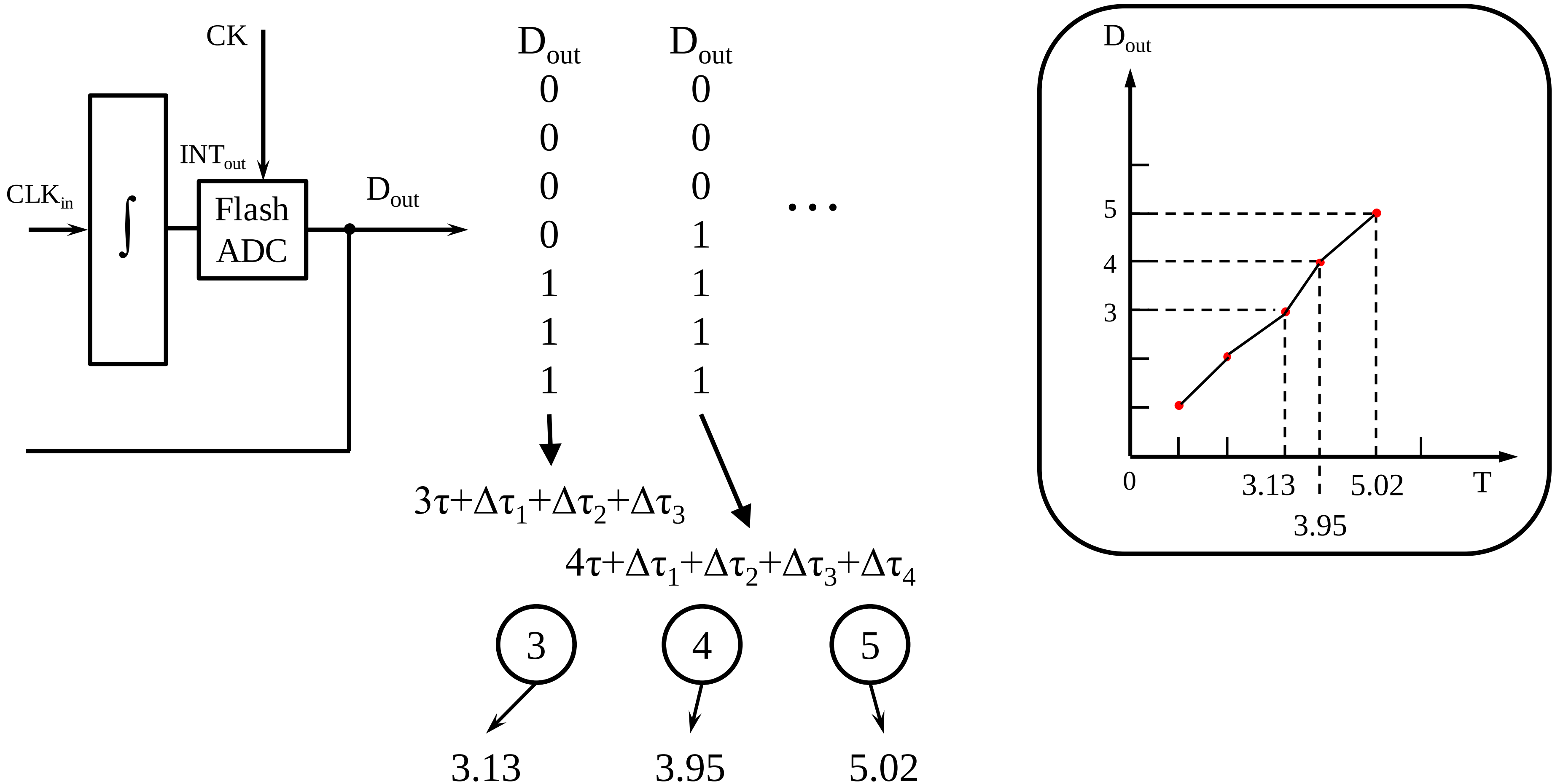
- All operations are done in digital domain
- Signal is Time instead of Voltage.

  ⇒ Easy, accurate measurement of $\Delta\tau$



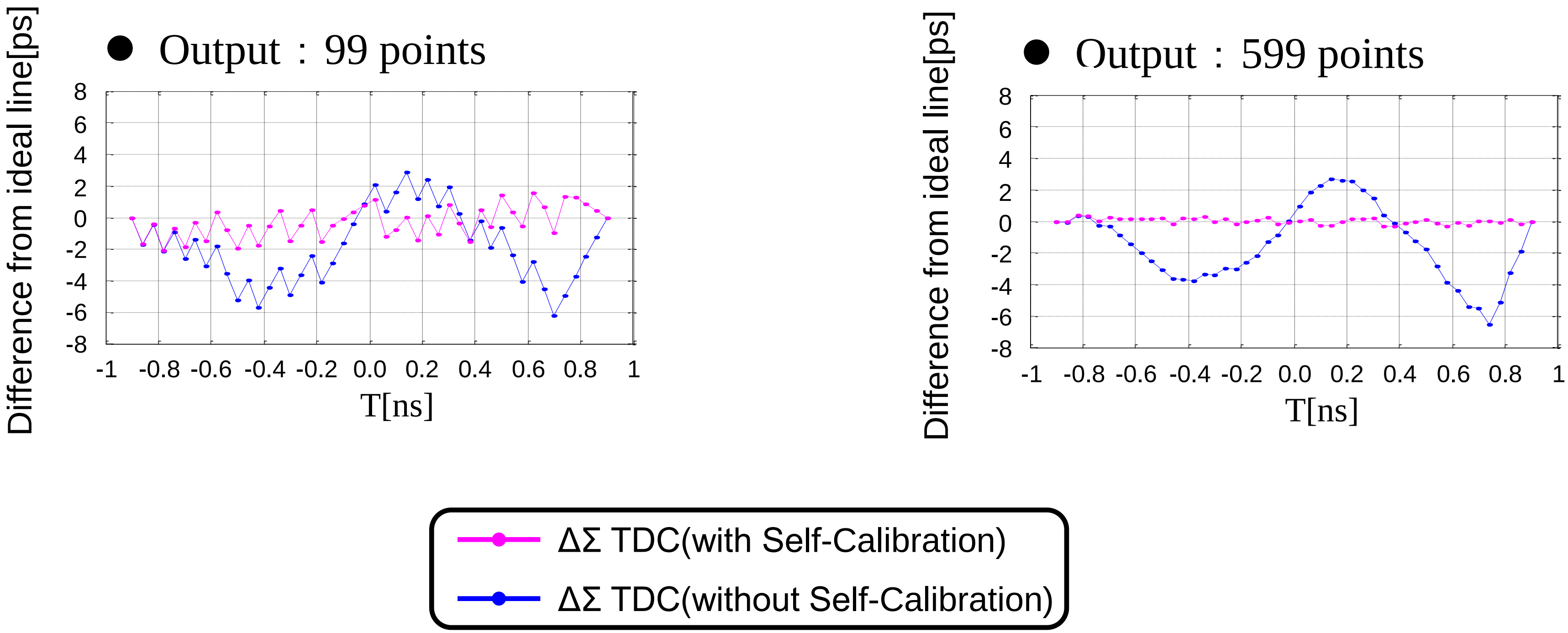
Time flies like an arrow!

Proposed Error Correction Scheme



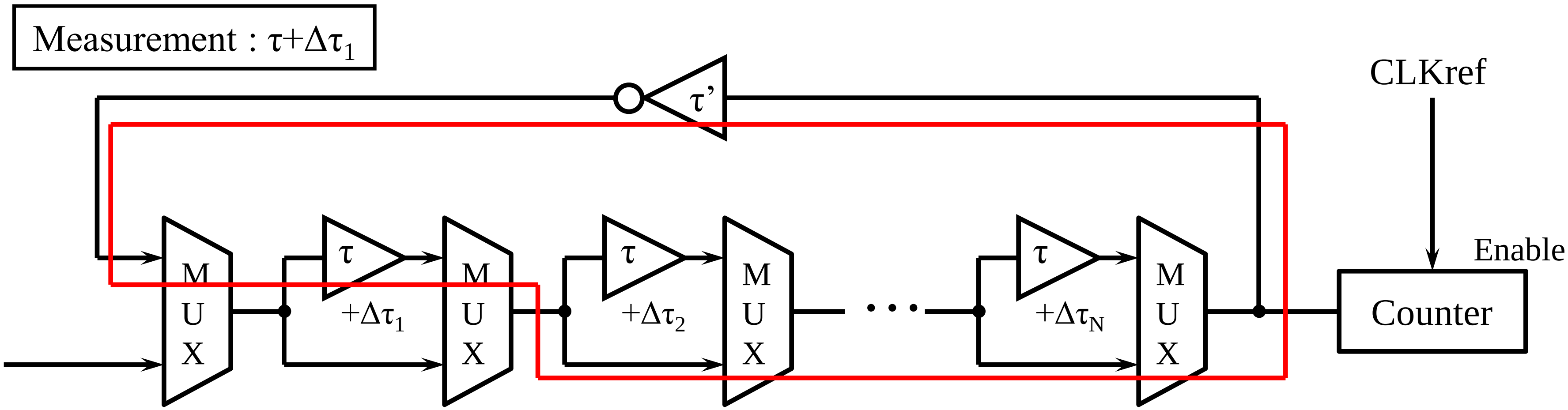
- Obtain TDC raw output (D_{out}) for two input clocks
- Read delay values from memory, and compensate for the output based on them

Simulation of Self-Calibration



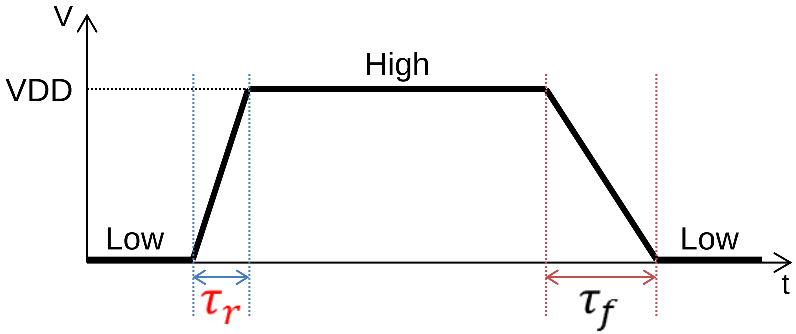
ΣΔ TDC linearity is improved

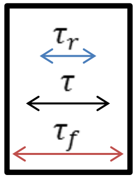
Problem of Ring Oscillator



$$f = \frac{1}{2(\tau' + \tau + \Delta\tau_1)}$$

Measured delay

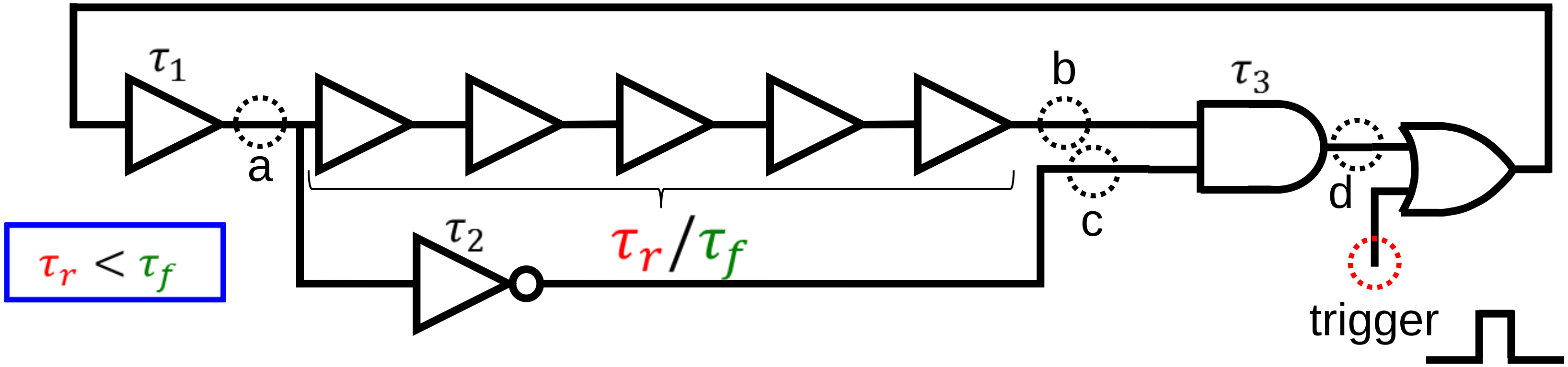




$$\tau = \frac{\tau_r + \tau_f}{2}$$

However, we need the rise delay τr

Improved Delay Measurement Circuit

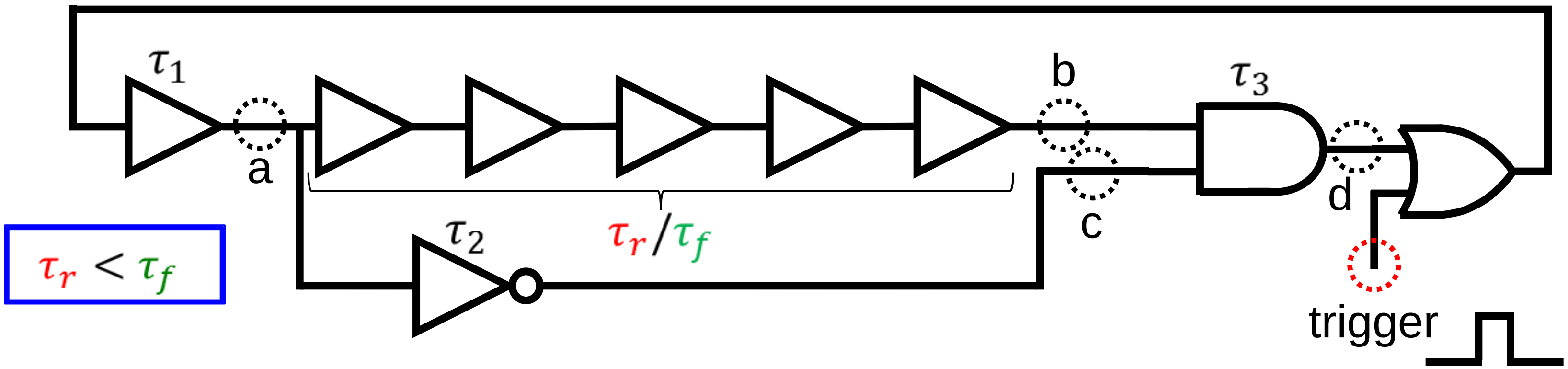


Oscillator circuit to measure

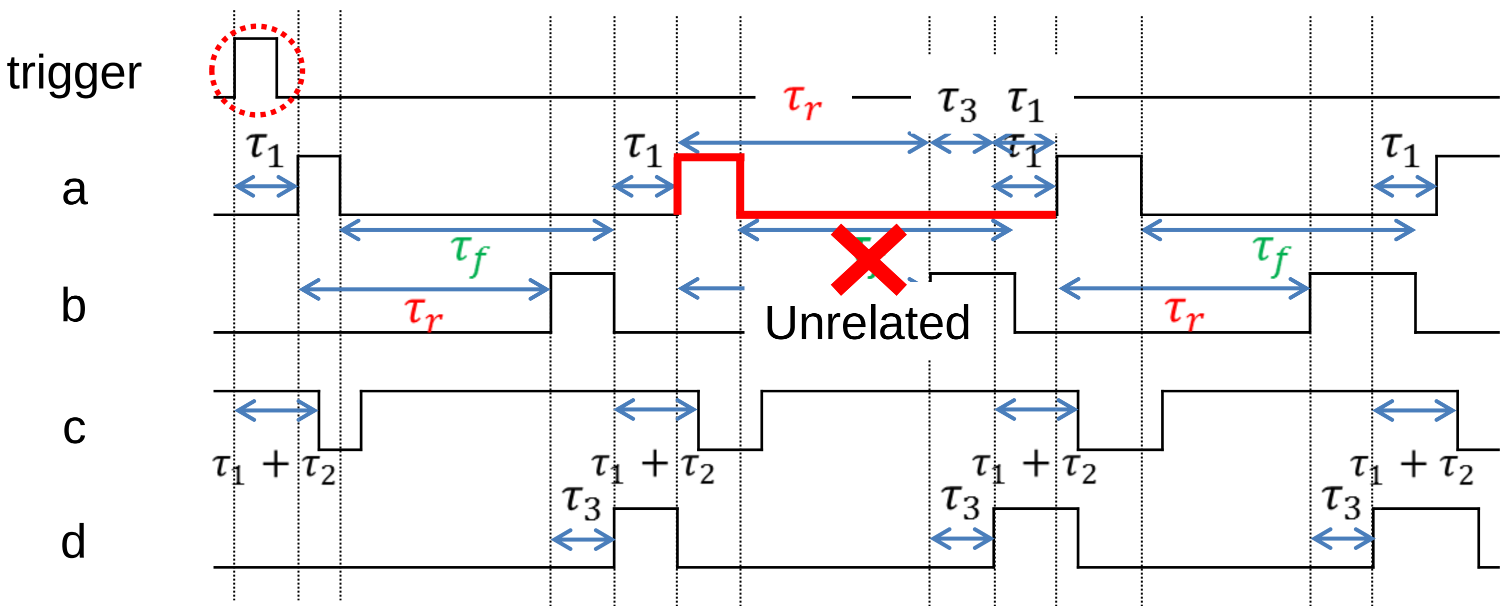
the rise delay τr of the buffer

Oscillation period is a function of τr , but NOT τf

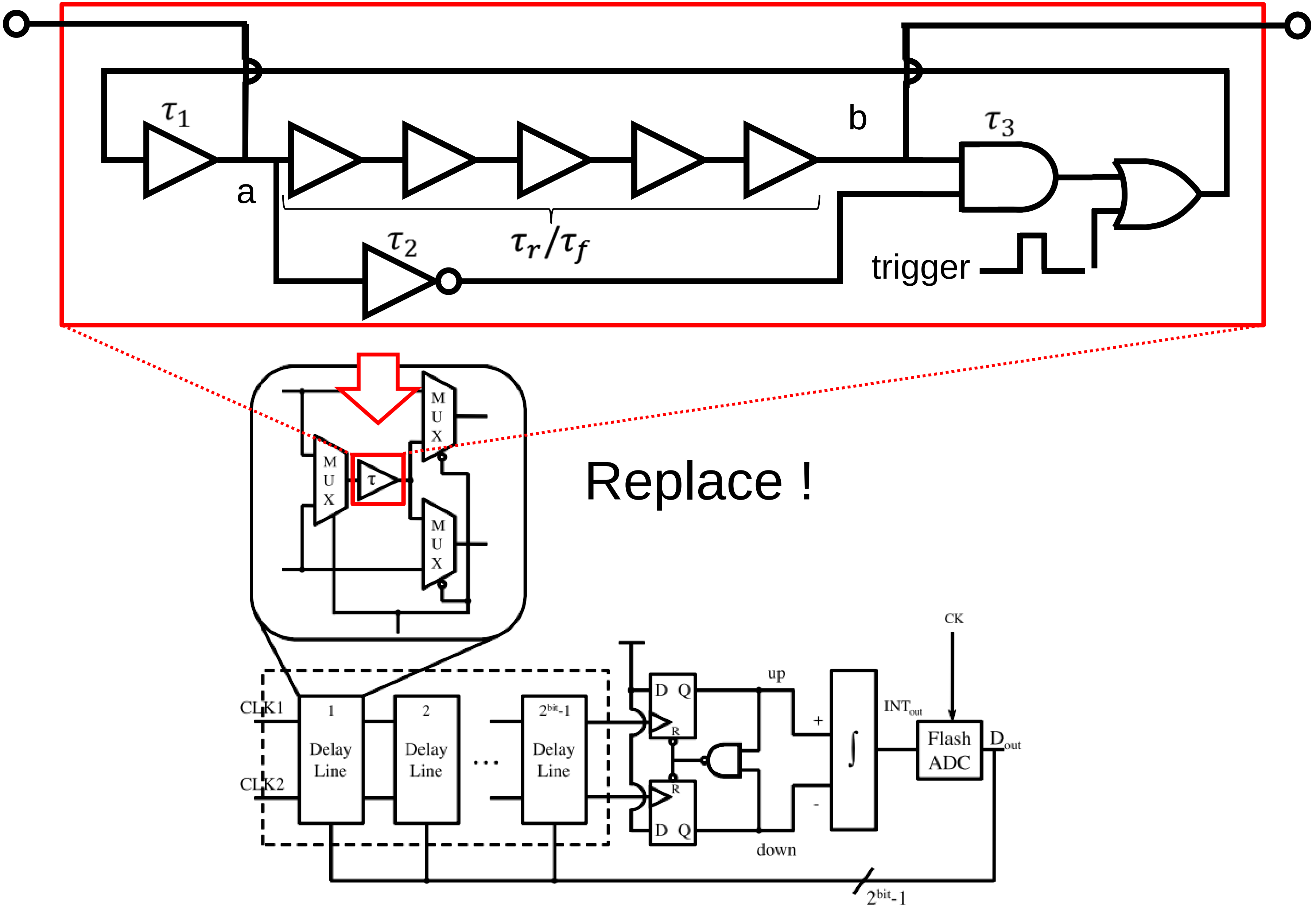
Oscillation Timing Chart



Period: $\tau 1 + \tau 3 + \tau r$



Delay with Several Buffers



Replace !

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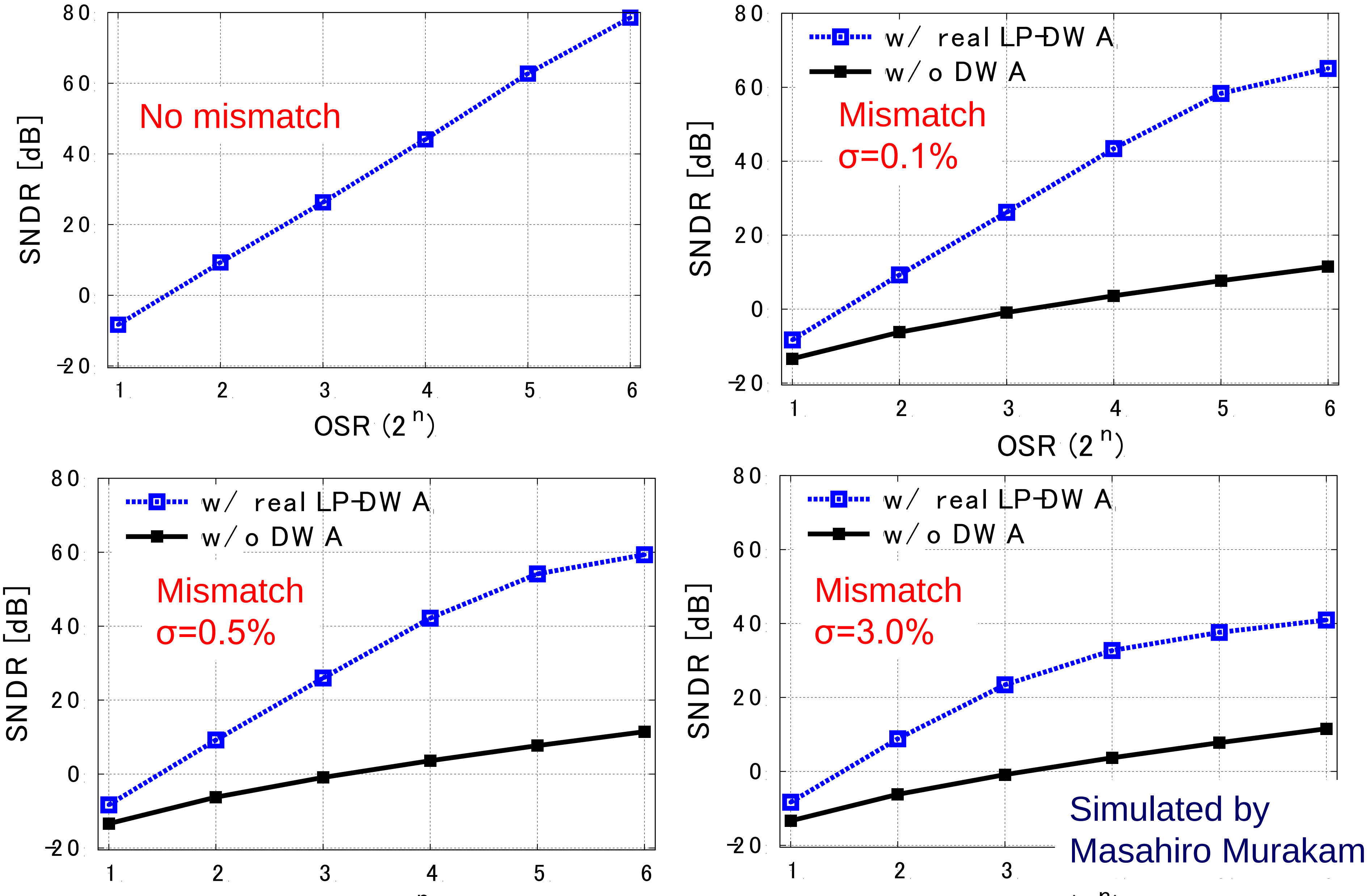
DWA & Mismatches



Simulated by
Masahiro Murakami

Possible Problem in Multi-bit TDC

For ΣΔ ADC,

mismatch σ_{dac} in internal DAC

is as small as 0.1 %.

→ DWA is effective.

For ΣΔ TDC,

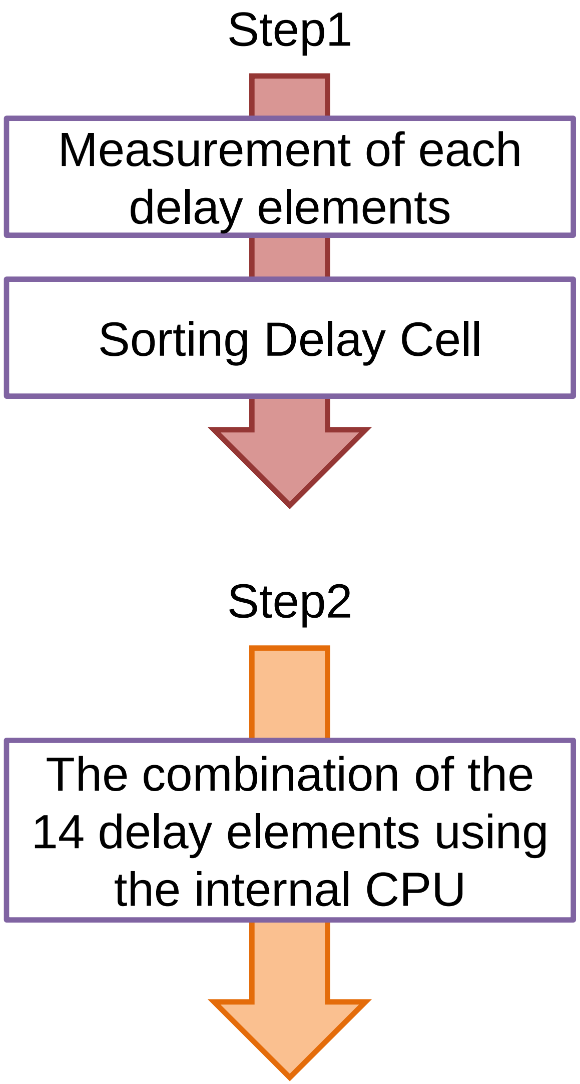
mismatch σ_{delay} in internal delay cells

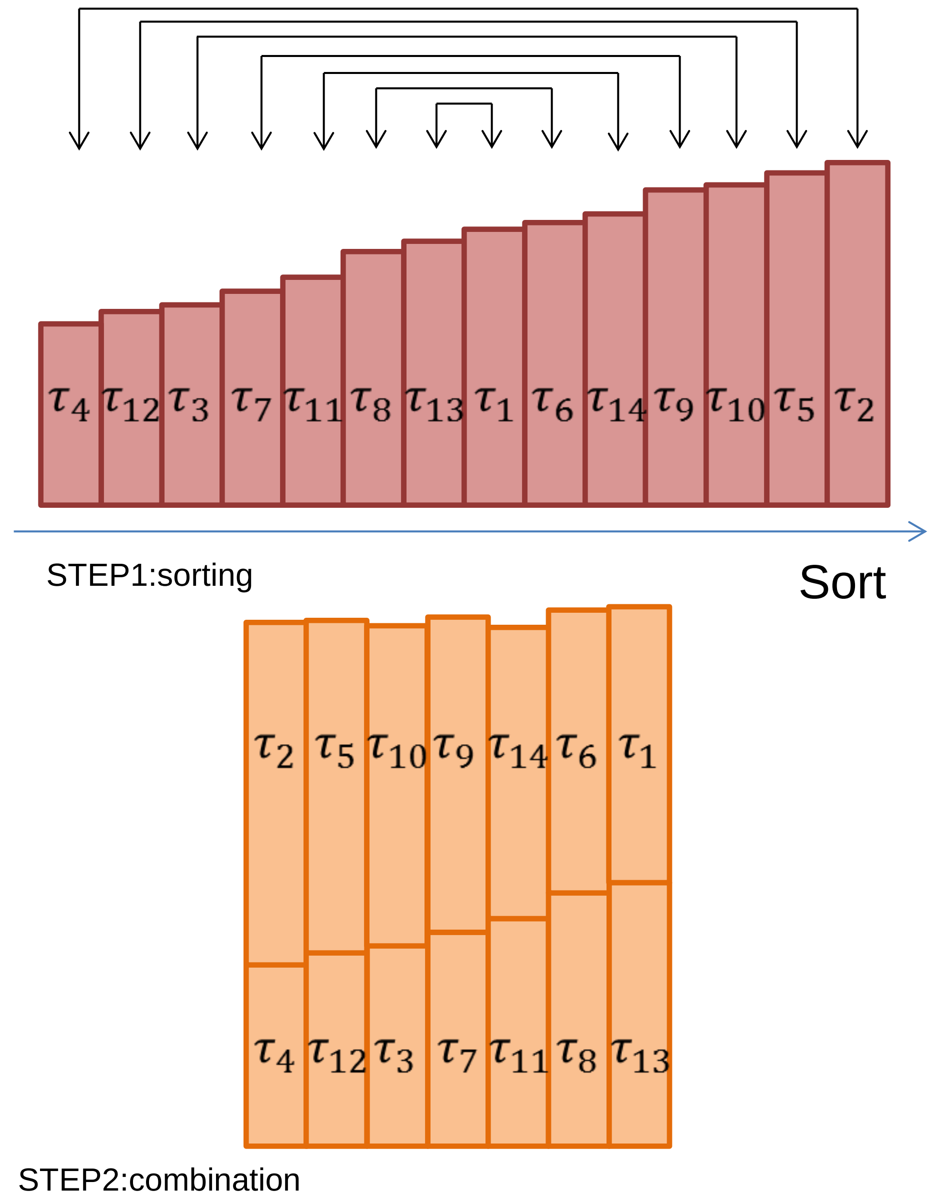
can be much larger than 0.1 %

depending on spec. & delay cell design.

→ DWA may not be effective.

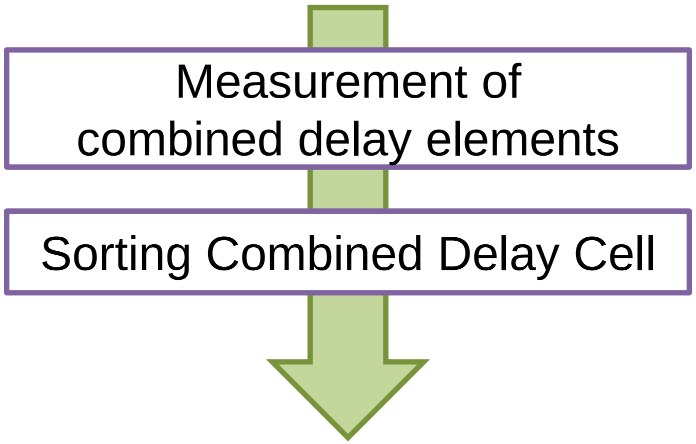
Delay Cell Sorting (Step 1, 2)

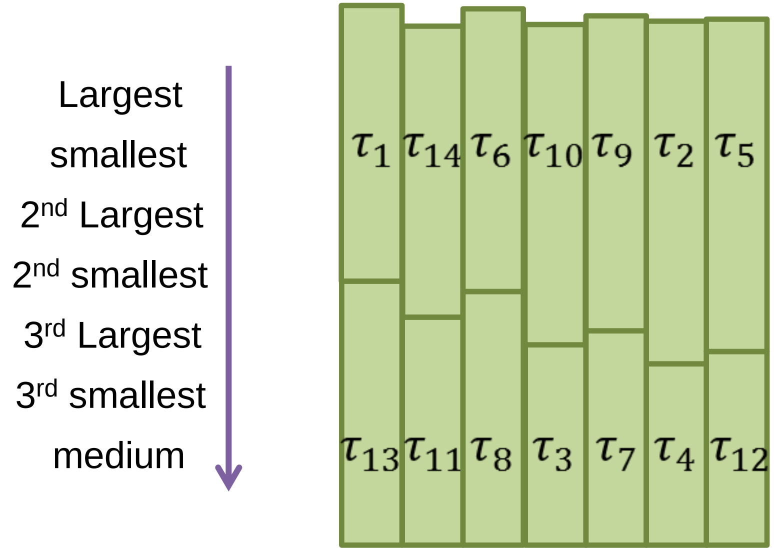




Delay Cell Sorting (Step 3, 4)

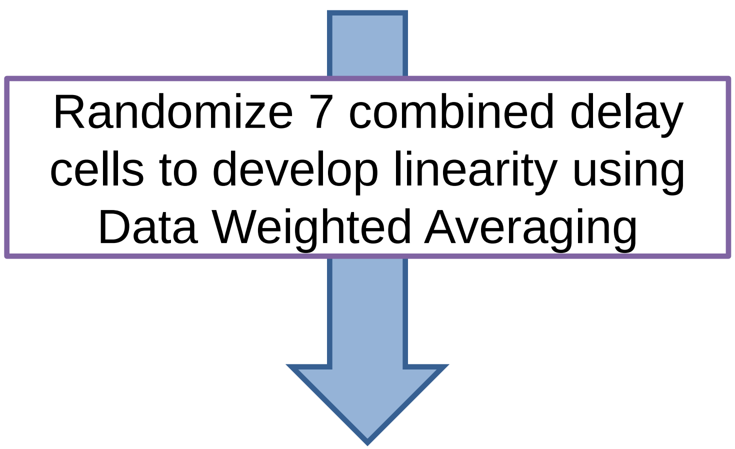
Step3

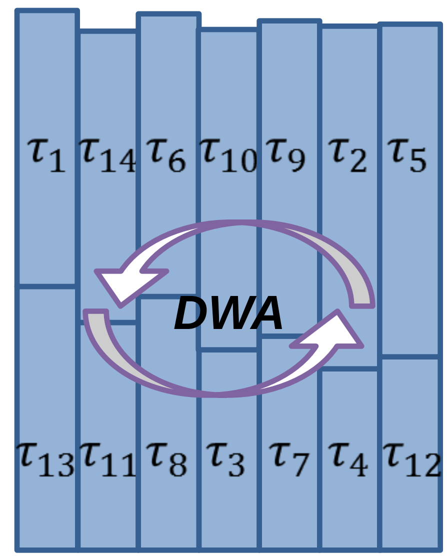




STEP3:sorting

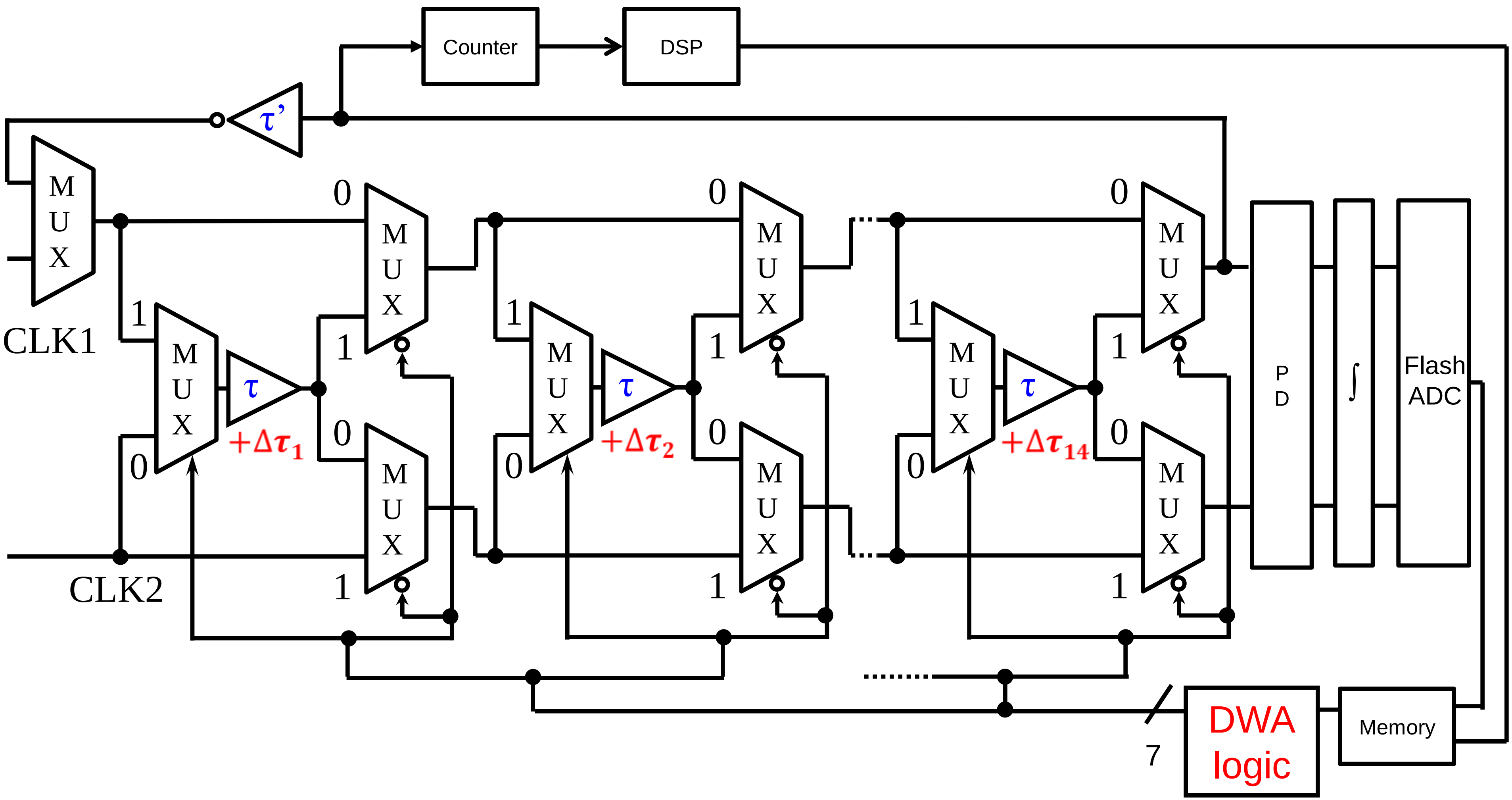
Step4





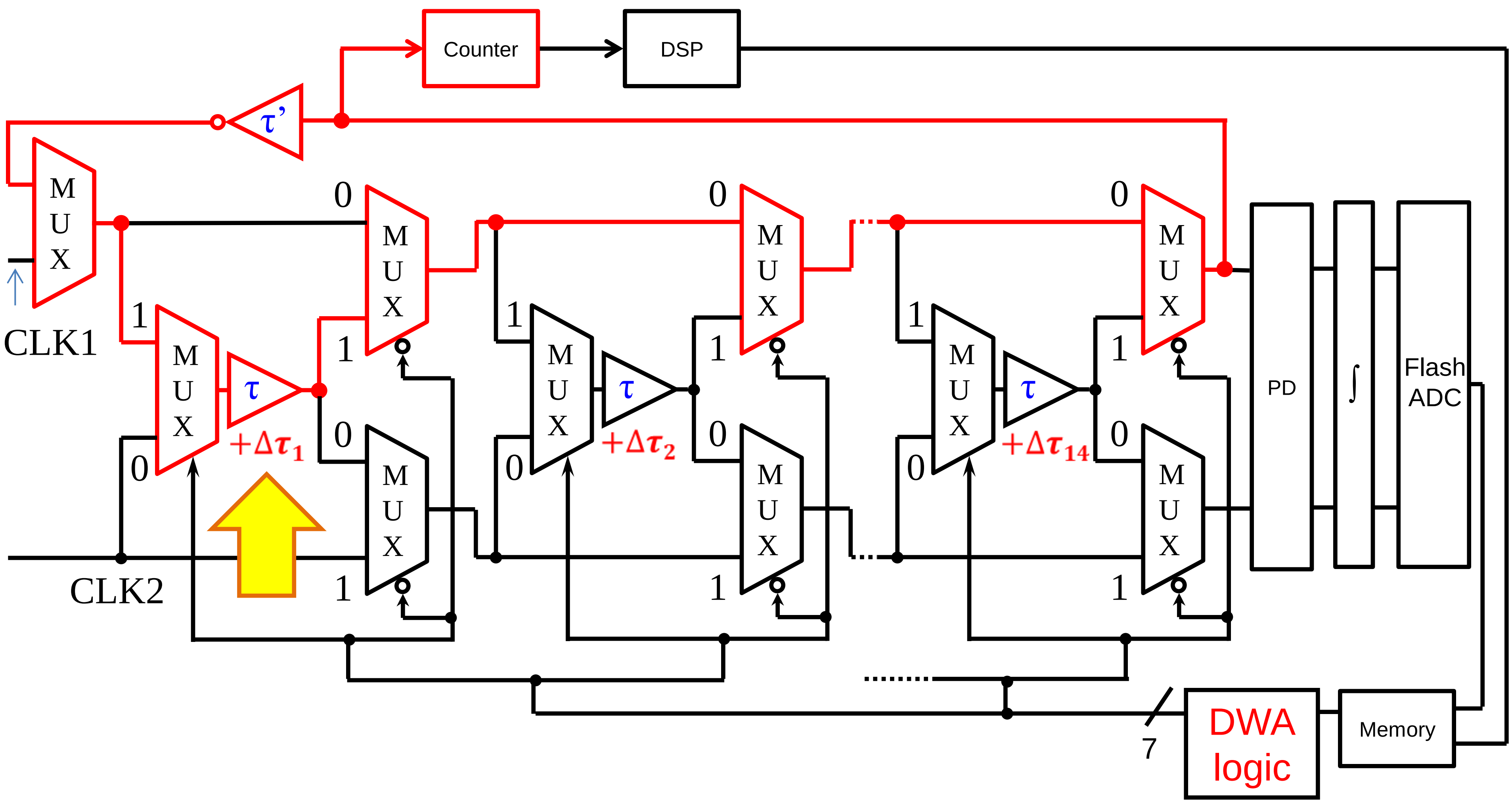
STEP4:DWA

Multi-Bit ΣΔ TDC with Sorting Technique



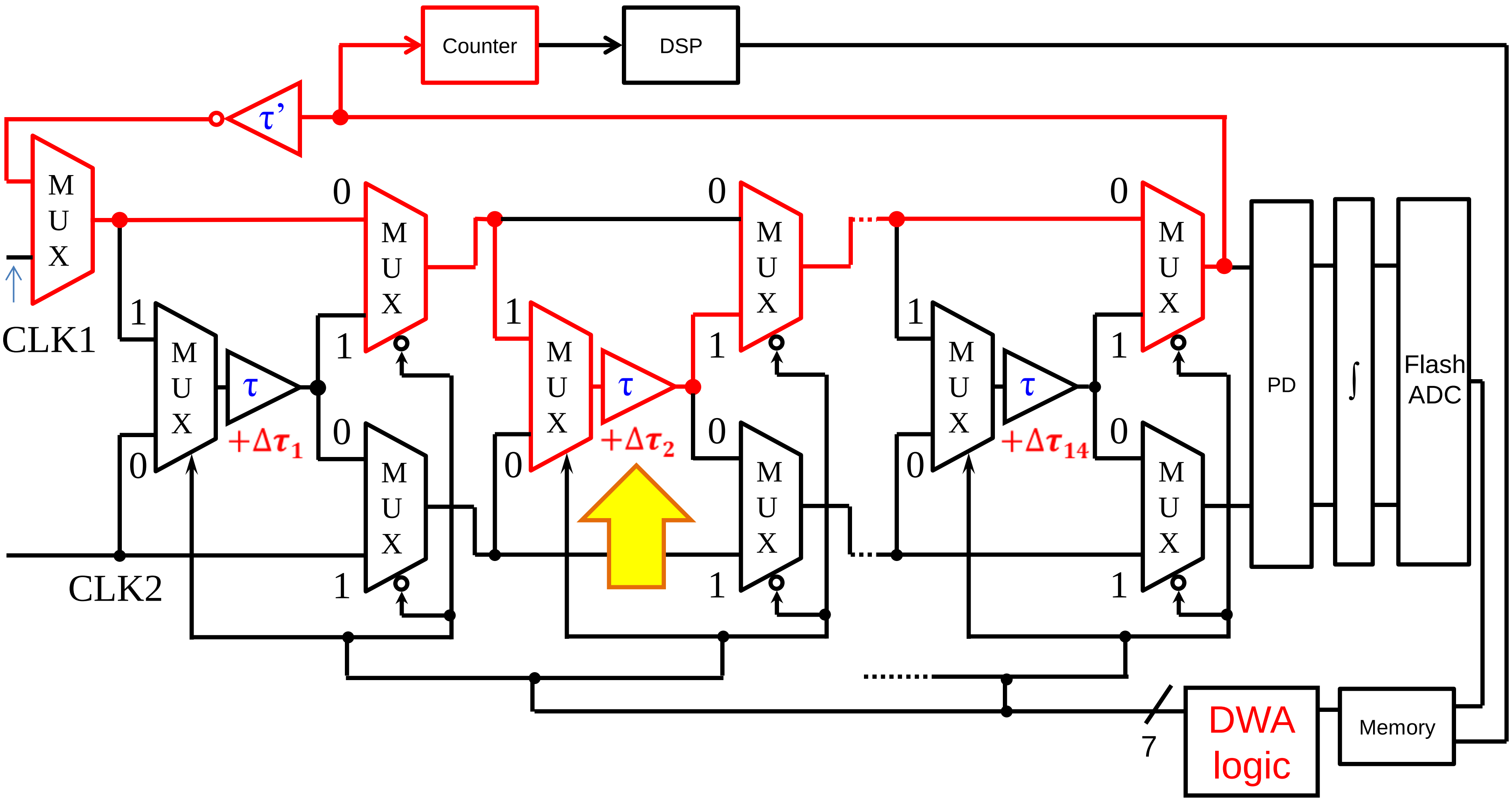
Measure $\tau + \Delta\tau 1$

$\Delta\tau 1$ can be measured digitally.

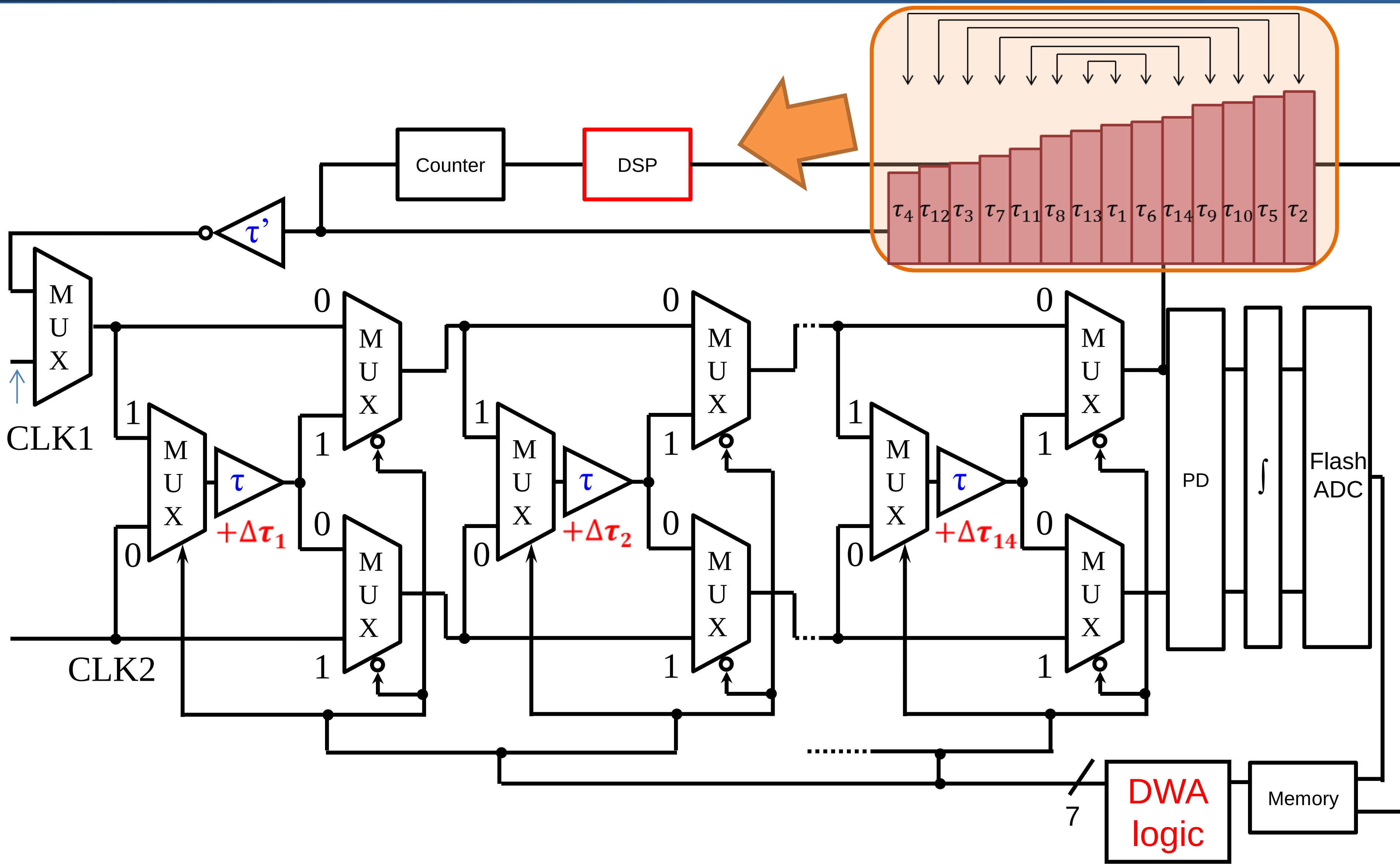


Measure τ + $\Delta\tau 2$

$\Delta\tau 2$ can be measured digitally.

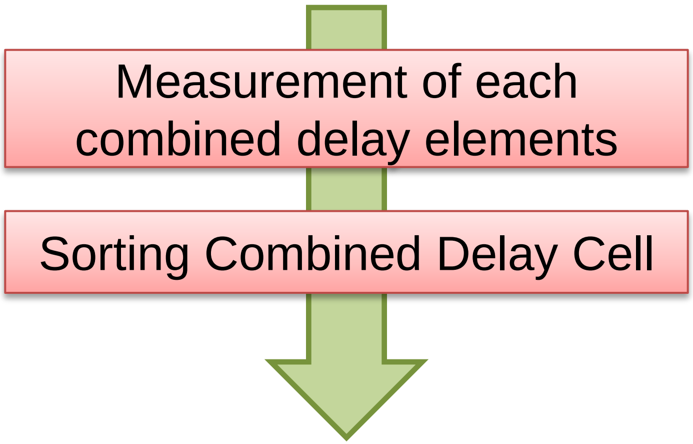


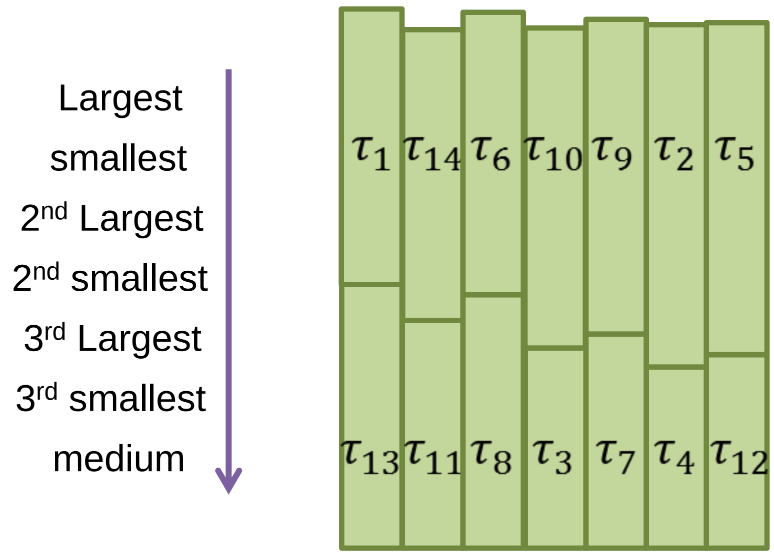
Multi-Bit ΣΔ TDC with Sorting Technique



Delay Cell Sorting (Step 3, 4)

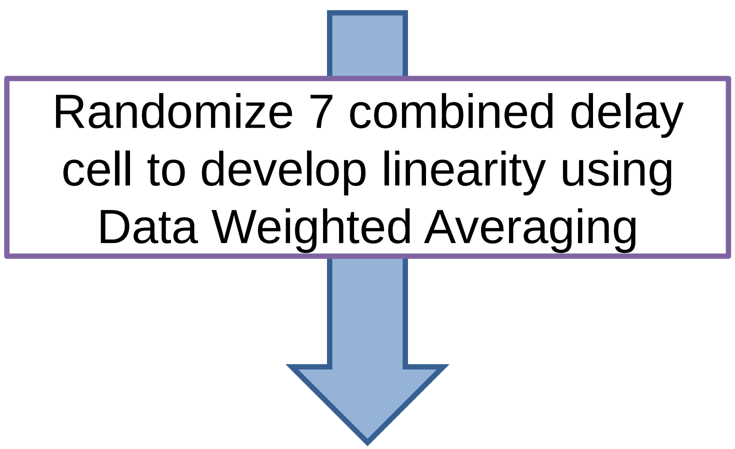
Step3

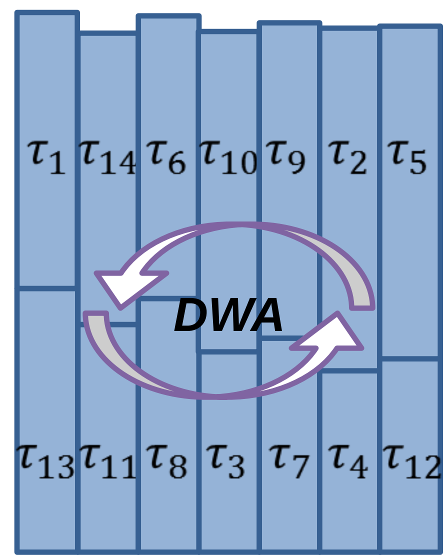




STEP3:sorting

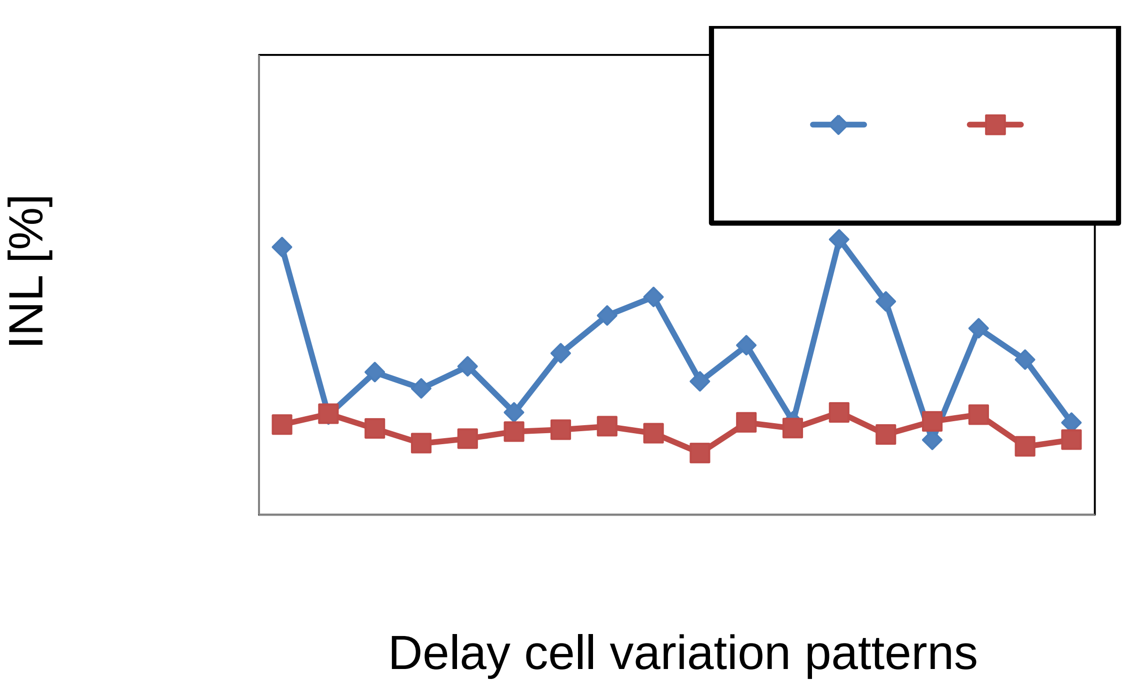
Step4





STEP4:DWA

Matlab Simulation Result



Delay variation σ_{delay} : up to 5%.

Number of TDC output data: 1K points

For large delay variation,
Sorting is effective, but only DWA may NOT be effective enough.

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Circuit Performance Comparison

	Flash TDC	1-bit ΣΔ TDC	Multi-Bit ΣΔ TDC (without correction)	Multi-Bit ΣΔ TDC (with correction)
Area	×	◎	○	○
Resolution	×	◎	◎	◎
Accuracy	△	◎	×	◎
Time	◎	×	○	○

Conclusion

- We propose to use ΣΔ TDC for digital signal timing measurement

- Multi-bit ΣΔ TDC
  - Short measurement time
  - Fine time resolution
  - Non-linearity due to mismatches among delay cells

  ⇨ Three techniques to improve linearity
  - DWA
  - Self-Calibration (signal is "time")
  - Sorting

Low cost, high quality digital timing test can be realized

Final Remark

ΣΔTDC can also measure
phase noise power spectrum.

Presented by

“Phase Noise Measurement with Sigma-Delta TDC”,
IEEE International Test Conference, Poster Session,
Poster No. 3, Anaheim, CA (Sept. 11, 2013)

Kobayashi Laboratory

Time is GOLD !!

ΣΔTDC is a key.