Noise-Shaping Cyclic ADC Architecture

Yukiko Arai[1],   Yu Liu [1],   Haruo Kobayashi[1],   Tatsuji Matsuura[1],   Osamu Kobayashi [2]

Masanobu Tsuji[2],   Masafumi Watanabe[2] ,   Ryoji Shiota[2],   Noriaki Dobashi[2], Sadayoshi Umeda[2]

Isao Shimizu[1],   Kiichi Niitsu[3],   Nobukazu Takai[1],   Takahiro J. Yamaguchi[1]

[1]Gunma University   1-5-1 Tenjin-cho, Kiryu-shi, Gunma, 376-8515 Japan

[2]Semiconductor Technology Academic Research Center   Kohoku, Yokohama-shi, Kanagawa, 222-0033 Japan

[3] Nagoya University   Furo-cho, Chikusa-ku, Nagoya, 464-8601, Japan

E-mail: t13801404@gunma-u.ac.jp   k_haruo@el.gunma-u.ac.jp

Abstract   This paper presents an ADC architecture comprising a pipelined cyclic ADC and continuous-time delta-sigma ADC; it provides high resolution at medium speed, with small power requirements. It is also reconfigurable for different combinations of speed, precision, and power consumption. The cyclic ADC produces a residue after the final cycle, and the following delta-sigma ADC converts it to a digital value (the residue is then noise-shaped). The ADC output combines the digital outputs of the cyclic ADC and the delta-sigma ADC so as to achieve high resolution. The delta-sigma ADC can be implemented simply with continuous-time analog circuitry. We describe the overall ADC architecture and operation, show simulation results, and describe features such as its potential for reconfiguration.

Keyword   Cyclic ADC, Pipeline ADC, Delta-Sigma, Noise-Shaping

1.   Introduction

Real world signals such as light and sound are analog, so ADCs and DACs are essential for digital signal processing and data storage inside digital LSI circuits; hence ADC/DAC R&D is currently quite active [1][2]. We here propose a pipeline ADC architecture consisting of a cyclic ADC and a continuous-time delta-sigma ADC (where integrators are designed with Gm-C or active RC circuits instead of switched capacitor circuits) [3][4] to provide a good trade-off among speed, precision, and power consumption with relatively simple circuitry.

2.   Cyclic ADC

2.1 Architecture and operation of cyclic ADC

Fig. 1 shows the architecture of a cyclic ADC [5][6]. A 1-bit ADC (comparator) inside the cyclic ADC compares the analog input voltage Vin (Va) to a half of the reference voltage (V1lsb), and outputs a digital value Dout. Then a 1-bit Multiply-DAC (MDAC) outputs Vb depending on Dout and produces a residual value Va-Vb, which is amplified by 2. This 2 x (Va-Vb) is used as the input voltage Va to the next stage. This operation is repeated.

We see that, in principle, the cyclic ADC can achieve N-bit resolution (where N is an arbitrary positive integer) in N steps, using the same core circuit for each step. However its disadvantage is that it is not very efficient in terms of power and chip area, because the noise performance of the first stage must be good, but the core circuits (such as MDAC) have to be designed with large

MOSFETs and large bias currents, and these MOSFETs are also used in the latter stages where good noise performance is not as important as in the first stage.

Next we consider the residue voltage Vout (n) of the nth-stage.

$$V_{out}(n) = 2^n \times (V_{in} - K(n) \times V_{ref}). \qquad (1)$$

K(n) is the nth-bit digital output of the cyclic ADC. It is obtained by multiplying by digital output bit weight of each stage as follows:

$$K(\mathrm{n}) = (1/2)Dout(1) + (1/4)Dout(2)$$
$$+(1/8)Dout(3) + \cdots + (1/2^n)Dout(n) \qquad (2)$$

where $Dout(n) = 1 \quad (Va(n) \geq Vref/2)$

$Dout(n) = 0 \quad (Va(n) < Vref/2)$
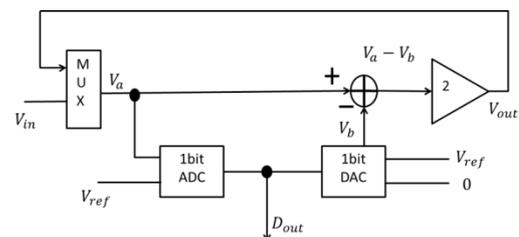
Fig.1 Cyclic ADC block diagram.

2.2 Noise Shaping Algorithm

Next we consider how to digitize the residue voltage Vout(n) using a following $\Delta\Sigma$ ADC. Since the cyclic ADC produces a difference (Va(n)-Vb(n)) between the analog input and the DAC output, it is straightforward to use the $\Delta\Sigma$ ADC to capture the quantization error (or residue Vout(n)).

We combine the $\Delta\Sigma$ ADC and cyclic ADC n-bit outputs in the

digital domain to cancel quantization error; this MASH 0-1 [3] method increases resolution by noise-shaping the residue of the Nyquist ADC using the following ΔΣ ADC, their outputs are added in the digital domain. We explain this noise-shaping algorithm as follows (Fig.2):

1) Quantization error e(n) of the cyclic ADC is given by

$$e(n) = V_a - V_b \tag{3}$$

2) We accumulate e(n) and obtain acc(n).

$$acc(n) = acc(n-1) + e(n) \tag{4}$$

3) When acc(n) is larger than 1LSB, we subtract 1LSB from acc(n) and add 1 to the total digital output.

If acc(n) > 1LSB, acc(n) = acc(n) − 1LSB $\tag{5}$

$$D_{out}(n) = D_{out}(n) + 1 \tag{6}$$

When acc(n) is not larger than 1LSB, we do not do anything.
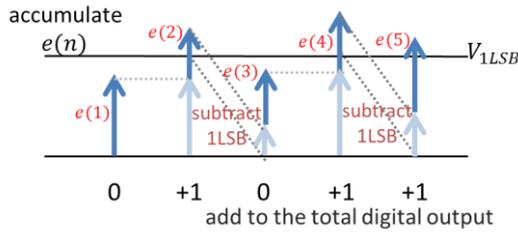
Fig. 2 Cyclic ADC residue accumulation (precisely ΔΣ modulation) with the ΔΣ ADC.

2.3 MASH 0-1 ΔΣ ADC

We consider the pipeline structure of the cyclic ADC and the first-order ΔΣ ADC in Fig.3. First the Nyquist (cyclic) ADC output is produced as follows:

$$Y_1(z) = X(z) + E_1(z). \tag{7}$$

Since the following ΔΣ ADC input is given by $-E_1(z)$, we have

$$Y_2(z) = -E_1(z) + (1/G_2)E_2(z). \tag{8}$$

To cancel quantization error $E_1(z)$, we have

$$H_1(z) = 1, \quad H_2(z) = 1.$$

Then we obtain the final digital output $Y(z)$.

$$\begin{aligned} Y(z) &= Y_1 H_1 + Y_2 H_2 \\ &= X(z) + E_1(z) - E_1(z) + (1/G_2) E_2(z) \\ &= X(z) + (1/G_2)E_2(z). \end{aligned} \tag{9}$$

Eq. (9) shows that $E_1(z)$ is canceled and $E_2(z)$ is filtered by $1/G_2$. We design G_2 as an integrator function, and thus $1/G_2$ is a high-pass filter function; this is used for noise-shaping $E_2(z)$.
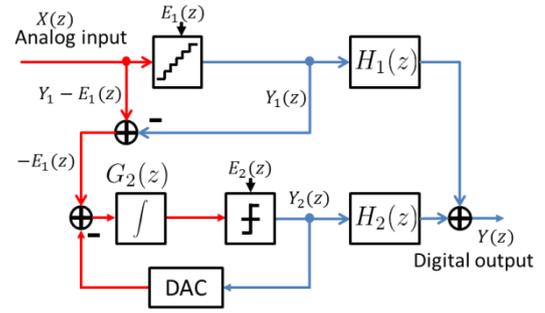
Fig.3 Nyquist ADC and ΔΣ ADC with MASH 0-1 structure.

2.4 Configuration of Noise-Shaping Cyclic ADC

Fig. 4 shows the configuration of our noise-shaping cyclic ADC. The ΔΣ ADC accumulates the quantization error of the cyclic ADC, and the accumulated quantization error is compared to the reference voltage V1LSB to check whether it is over 1LSB analog voltage. When it is over 1LSB analog voltage, the ΔΣ ADC outputs 1 and the accumulated error is subtracted by 1LSB analog voltage; otherwise it outputs 0. The ΔΣ ADC output is combined with the cyclic ADC output.
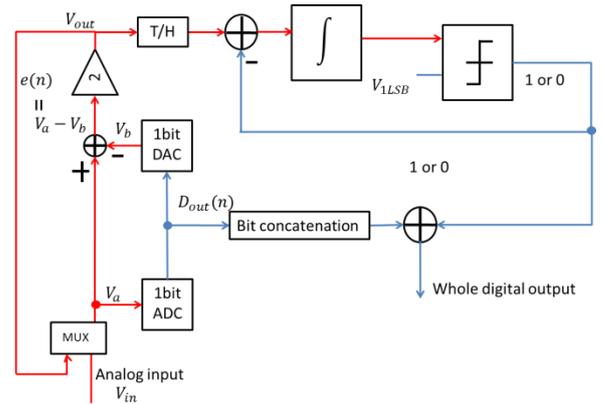
Fig. 4   Proposed noise-shaping cyclic ADC configuration.
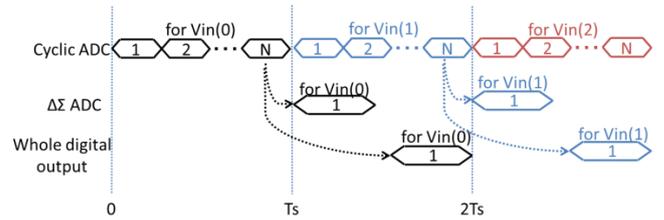
Fig. 5   Operation of the proposed noise-shaping cyclic ADC.

3.   Matlab Simulation

3.1 Noise-shaping cyclic ADC

We have performed Matlab simulation of the noise-shaping cyclic ADC, and Fig. 6 shows the results; Fig. 6 (a) shows the waveform reconstructed from the cyclic ADC output for a sinusoidal analog input, and Fig. 6 (b) shows that of the noise shaping cyclic ADC.

We have performed FFT of the noise-shaping cyclic ADC output

and obtained its frequency power spectrum (Fig. 7). We see that in Fig.7 (a) the noise is uniformly distributed, while in Fig. 7 (b), low frequency noise is decreased and high-frequency noise increased; in other words noise shaping is realized.

(a)   (b)

(c)   (d)
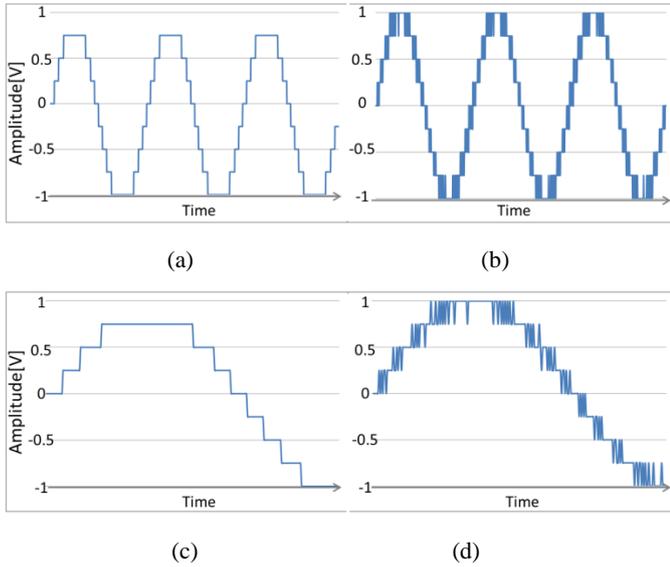
Fig. 6   Reconstructed digital output waveforms for a sinusoidal analog input.

(a) Output waveform from the cyclic ADC output.

(b) Output waveform from the noise-shaping cyclic ADC.

(c) Enlarged view of the output waveform from the cyclic ADC.

(d) Enlarged view of the output waveform from the noise-shaping cyclic ADC.

(a)   (b)
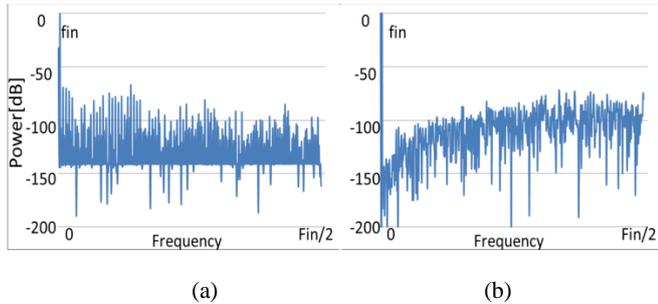
Fig. 7   ADC output power spectrum. (a) Power spectrum of the cyclic ADC output. (b) Power spectrum of the noise-shaping cyclic ADC output, where the quantization noise is shaped.

3.2 SQNDR evaluation

Signal-to-noise-and-distortion ratio (SNDR) is one important metric for ADC performance. Here we consider only quantization noise as "noise" and do not consider the other noises (such as thermal noise and 1/f noise) for system level design; we discuss here signal-to-quantization-noise-and-distortion (SQNDR). The graph in Fig. 8 shows SQNDR (y-axis) vs. over-sampling ratio (OSR) (x-axis); we see that the SQNDR of the noise-shaping cyclic

ADC is better than that of the cyclic ADC. Fig.9 explains OSR, defined as log2 (1/signal bandwidth x (2Ts)), where Ts is the ADC conversion period.
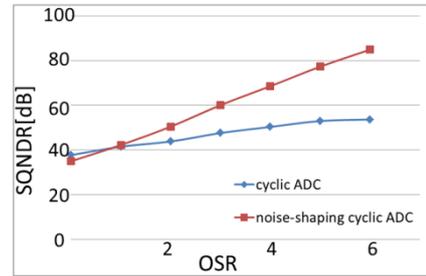
Fig. 8   SQNDR comparison of a 6-bit cyclic ADC and a noise-shaping cyclic ADC.
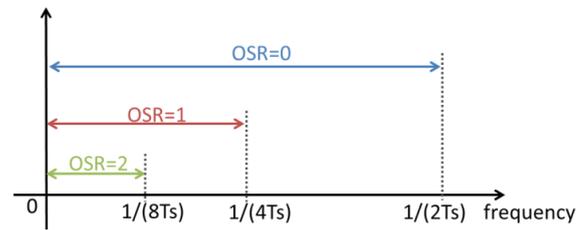
Fig. 9   Explanation of over-sampling ratio (OSR).

4.   ΔΣ ADC Operation

Now we consider improving the performance of the proposed ADC by increasing the operating frequency of the ΔΣ ADC. The cyclic ADC uses an MDAC, which employs an operational amplifier with associated capacitors; this is slow and consumes considerable power due to the feedback structure. The following ΔΣ ADC can be implemented using a fast, low-power open-loop Gm-C integrator; it may not be very linear, but this may be acceptable because the ΔΣ ADC produces only the lower-order bits. In the proposed technique described in previous sections, the quantization error of the cyclic ADC goes to the ΔΣ ADC after cyclic ADC operation completes. Since the ΔΣ ADC is used only once after N-cycle operation of the cyclic ADC; this is not very efficient.

So we propose multiple operations of the ΔΣ ADC during N-cycle operations of the cyclic ADC, to obtain high resolution. The ΔΣ ADC is fast, and it can operate at the same clock frequency as the cyclic ADC, or at an even higher clock frequency (say, twice the frequency) - i.e. while the cyclic ADC performs N cycles (N bits output), the ΔΣ ADC can perform N or 2N cycles.

4.1 ΔΣ ADC Multiple-Cycle Algorithm

Quantization error of the cyclic ADC is $e_1(n)$, as obtained from (3). Digital output after 1-cycle ΔΣ AD conversion of $e_1(n)$ is

given by $D_{\Delta\Sigma1}(n)$, and accumulated cyclic ADC quantization value (or $\Delta\Sigma$ ADC quantization error) is $e_2(n)$. When the accumulated value of $e_1(n)$ is larger than 1LSB, the $\Delta\Sigma$ ADC outputs $D_{\Delta\Sigma1}(n) = 1$, and subtracts 1LSB from the accumulated quantization error value. When it is smaller than 1LSB, the $\Delta\Sigma$ ADC outputs $D_{\Delta\Sigma1}(n) = 0$, and it does not do the subtraction. After 1-cycle $\Delta\Sigma$ AD conversion, $\Delta\Sigma$ ADC quantization error is given by $e_2(n)$. Fig.10 shows its operation.
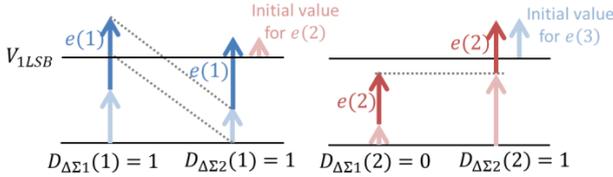
Fig. 10 $\Delta\Sigma$ modulation of a cyclic ADC residue.

In a 2-cycle $\Delta\Sigma$ ADC, quantization error $e_1(n)$ is accumulated and $e_1(n) + e_2(n)$ is obtained. Thus we can obtain $D_{\Delta\Sigma2}(n)$ and $e_2(n)$ as for the 1-cycle $\Delta\Sigma$ ADC. If the $\Delta\Sigma$ ADC performs N cycles, we obtain N digital outputs $D_{\Delta\Sigma1}(n)$, $D_{\Delta\Sigma2}(n)$, $\cdots$, $D_{\Delta\Sigma N}(n)$. We divide the N digital outputs by N to give the N-cycle $\Delta\Sigma$ ADC digital output $D_{\Delta\Sigma}(n)$. Then we add $D_{out}(n)$ and $D_{\Delta\Sigma}(n)$. Fig.11 shows the operation of the proposed architecture.
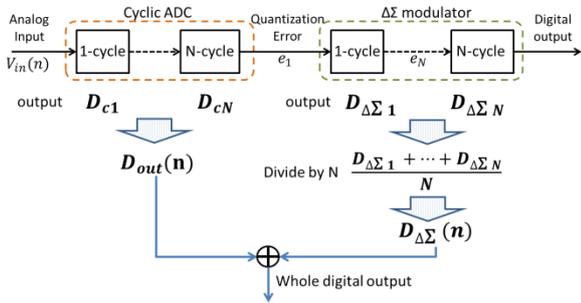
Fig. 11 Operation of the proposed architecture with a cyclic ADC followed by a multi-cycle $\Delta\Sigma$ ADC.

Fig. 12 shows the reconstructed output waveform of the noise-shaping 1-bit cyclic ADC. Fig. 12(a) shows 1-cycle $\Delta\Sigma$ AD conversion, and Fig. 12(b) shows 2-cycle $\Delta\Sigma$ AD conversion. Repeating the $\Delta\Sigma$ AD-conversion cycle increases the resolution.

Fig. 13 explains the pipeline operation of a 1-bit cyclic ADC and a 1-cycle $\Delta\Sigma$ ADC as well as a 2-cycle $\Delta\Sigma$ ADC, where Ts is an ADC conversion period. While the cyclic ADC performs 1-cycle operation, the $\Delta\Sigma$ modulator performs 1-cycle or 2-cycle operations.

(a)   (b)
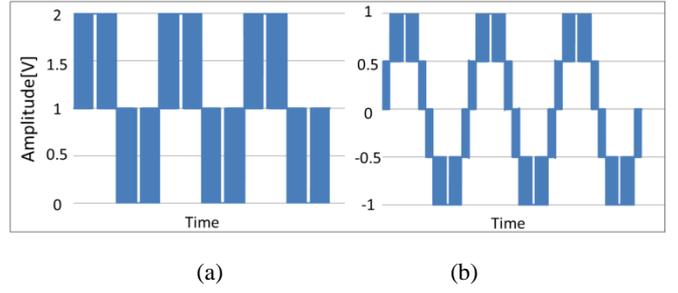
Fig. 12   Reconstructed output waveforms. (a) 1bit-cyclic ADC + 1-cycle $\Delta\Sigma$ ADC. (b) 1bit-cyclic ADC + 2-cycle $\Delta\Sigma$ ADC.
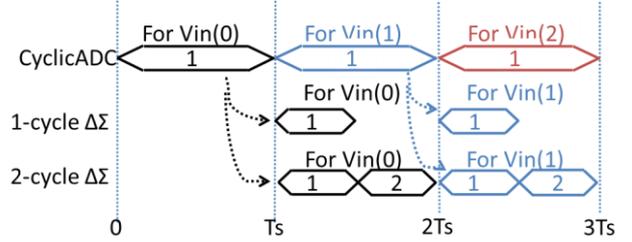
Fig. 13   Pipeline operation of a 1-bit cyclic ADC and a 1-cycle or 2-cycle $\Delta\Sigma$ ADC.

4.2   SQNDR and Over Sampling Ratio

Fig. 14 shows SQNDR versus Over-Sampling Ratio (OSR) of a noise-shaping 2-bit cyclic ADC and compares 1-cycle, 2-cycle, and 4-cycle $\Delta\Sigma$ AD conversions, obtained by Matlab simulation. With 2-cycle $\Delta\Sigma$ AD conversion, SQNDR is improved by 6 dB, while for 4-cycle $\Delta\Sigma$ conversion, it is improved by 12 dB. In Fig.14, ENOB stands for effective number of bits, which is calculated as follows:

$$\text{ENOB} = (\text{SQNDR} - 1.76)/6.02 \text{ [bits]} \qquad (10)$$

(a)   (b)
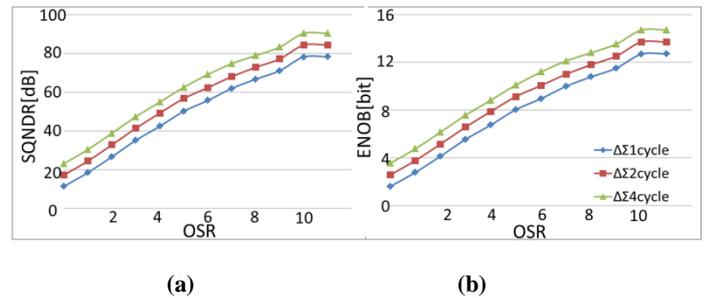
Fig. 14   Simulation results for a 2-bit cyclic ADC with following $\Delta\Sigma$ ADC. (a) SQNDR. (b) ENOB.

Next we show SQNDR of the noise-shaping 4-bit cyclic ADC and compare 1-cycle, 4-cycle, and 8-cycle $\Delta\Sigma$ AD conversion in Fig.15. 4-cycle $\Delta\Sigma$ AD conversion improves SQNDR by 12 dB, while 8 cycles improve it by 18 dB; it can achieve 6-bit resolution with 4-cycle $\Delta\Sigma$ AD conversion and 7-bit resolution with 8 cycles. So we can improve resolution by using more following $\Delta\Sigma$ ADC cycles.

Then we have the following SQNDR formula with respect to OSR, for the proposed architecture with an N1-bit cyclic ADC and an N2-cycle ΔΣ ADC (where $N2 = 2^{M2}$).

$$SQNDR = 6 \times (N1 + M2) + 2 + 9 \times OSR \text{ [dB]} \qquad (11)$$
$$ENOB = (N1 + M2) + 1.5 \times OSR \text{ [bits]} \qquad (12)$$

(a)   (b)
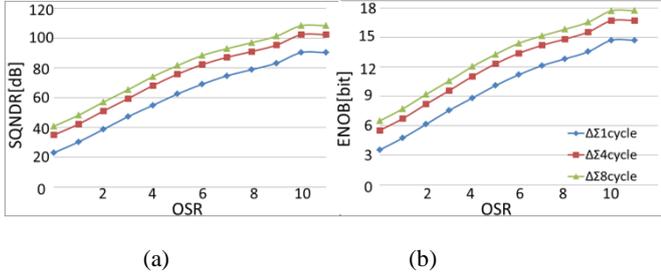
Fig.15   SQNDR simulation results of a 4-bit cyclic ADC with a following ΔΣ ADC. (a) SQNDR. (b) ENOB.

5.   Positioning of Proposed ADC

In this section we discuss the positioning of the proposed ADC. Let us consider an ADC using the proposed architecture whose signal band is from 0 to f_{BW} and resolution is K bits, and let us define the following:

   Ts: ADC conversion period

   N1: Number of cyclic operations during Ts.

   N2: Number of sampling clocks for the ΔΣ ADC during Ts.

      Let $N2 = 2^{M2}$.

Fig. 16 shows operation diagram; while the cyclic ADC performs N1-cycle operations, the ΔΣ ADC performs N2-cycle operations.
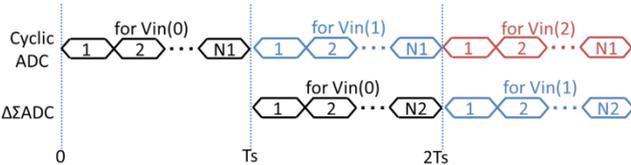
Fig. 16 Operation of the proposed ADC architecture.

We have the resolution K from eq.(12):

   K = N1 + M2 + 1.5 x OSR [bits]

Case 1: Cyclic ADC

Let us consider N1=12 and N2=0 (i.e., in case of only cyclic ADC (Fig.18)). We set the ADC conversion period Ts1 as

      Ts1 = 1/(8 f_{BW}).

Ideally Ts1 = 1/(2 f_{BW}) according to the sampling theorem, but due to the implementation requirement for an anti-aliasing filter, we assume Ts1 = 1/(8 f_{BW}).

Then each cyclic operation is performed in

   Tcyclic1=Ts1/12 = 1/(96f_{BW})
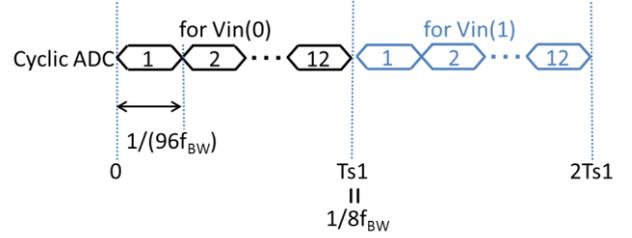
Fig. 17   Only cyclic ADC operation.
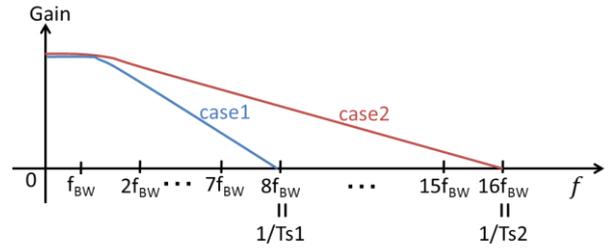
Fig. 18   Anti-aliasing filter requirements for cases 1 and 2.

Case 2: Proposed ADC

Next we consider using our architecture with N1=4 and N2=32 (M2=5), OSR=2 (where K=12 from eq.(12)) and we set the ADC conversion period as

   Ts2 = 1/(16f_{BW}).

Then each cyclic operation of the cyclic ADC is performed in

   Tcyclic2= Ts2/4 = 1/(64f_{BW}).

Fig. 19 shows simulation result where N1=4 and N2=32. In case of OSR=2, resolution achieves 11.2 bits.
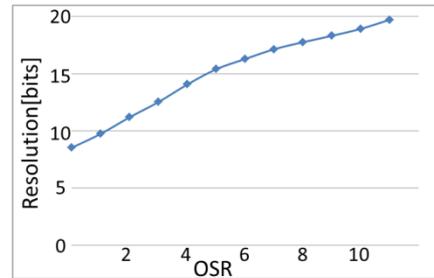
Fig. 19 Simulation result in case 2 (where N1=4 and N2=32).

Now let us compare cases 1 and 2.

(1) Cyclic ADC operation period comparison is given as follows:

      Tcycle2 = (96/64) Tcycle1 = 1.5 Tcycle1

   In the proposed architecture, each cyclic ADC operation duration is 1.5 times longer than in case 1, and hence the power of an operational amplifier in the MDAC, the most power-consuming part can be reduced.

(2) Also since OSR is 2 in the proposed architecture, the noise performance requirement of the cyclic ADC is reduced by 6dB as an input-referred noise, and also the anti-alias analog

filter requirement is relaxed; hence power can be reduced.

(3) The proposed ADC uses the ΔΣ ADC, but which is for lower-bit generation and hence which can be implemented with a simple Gm-C integrator due to the relaxed requirements.

Case 3: ΔΣ ADC

The first-order ΔΣ ADC needs N2=64 (M2=6), OSR=3 for K=10.5, and N2=128 (M2=7), OSR=4 for K=13bits. Hence a higher clock frequency is required. Also an RC active integrator (which is power consuming) as the first stage integrator instead of the Gm-C integrator or power-hungry switched capacitor circuits would be required to meet the requirement for high linearity.

Note that the cyclic ADC can achieve 12-bit resolution with 12 cycle operations but the ΔΣ ADC is difficult to obtain 12-bit resolution with 12 cycle operations even if a high-order/multi-bit modulator is used; in other words, the cyclic ADC has an advantage of achieving high-resolution with small operation cycles. Hence the proposed architecture can be considered as taking all advantages of the cyclic ADC and the ΔΣ ADC as well as the pipeline architecture.

The proposed ADC architecture is suitable for medium-to -high-resolution, medium-speed and low-power applications.

Remarks:

(i) The proposed noise-shaping cyclic ADC is inspired by the noise-shaping SAR ADC [7, 8].

(ii) In many pipelined ADCs, the clock frequency of each stage is the same. However, in the proposed ADC the clock frequencies of the cyclic and ΔΣ ADC parts can be different.

(iii) In the proposed architecture, the cyclic ADC is used for higher bits and the ΔΣ ADC is used for the remaining lower bits; this makes it suitable for use as a reconfigurable ADC [9]. The core circuits in the cyclic ADC part can be reconfigured for different resolution (though bias currents need to be different for best noise performance) and the ΔΣ ADC part can also be reconfigured for different combinations of bandwidth and resolution. Many parameters may be changed to optimize the combination of resolution, bandwidth, and power characteristics.

(iv) Non-binary algorithms [10] can be used in the cyclic ADC part to improve reliability.

6. Conclusion

We have presented a noise-shaping cyclic ADC architecture which combines a cyclic ADC and a ΔΣ ADC in pipeline manner, and we have validated its operation by Matlab simulation. Quantization error of the cyclic ADC can be noise-shaped (reduced around the input frequency band) by the following ΔΣ ADC.

We believe that the ΔΣ ADC can be designed with simple continuous-time analog circuitry with fast operation and low power. The cyclic ADC can be reconfigured without modifying its core circuits, and the ΔΣ ADC can be "tuned" for trade-offs between speed (signal band) and resolution. Therefore the proposed architecture is potentially very flexible and reconfigurable for trade-offs among speed (bandwidth), resolution, and power.

REFERENCES

[1] F. Maloberti, *Data Converters,* Springer (2007).

[2] R. J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters,* Springer (2010).

[3] R. Schreier, G. C. Temes, *Understanding Delta-Sigma Data Converters,* Wiley (2005).

[4] M. Uemori, H. Kobayashi, T. Ichikawa, A. Wada, K. Mashiko, T. Tsukada, M. Hotta, "High-Speed Continuous-Time Subsampling Bandpass ΔΣAD Modulator Architecture", IEICE Trans. Fundamentals, E89-A, no.4, pp.916-923 (April 2006).

[5] S. Kawahito, "Column-parallel A/D Converters for CMOS Image Sensors", IEEE Asia Pacific Conference on Circuits and System, Kuala Lumpur (Dec.2010)

[6] T. Watabe, K. Kitamura, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, N. Egami, "A 33Mpixel 120fps CMOS Image Sensor Using 12b Column-Parallel Pipelined Cyclic ADCs", IEEE Int. Solid-State Circuits Conf. pp.388-389, San Francisco (Feb.2012).

[7] J. Fredenburg, M. P. Flynn, "A 90MS/s 11MHz Bandwidth 62dB SQNDR Noise-shaping SAR ADC", IEEE International Solid-State Circuits Conf. pp. 468-469, San Francisco (Feb. 2012).

[8] J. Fredenburg, M. P. Flynn, "A 90MS/s 11MHz Bandwidth 62dB SQNDR Noise-shaping SAR ADC", IEEE Journal of Solid-State Circuits, vol.47, no.12   pp. 2898-2904 (Dec. 2012).

[9] T. Ogawa, H. Kobayashi, Y. Tan, S. Ito, S. Uemori, N. Takai, K. Niitsu, T. J. Yamaguchi, T. Matsuura, N.Ishikawa, "SAR ADC That is Configurable to Optimize Yield", IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia (Dec. 2010).

[10] T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, H. San, T. Matsuura, A. Abe, K. Yagi, T. Mori, "SAR ADC Algorithm with Redundancy and Digital Error Correction", IEICE Trans. Fundamentals, vol.E93-A, no.2, pp.415-423 (Feb. 2010).