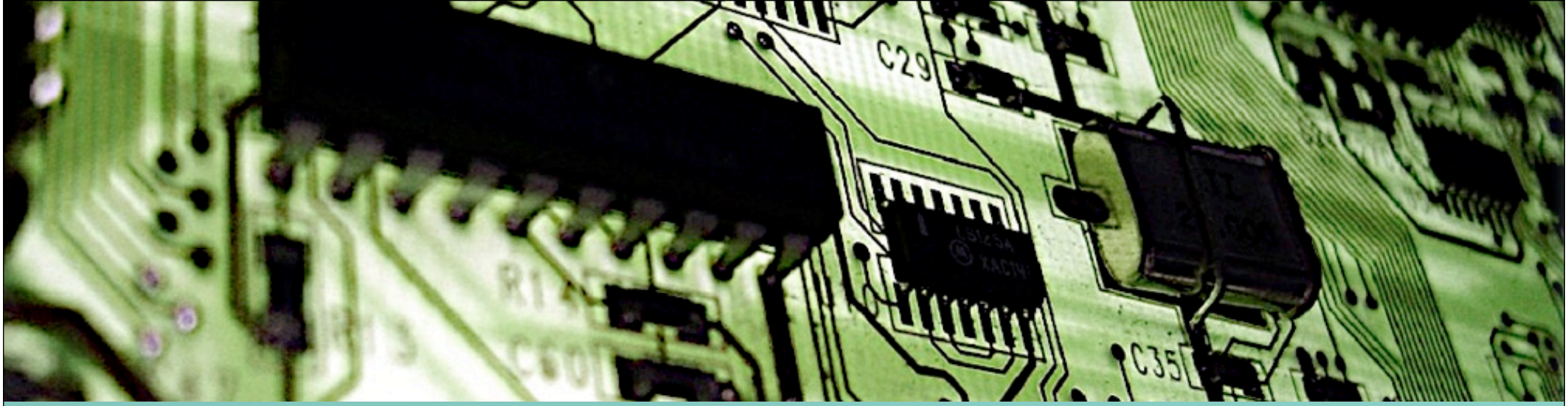

Automatic Synthesis of Comparator Circuit Using Genetic Algorithm

Takayuki NEGISHI, Naoki ARAI, Nobukazu TAKAI,

Masato KATO, Hiroaki SEKI, Sumit Kumar BISWAS and Haruo KOBAYASHI

Gunma University, Japan

16th November 2013

OUTLINE

- Background and Objective
- Method of Automatic Synthesis
- Result of Automatic Synthesis
- Summary and Future Work

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- Background and Objective
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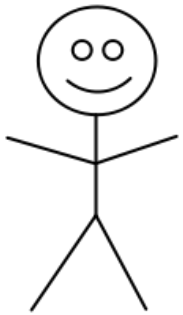
- Result of Automatic Synthesis
- Summary and Future Work

Research Background

「Engineer of Analog Circuit」



Time required for designing circuit

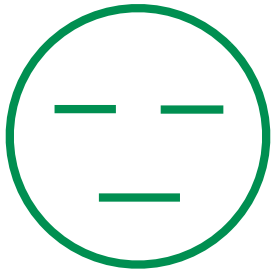
- Selection : Proper Circuit Topology
- Determination : Circuit Parameter Values
- Accumulation : Knowledge and Experience

Take time to become a good circuit designer

Industry Demands

- Short Time to Market
- Cost Reduction

Short time to development



DILEMMA

Research Background

「Automatic Design by Computer」

Time required for designing circuit

- Programming Time
- Execution Time

It can be designed in a shorter time than engineer

Industry Demands

- Short Time to Market
- Cost Reduction

Short time to development

Compatible

Research Objective

Comparator circuit is always used for signal comparison.

- **Short Time to Market**
- **Cost Reduction**

Merit of automatic synthesis!

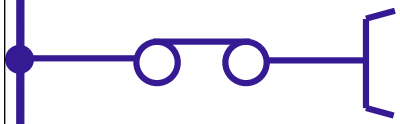
Electrical Characteristics of Comparator

- ☑ **Input-offset voltage**
- ☐ Input-offset current
- ☐ Input bias current
- ☑ **Current consumption**
- ☐ CMRR
- ☐ PSRR
- ☑ **Response time**

We realize automatic synthesis focusing on 3 characteristics!

OUTLINE

Background and Objective



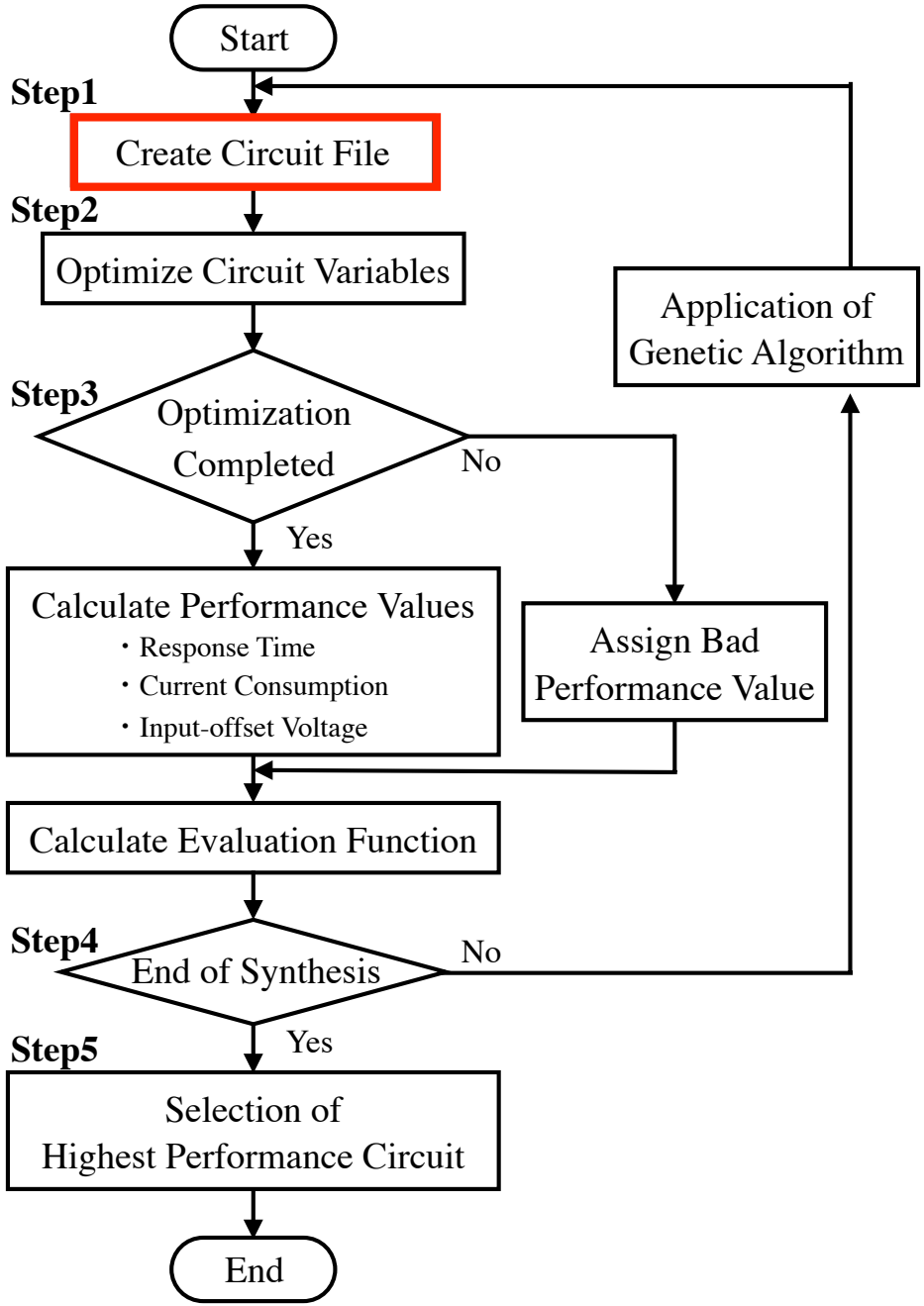
Method of Automatic Synthesis

Result of Automatic Synthesis

Summary and Future Work

Overview of Automatic Synthesis

※ Java-language programming



Step1

Create circuit file.

HSPICE input file format

preparation for variable parameters.

Step2

Determines proper values

that satisfies the setting condition

using HSPICE optimizing function.

Step3

< Performance reach the demand (Yes) >

Determines performance values.

< Performance don't reach the demand (No) >

Circuit topology is considered as "**bad**".

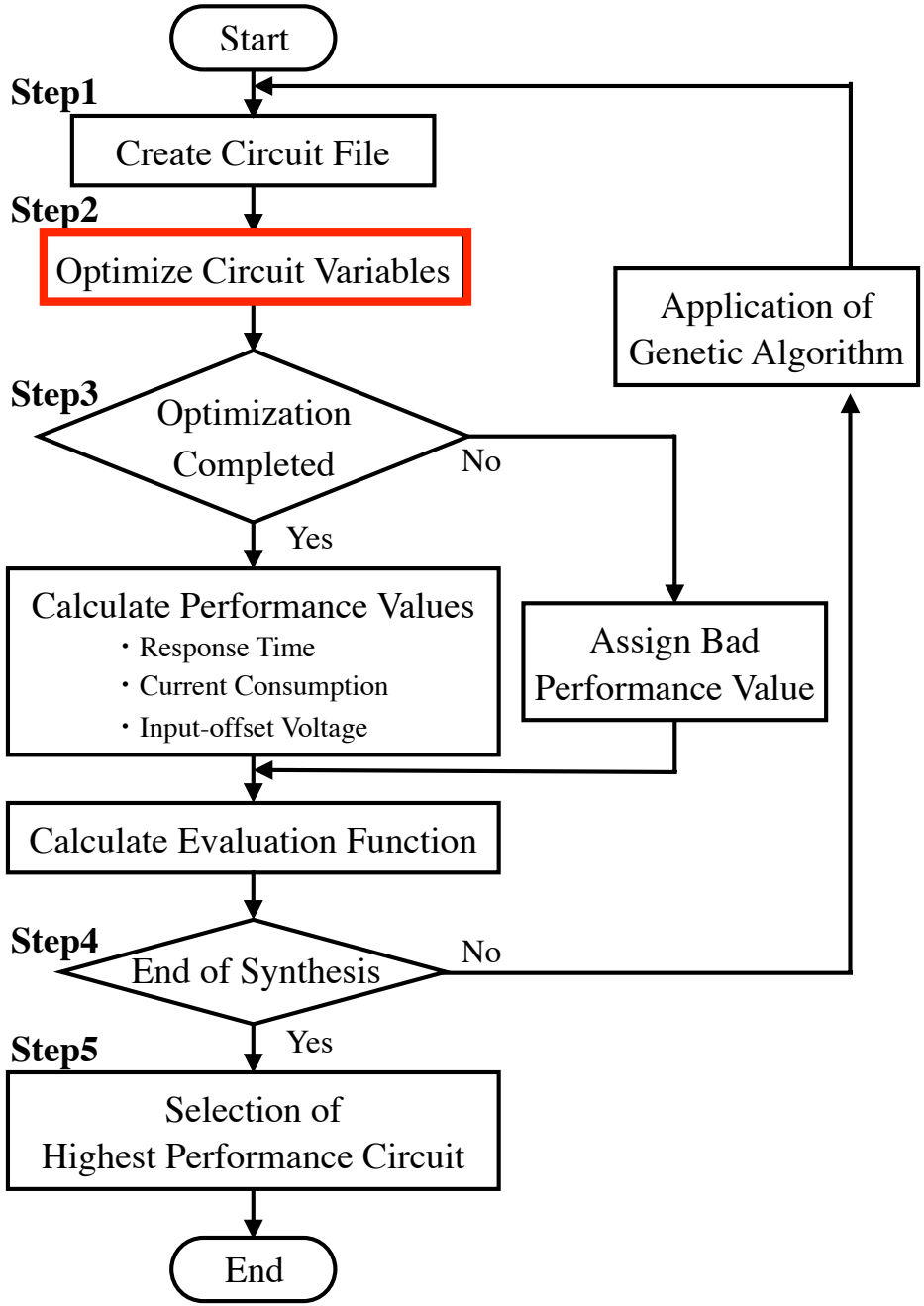
⇩

Calculate evaluation function

as circuit performance figure.

Overview of Automatic Synthesis

※ Java-language programming



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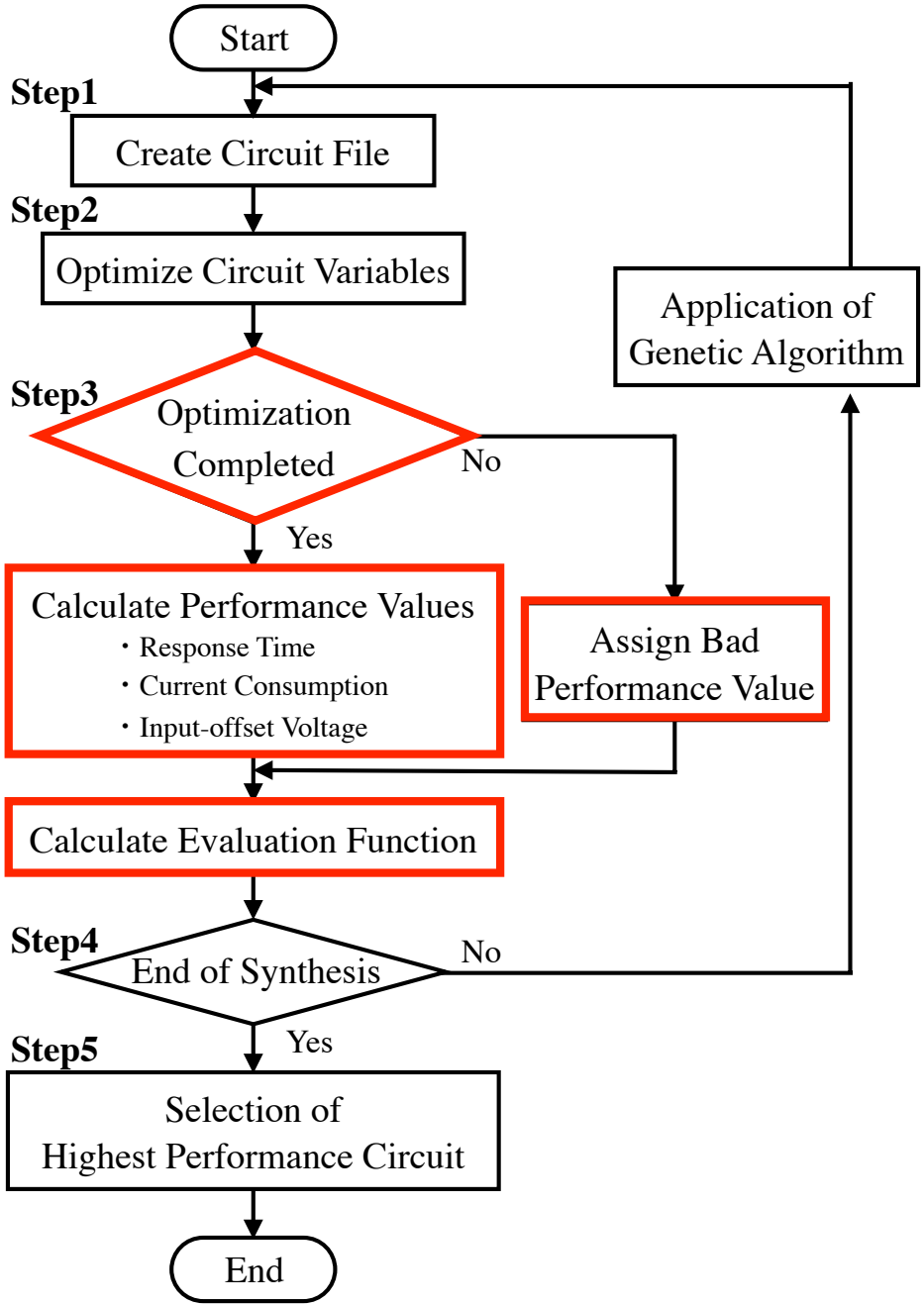
※ Java-language programming



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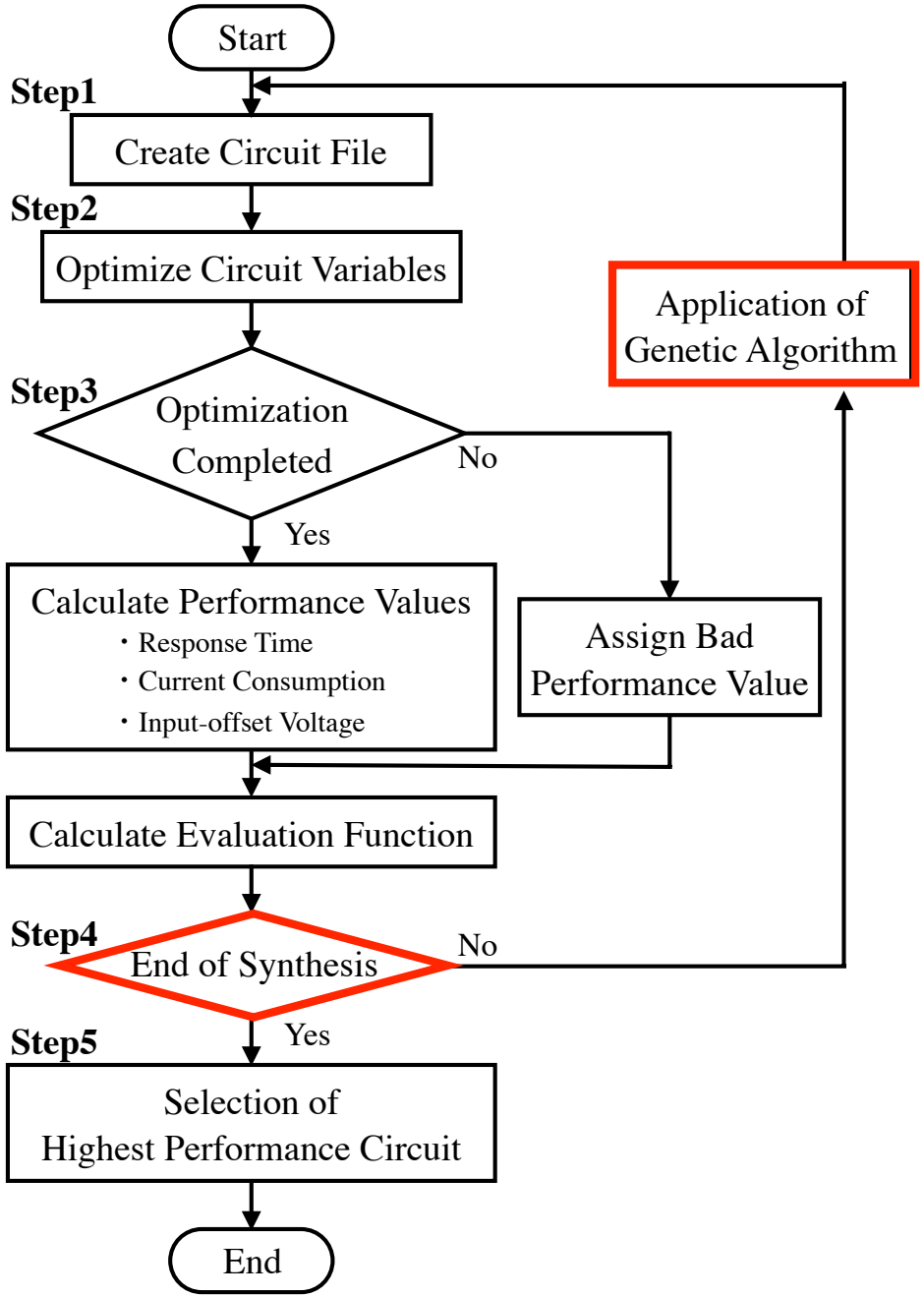
Overview of Automatic Synthesis



Step4

Increment loop number by 1.

< Loop number is less than the specified value >

Change another topology using GA.

Go to Step 1.

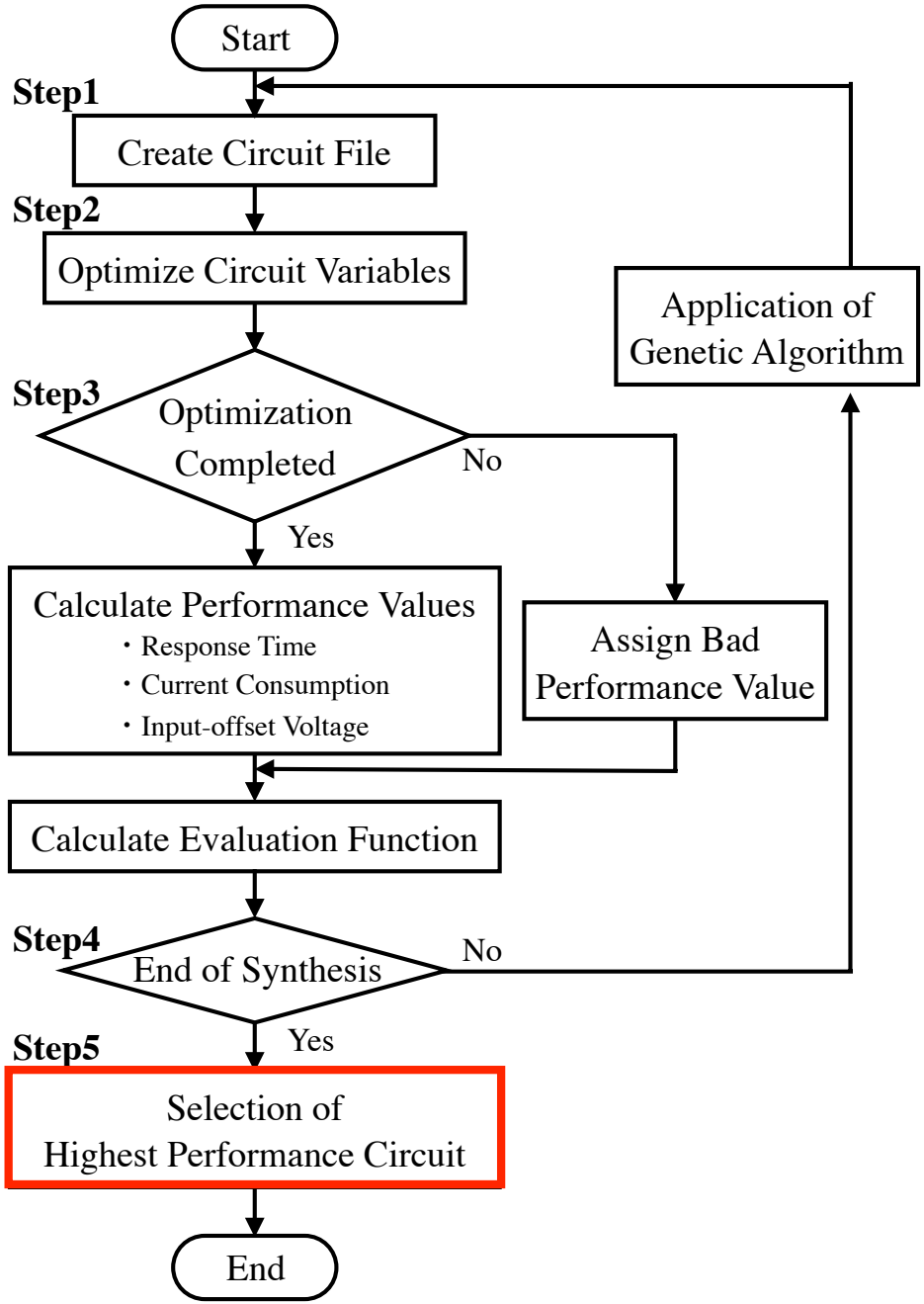
< Loop number is equal to the specified value >

Go to step 5.

Step5

Select the highest performance circuit among all of evaluated circuits.

Overview of Automatic Synthesis



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Go to Step 1.

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Step5

Select the highest performance circuit among all of evaluated circuits.

Create Circuit File to Use HSPICE

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit

Describe circuit information to run HSPICE

(Ex)

```
Comparator_001

.lib './contest.lib' model1

.OPTION INGOLD=2 NUMDGT=5 MEASDGT=5

M01 n03 n02 vdd vdd cmosp l=2.41u w=30.8u
M02 n04 inp  out  vss  cmosn l=49.8u w=48.4u
M03 out  n03 n04 vss  cmosn l=31.2u w=49.3u
M04 n01 vss  vdd vdd cmosp l=7.00u w=26.6u
M05 out  n02 n01 vdd cmosp l=0.25u w=2.34u
M06 out  inm vss  vss  cmosn l=7.30u w=18.0u
M07 n02 inp  vdd vdd cmosp l=14.2u w=3.52u
C08  out  n03 1p
R09  n02 vss  100

Vdd vdd gnd dc 1.5
Vss  gnd vss  dc 1.5

.lib 'Lib_Delay.lib' Delay

.end
```

Title

Reading a MOS model file

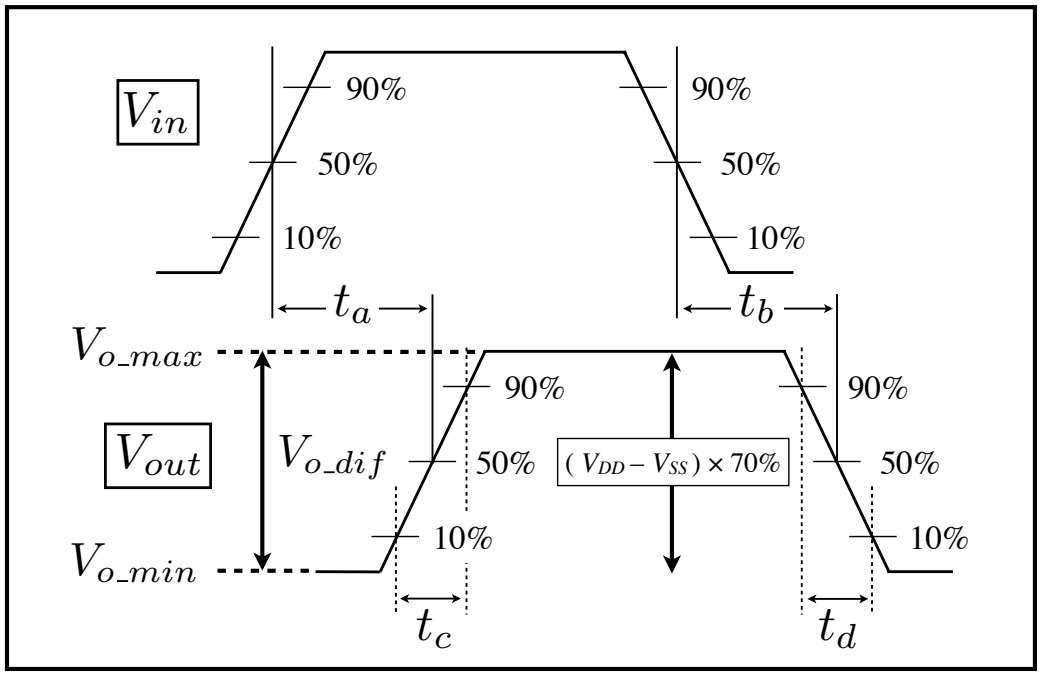
Circuit Topology & Circuit Parameter Values

Reading an analysis method file

How to Optimize

STEPs : Create Circuit File → Optimize Circuit Variables → Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit

Optimization uses response time



Goal

All response time parameters to 0.0 second

t_a, t_b, t_c, t_d

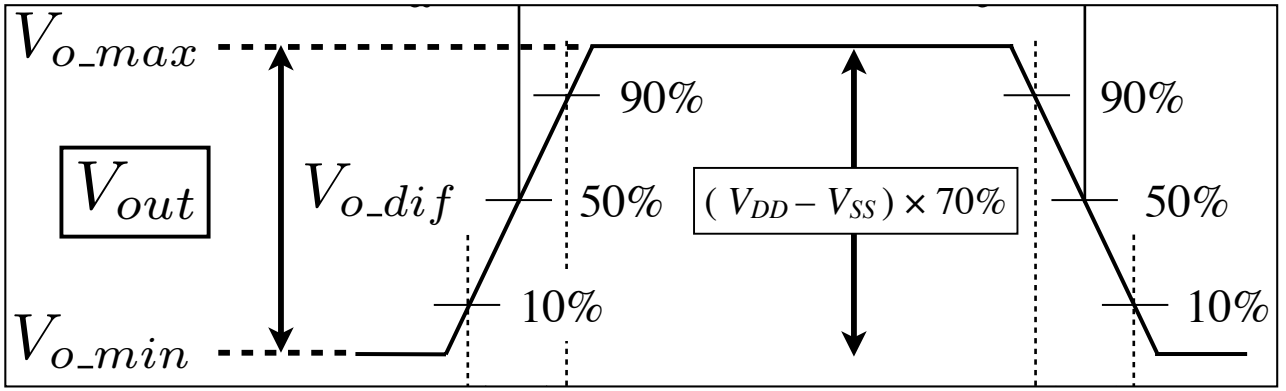
Output voltage difference(V_{o_dif}) to 70% of "$V_{DD}-V_{SS}$"

Target

MOSFET：Gate length and width

Judging Optimization

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit



$$V_{o\_dif} = V_{o\_max} - V_{o\_min}$$

Judgment Conditions

$$(V_{DD} - V_{SS}) \times 50\% \leq V_{o\_dif} \leq (V_{DD} - V_{SS})$$

$$V_{o\_max} \leq V_{DD}$$

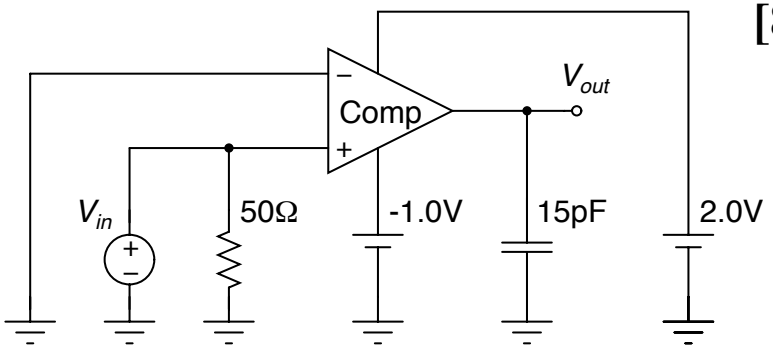
$$V_{SS} \leq V_{o\_min}$$

Only circuit that satisfied all conditions
→ Calculate performance values

Calculate Performance Value

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit

[8]



Input Pulse(V_{in})：200mV/μs [-0.1V~0.1V]

Calculated Items

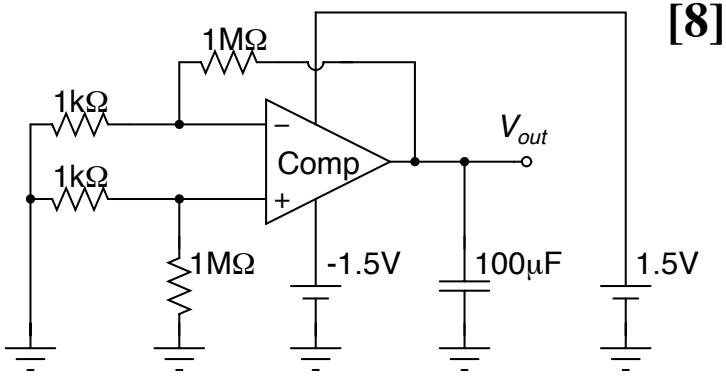
「**Output Voltage Difference**」：V_{o_dif}

「**Propagation Delay Time**」：$(t_a + t_b)/2$

「**Output Voltage Transition Time**」：$(t_c + t_d)/2$

「**Current Consumption**」：
Effective current value in 1 cycle of input pulse

[8]



Calculated Item

「**Input-offset voltage**」：V_{out}

[8] Renesas Electronics. HA1631S01/02/03/04.
http://documentation.renesas.com/doc/products/linear/rjj03d0044ha1631s01.pdf, 2006.

Calculate Evaluation Function

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit

Represent a Number for Circuit Performance

「Performance Values : s_k」
「Target Values : t_k」

- Output voltage difference : s_1 , t_1
- Propagation delay time : s_2 , t_2
- Output voltage transition time : s_3 , t_3
- Current consumption : s_4 , t_4
- Input-offset voltage : s_5 , t_5

Evaluation Item	Target Value
Output voltage difference	≥ 2.0V
Propagation delay time	≤ 168ns
Output voltage transition time	≤ 144ns
Current consumption	≤ 5.65mA
Input-offset voltage	≤ 59.6mV

「Evaluation Values : E_k」

Type1

$$E_1 = \begin{cases} \frac{s_1}{t_1} & (s_1 \le t_1) \\ 1 + \log\left(\frac{s_1}{t_1}\right) & (s_1 > t_1) \end{cases}$$

Type2

$$E_{2,\ldots,5} = \begin{cases} \frac{t_{2,\ldots,5}}{s_{2,\ldots,5}} & (s_{2,\ldots,5} > t_{2,\ldots,5}) \\ 1 + \log\left(\frac{t_{2,\ldots,5}}{s_{2,\ldots,5}}\right) & (s_{2,\ldots,5} \le t_{2,\ldots,5}) \end{cases}$$

「Fitness Value : F」

$$F = \prod_{k=1}^{5} E_k$$

Evaluation Function

Genetic Algorithm (GA)[6]

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit

Genetic Algorithm

Construction based on the laws of heredity in the real world.

Change a comparator circuit topology.

- 「**Selection**」 → Choose preferentially higher *F* (circuit performance).
- 「**Mutation**」 → Change circuit topology.

Item	Value
Population(N_p)	30
Generation	200
Crossover rate	0%
Mutation rate	30%

＜ GA conditions for automatic synthesis ＞

Population(N_p) :
Circuit topology number generated by the same loop

Generation :
Loop number

[6] D.E.Goldberg and K.Sastry. *Genetic Algorithms:The Design of Innovation, 2nd edition.* Springer, 2010.

Selection

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (**Selection**, Mutation) → Selection of The Highest Performance Circuit

Superior gene survives, Inferior gene weeds out.

Fitness Proportion Selection

Choose preferentially higher *F* (circuit performance).

「Expectation (topology k is selected as next-generation) 」

$$\frac{F_k}{\Sigma_k F_k / N_p} = \frac{F_k}{\bar{F}}$$

k : 1,..., N_p
N_p : Population (Circuit topology)
$\bar{F}$: Mean of fitness value

(Ex)

Fitness@N-th generation → **Expectation selected@(N+1)-th generation**

F_1=1, F_2=3, F_3=5, F_4=7, F_5=9

$\bar{F} = 5 (= \frac{1+3+5+7+9}{5})$

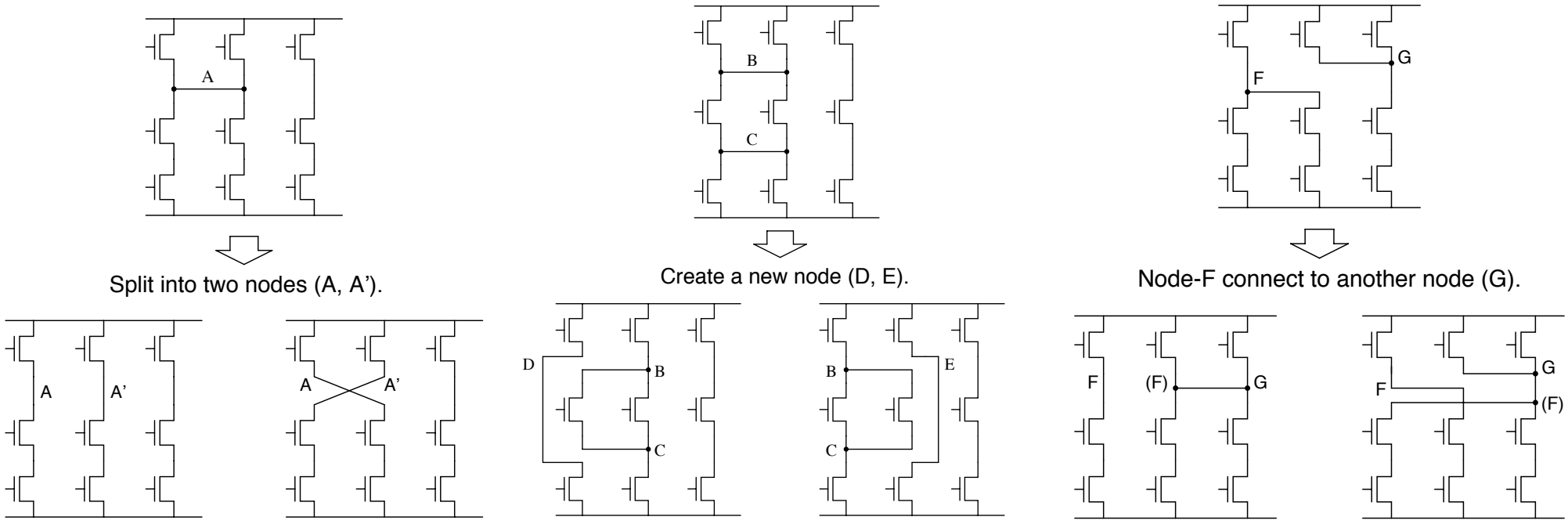
F_1=1/5, F_2=3/5, F_3=1, F_4=7/5, F_5=9/5

High performance (F_4, F_5) is easy to survive.

Mutation

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, **Mutation**) → Selection of The Highest Performance Circuit

Consider 3 type mutations to change circuit topology.



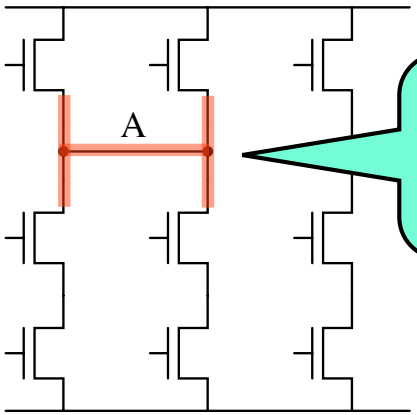
Change topology if such a connection exists.

※ Take care of not producing floating node.

Mutation - Case 1

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, **Mutation**) → Selection of The Highest Performance Circuit

Before

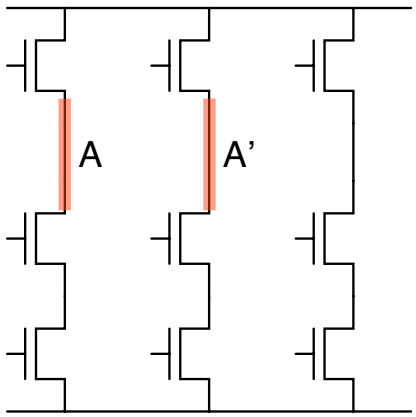


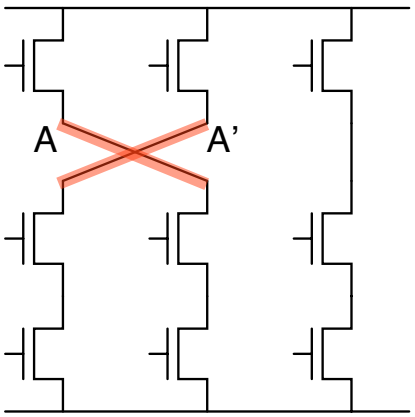
There is an H-type node

Node-A is H-type

Split into two nodes (A, A')

After

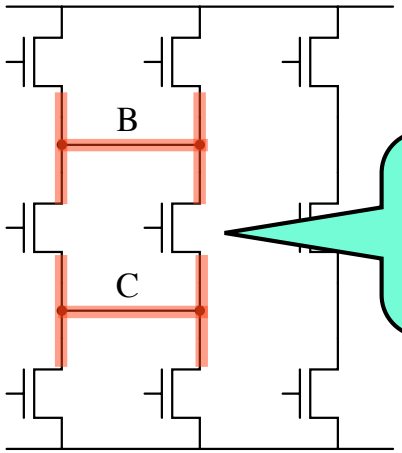




Mutation - Case 2

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, **Mutation**) → Selection of The Highest Performance Circuit

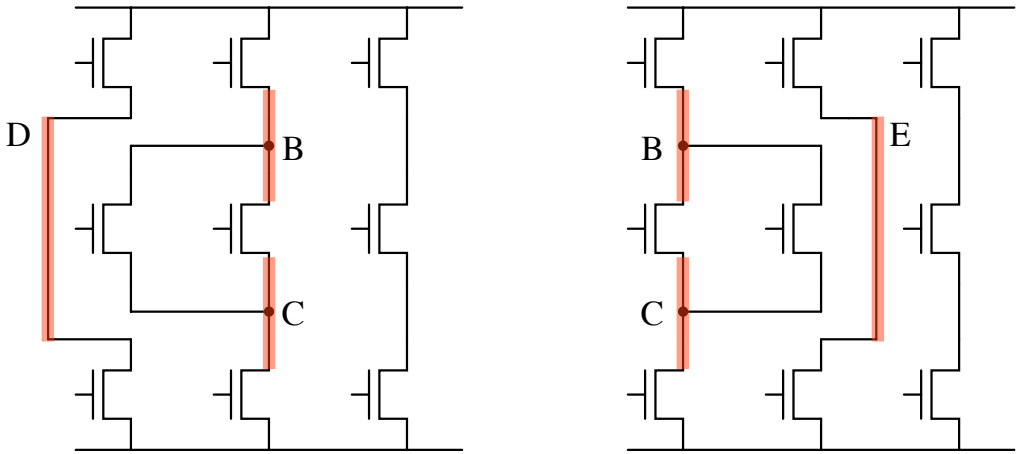
Before



There are two H-type nodes

Create new nodes (D, E).

After

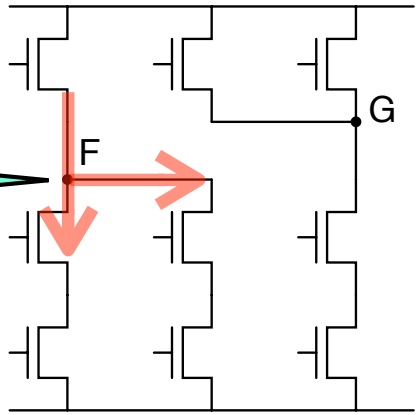


Mutation - Case 3

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, **Mutation**) → Selection of The Highest Performance Circuit

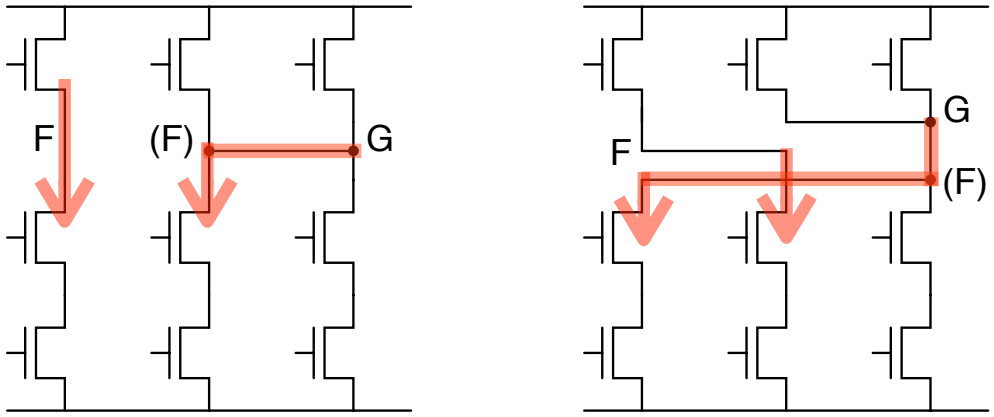
Before

If current path split into two



Node-F connected to another node (G).

After



OUTLINE

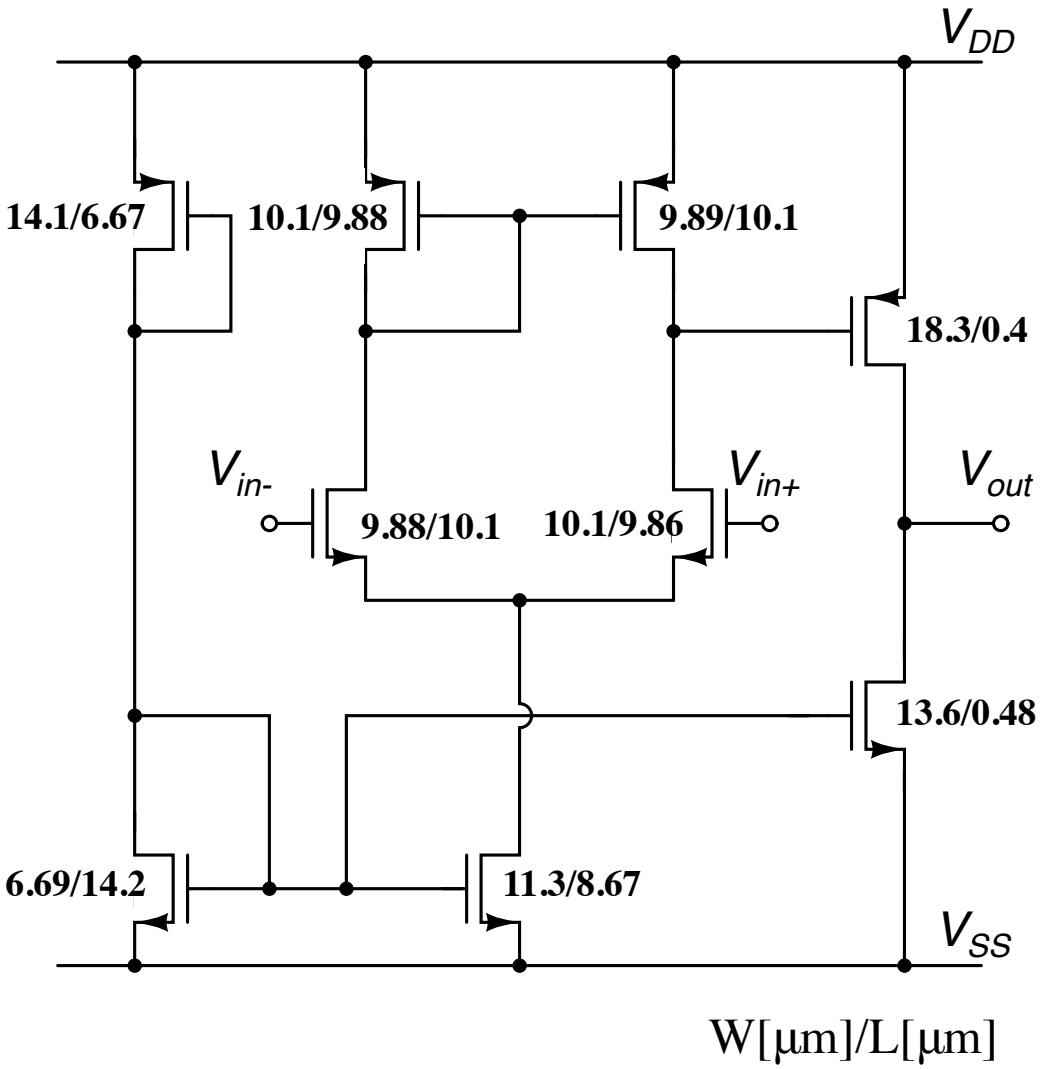
Background and Objective

Method of Automatic Synthesis

Result of Automatic Synthesis

Summary and Future Work

Initial Circuit



W[μm]/L[μm]

< Initial Circuit >

Required initial circuit in this study.

Evolve into high-performance topology using GA.

← basic comparator circuit.

Supply Voltage

V_{DD} = 1.5V

V_{SS} = –1.5V

Bulk

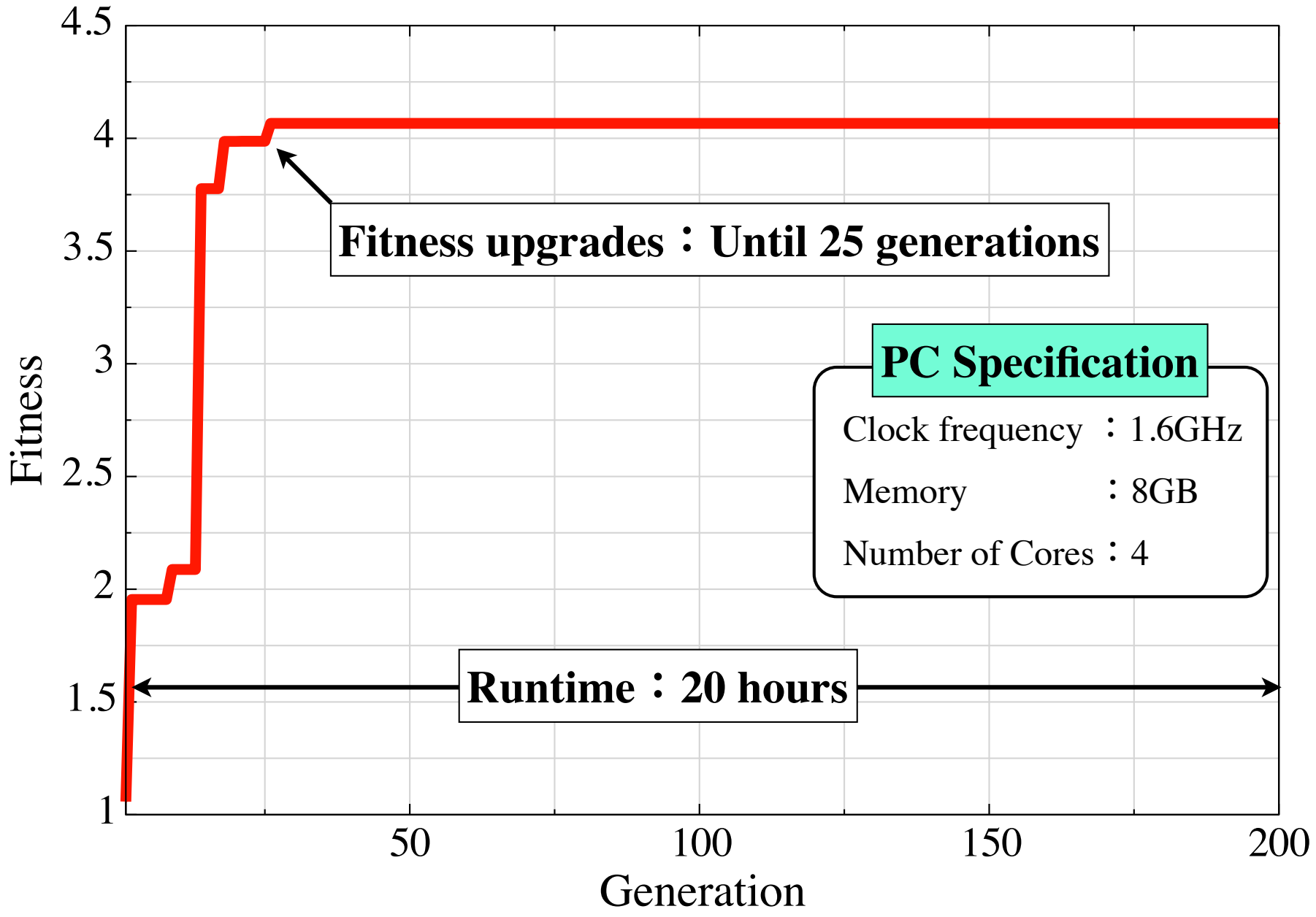
PMOS : V_{DD}

NMOS : V_{SS}

Technology

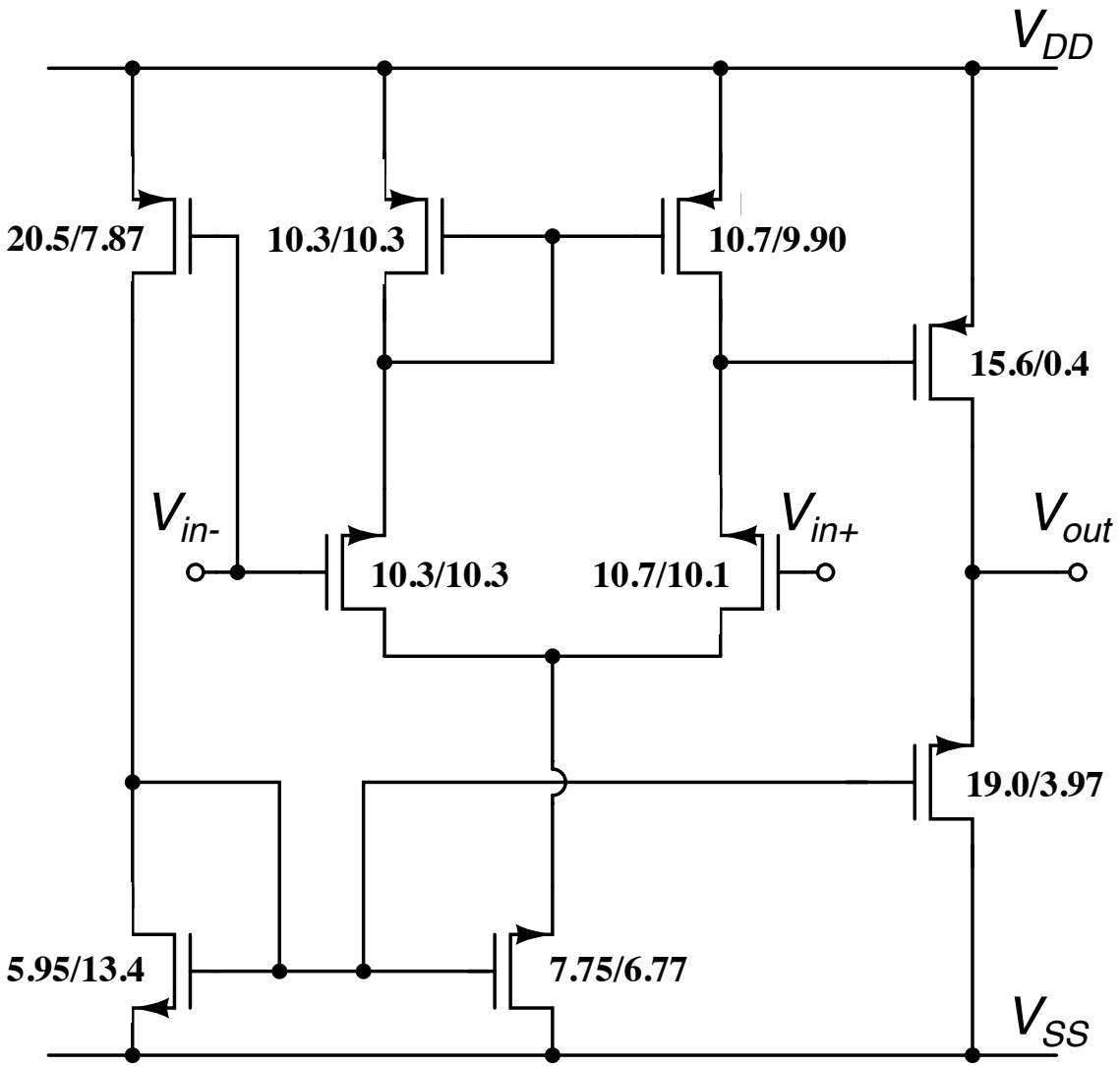
TSMC 180nm CMOS Process

Transition of the Maximum *F*



Best Performance Circuit

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit



W[μm]/L[μm]

Supply Voltage

V_{DD} = 1.5V

V_{SS} = –1.5V

Technology

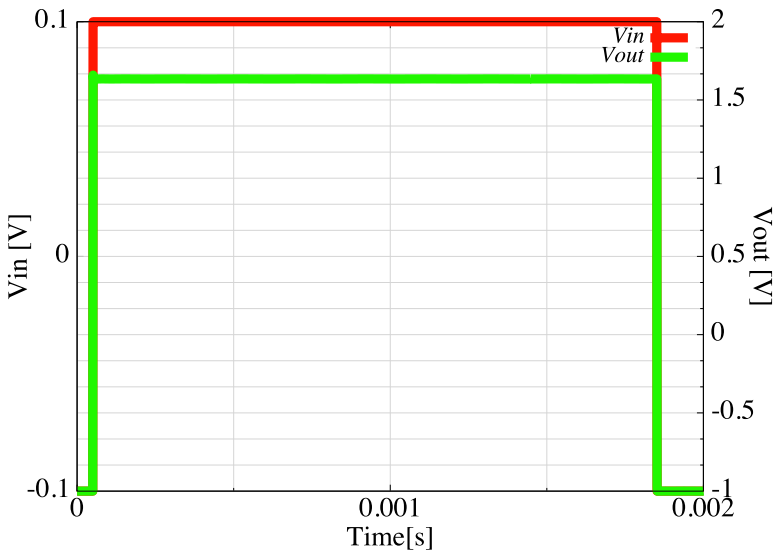
TSMC 180nm CMOS Process

Bulk

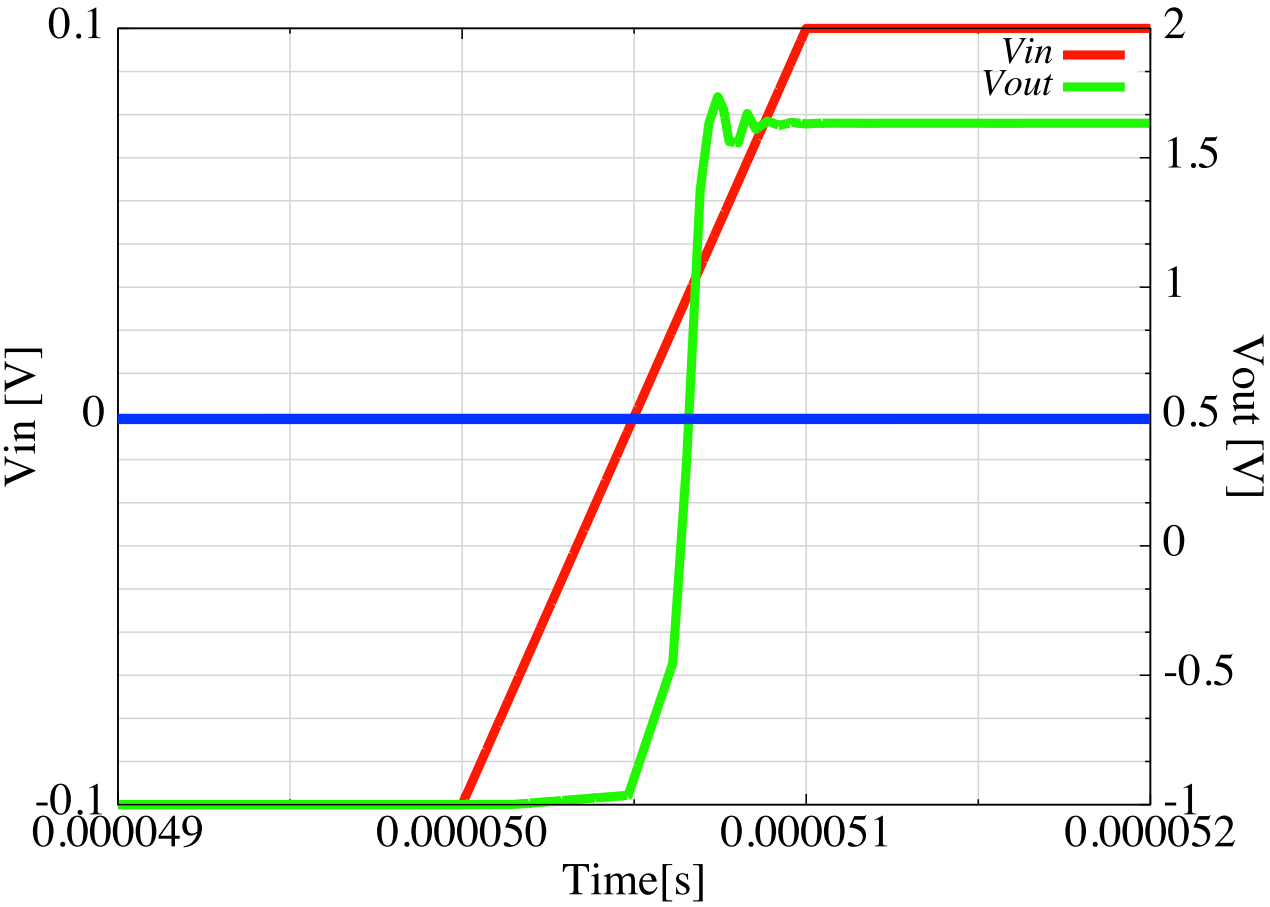
PMOS : V_{DD}
NMOS : V_{SS}

Input & Output Waveforms

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit



Enlarged view of rising part



Input & Output Waveforms

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
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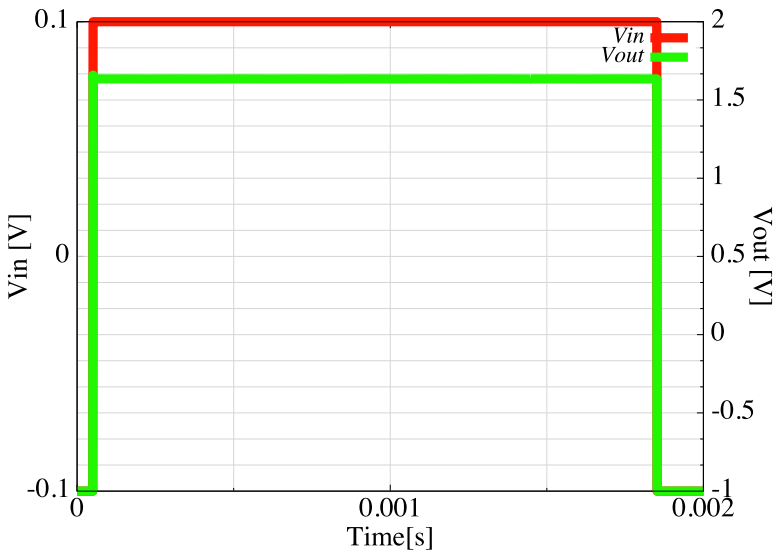
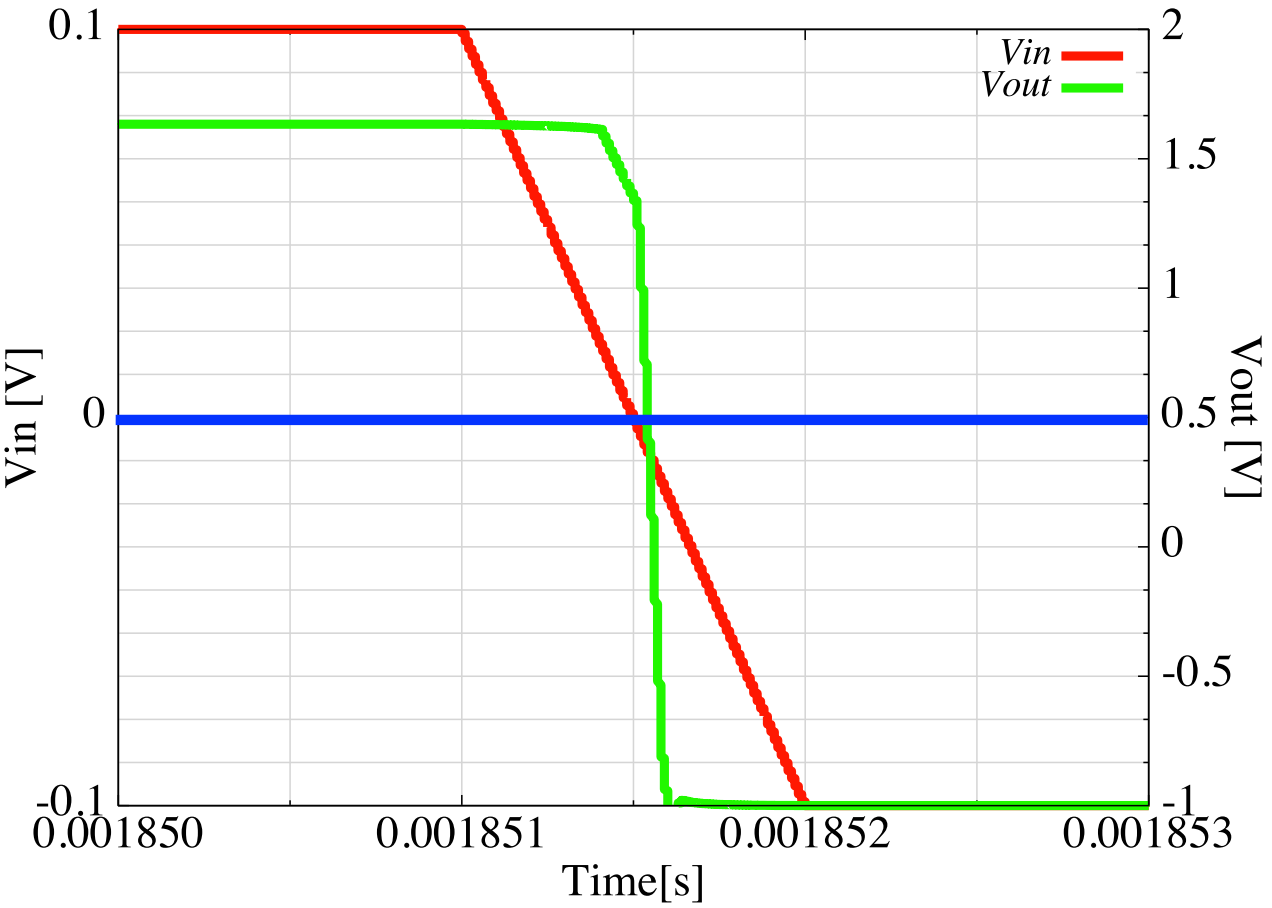


Enlarged view of falling part



Performance Comparison

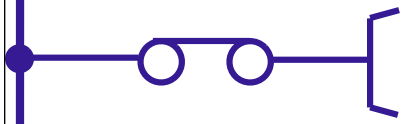
Evaluation Item	Value Type	Initial Circuit	Final Circuit
Output voltage difference	Performance	2.29V	2.72V
	Evaluation	1.06	1.13 ○
Propagation delay time	Performance	168ns	73.7ns
	Evaluation	1.0	1.36 ○
Output voltage transition time	Performance	144ns	272ns
	Evaluation	1.0	0.72 △
Consumption current	Performance	5.65mA	1.48mA
	Evaluation	1.0	1.58 ○
Input-offset voltage	Performance	59.6mV	3.0mV
	Evaluation	1.0	2.3 ◎
Fitness value (product of all evaluation)		1.06	4.06

OUTLINE

Background and Objective

Method of Automatic Synthesis

Result of Automatic Synthesis



Summary and Future Work

Summary & Future Work

- **Develop automatic synthesis program.**
  - Synthesize circuit topology
  - Determine circuit parameters
  - Simulation
  - Performance evaluation
- **HSPICE optimizing function determines circuit parameters.**
- **GA determines the circuit topology.**
- **Synthesized circuit performance is better than initial circuit.**

- Realize automatic synthesis of comparator from its *faulty* initial circuit.
- Silicon prototype of synthesized circuit.

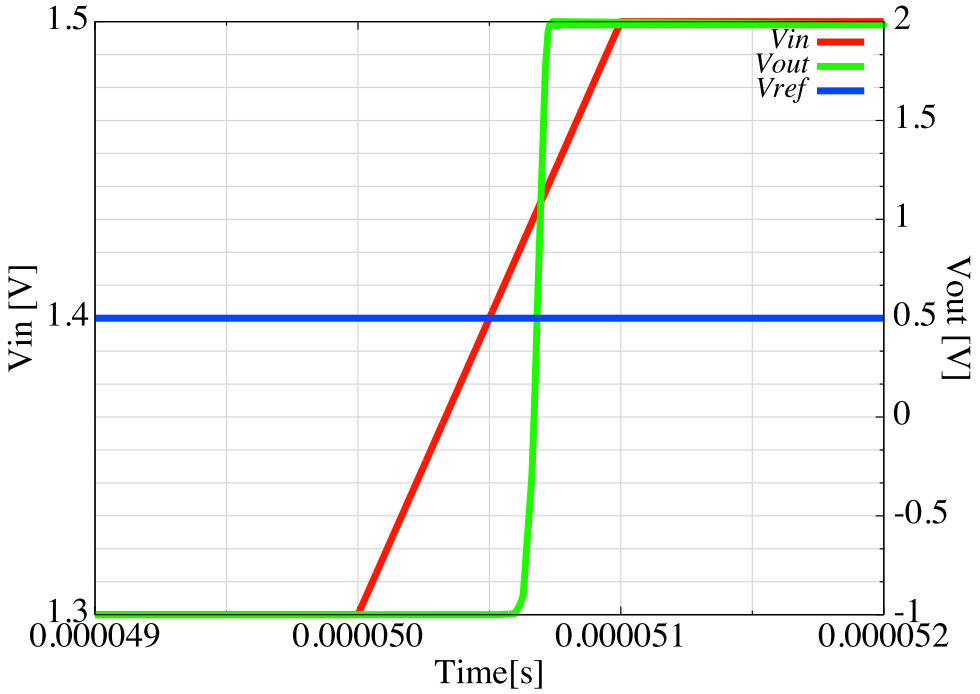
Appendix

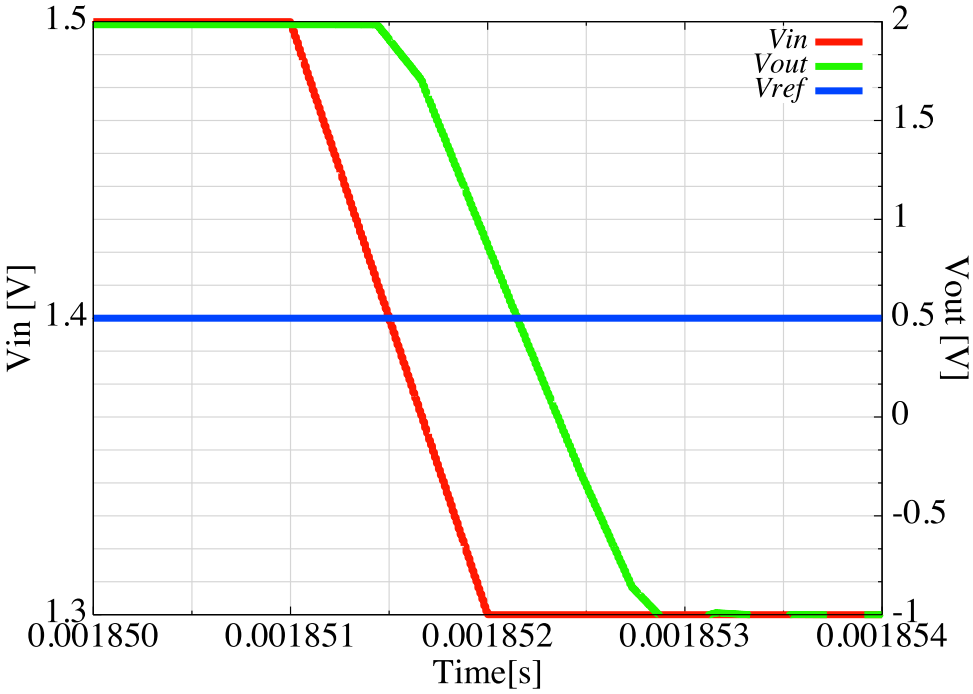
Change Reference Voltage

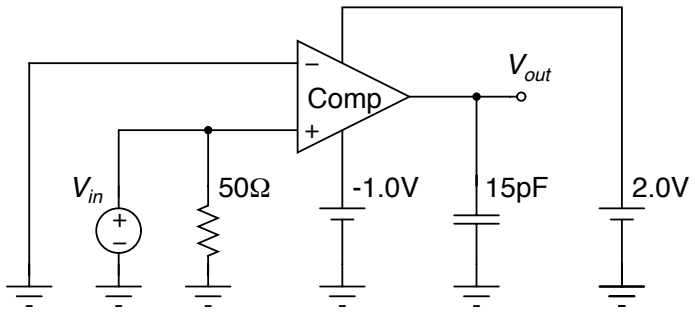
Change Input Pulse

MOSFET's Operating State

Change Reference Voltage





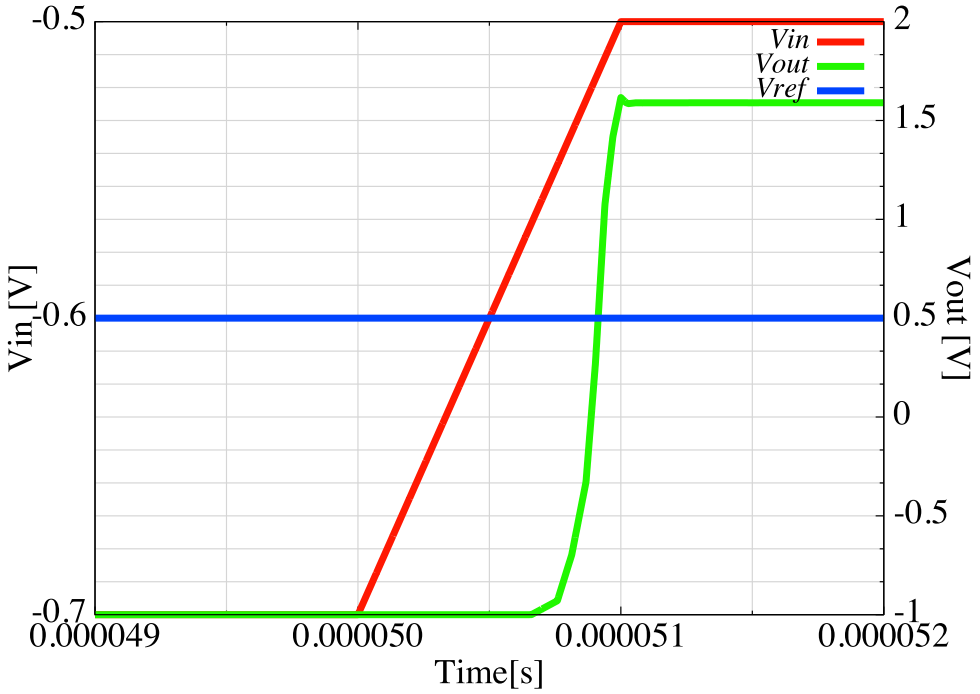


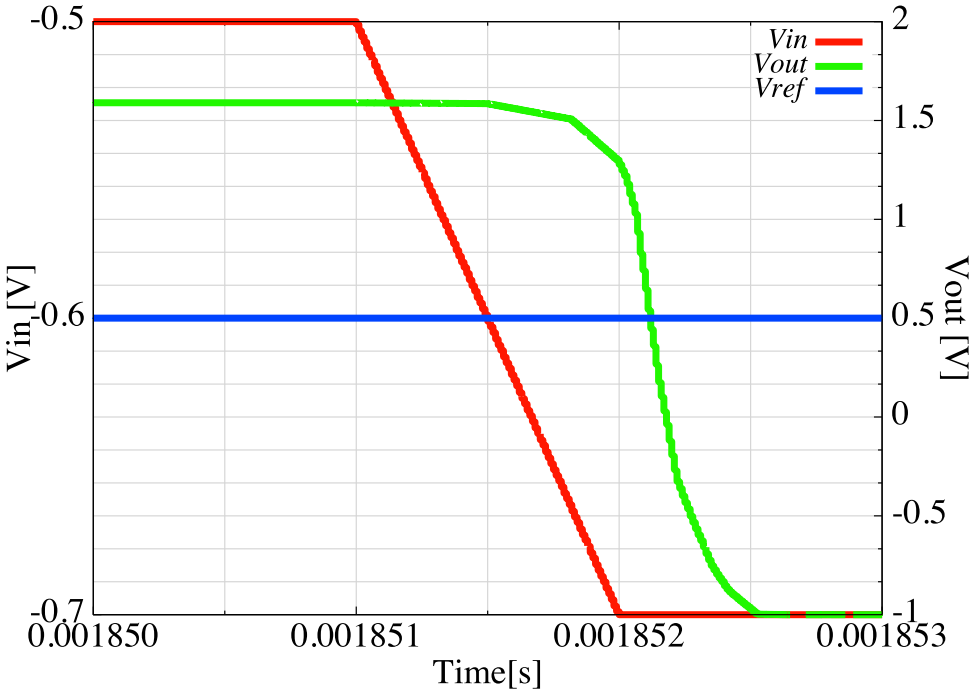
V_{ref} = 1.4V

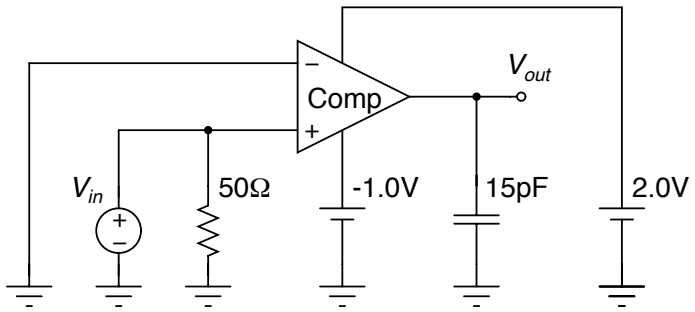
Input Pulse(V_{in})

200mV/μs [1.3V ~ 1.5V]

Change Reference Voltage







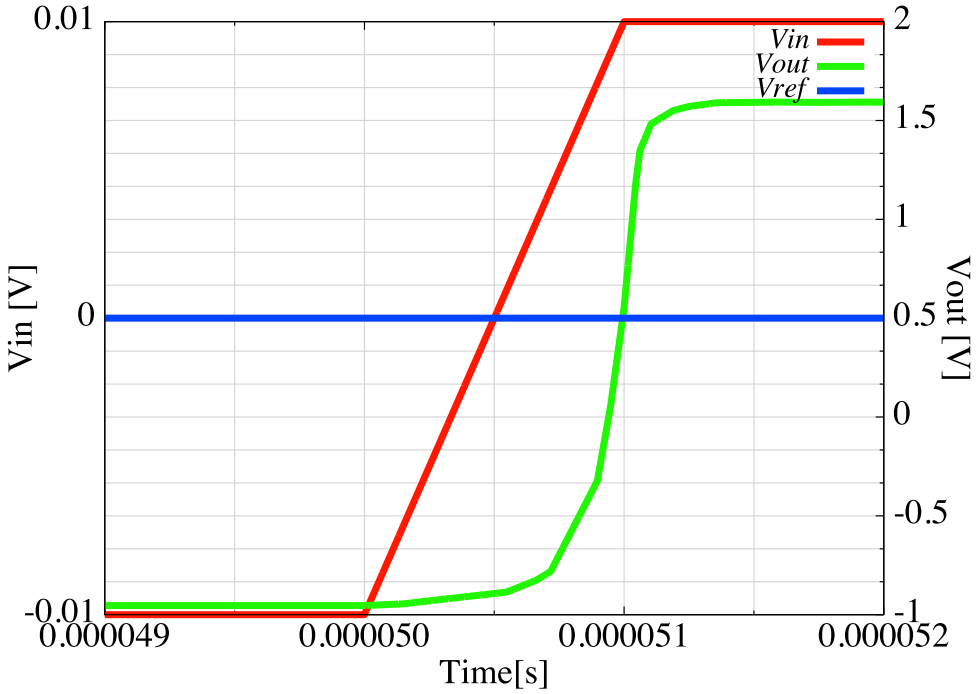
$V_{ref} = -0.6V$

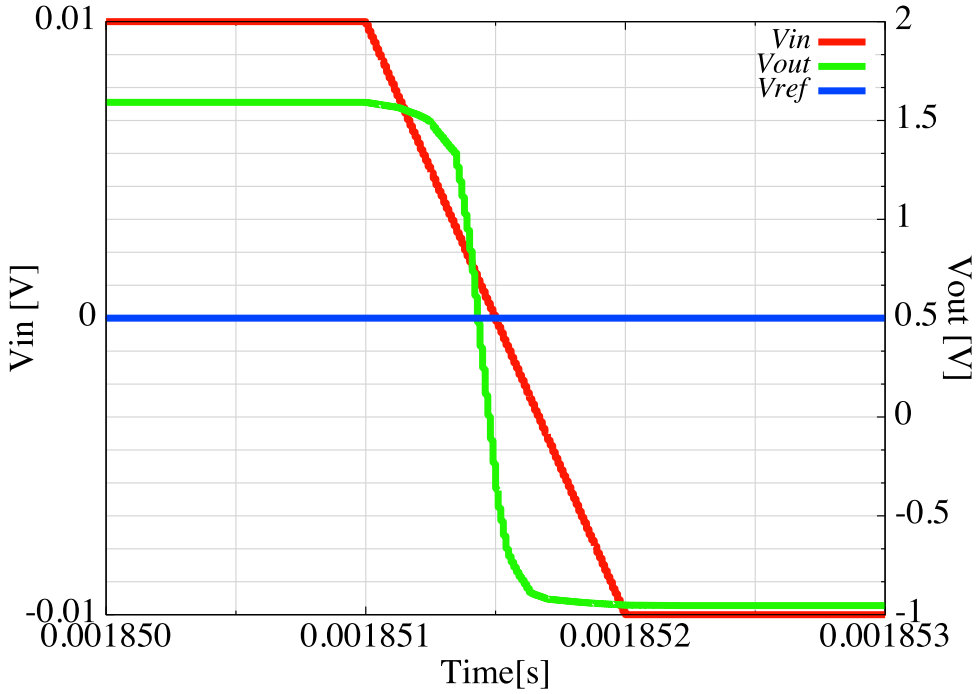
Input Pulse(V_{in})

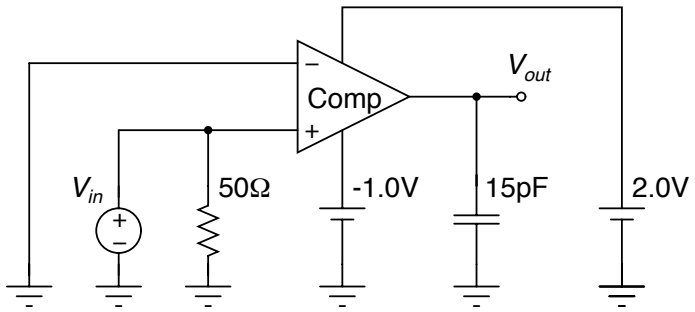
200mV/μs [–0.7V ~ –0.5V]

Operating Range： $-0.6V \leq V_{ref} \leq 1.4V$

Change Input Pulse







Input Pulse(V_{in})

200mV/μs [–0.1V ~ 0.1V]

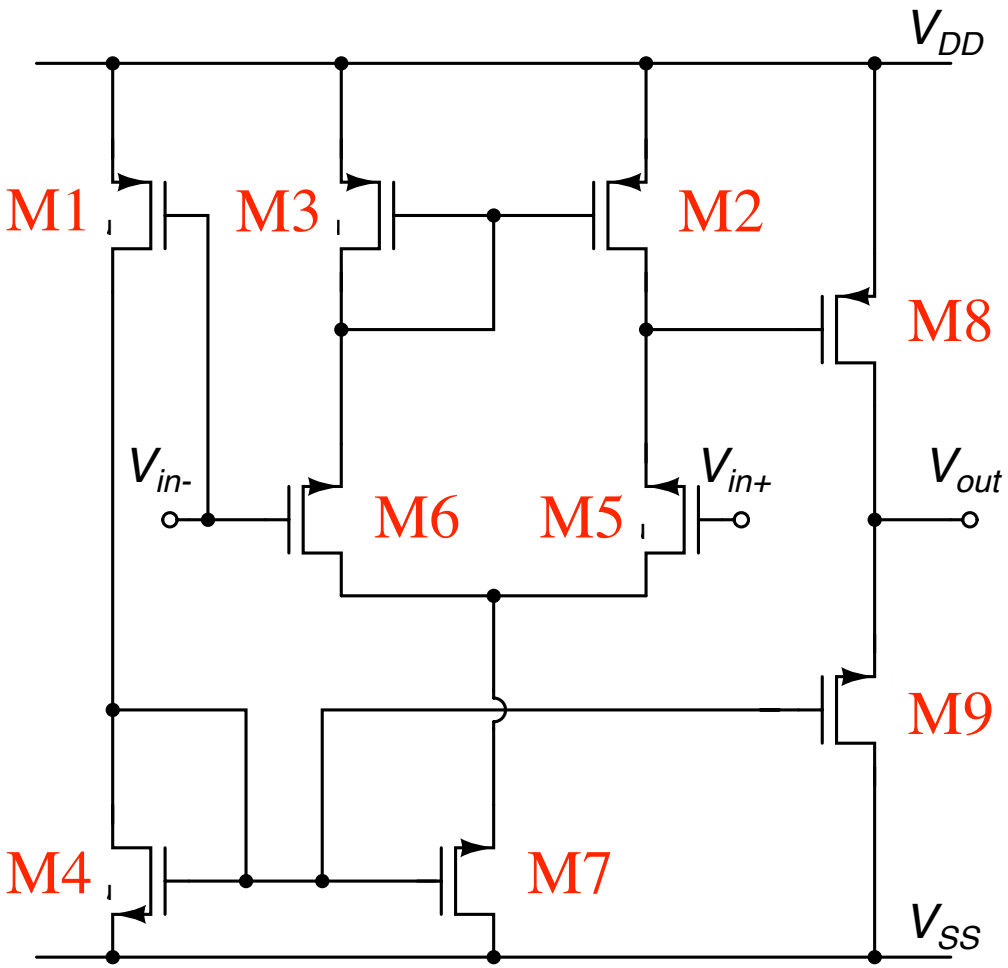
↓

20mV/μs [-0.01V ~ 0.01V]

Operation Check： Overdrive 10mV

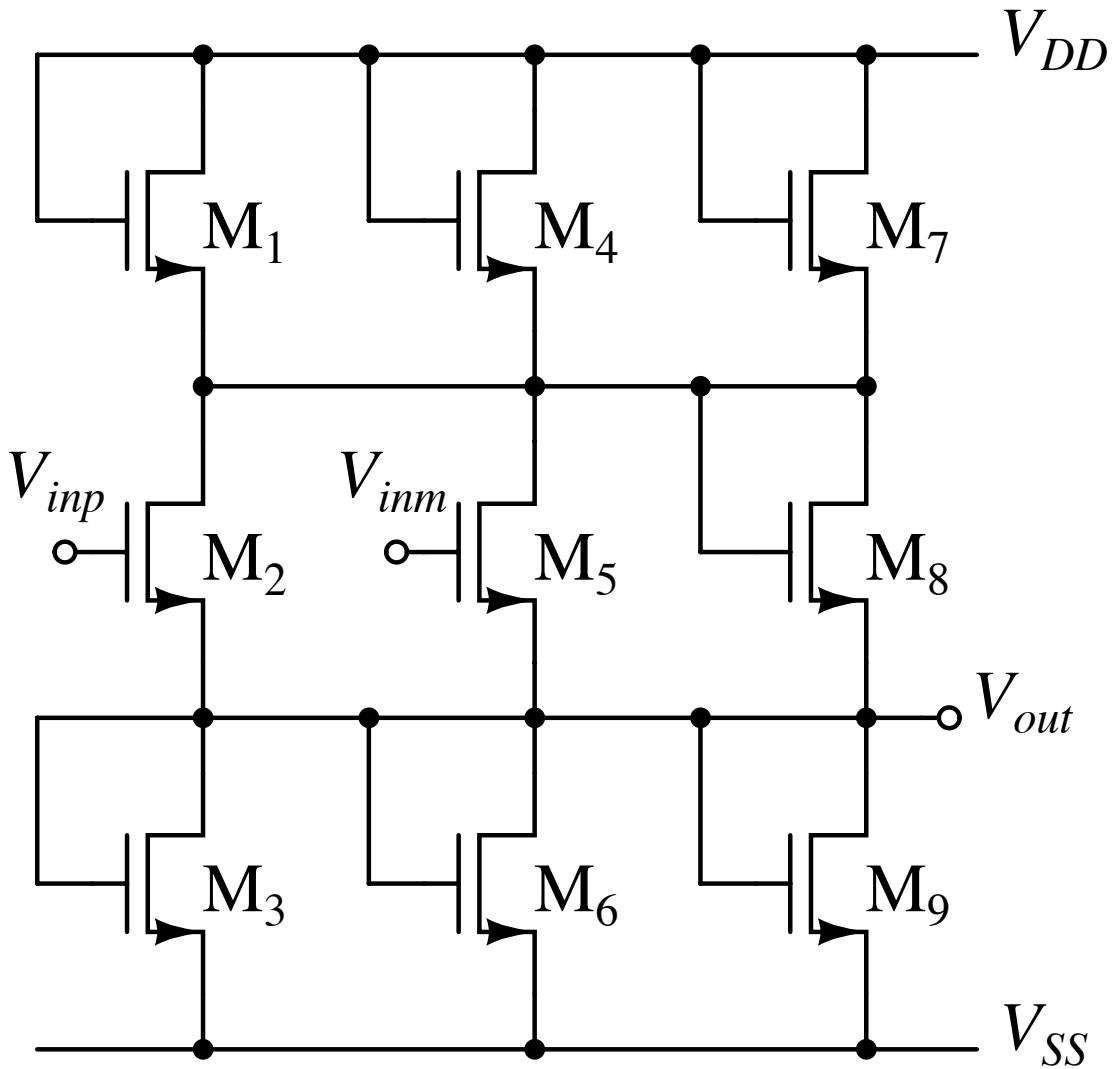
MOSFET's Operating State

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, Mutation) → Selection of The Highest Performance Circuit



MOS	Pulse Low	Pulse High
M1	Linear	Linear
M2	Linear	Saturation
M3	Saturation	Saturation
M4	Saturation	Saturation
M5	Saturation	Linear
M6	Saturation	Saturation
M7	Linear	Linear
M8	Cutoff	Linear
M9	Linear	Saturation

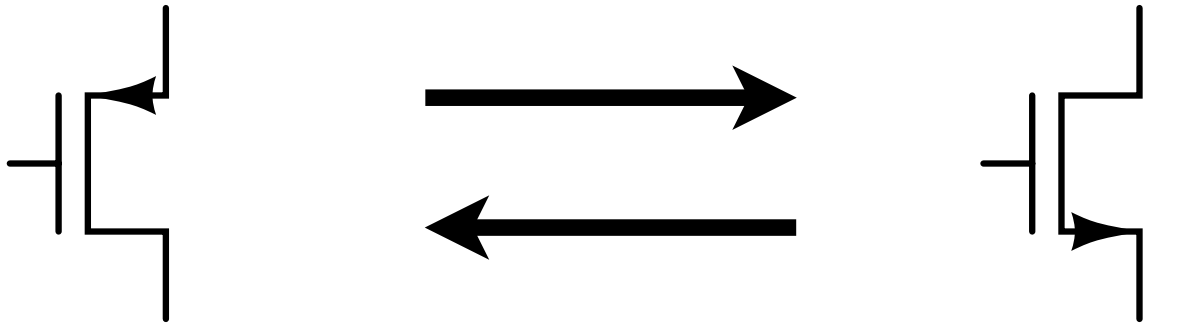
Faulty initial circuit



Mutation - Case 4

STEPs : Create Circuit File → Optimize Circuit Variables→ Calculate Circuit Performance
→ Application of GA (Selection, **Mutation**) → Selection of The Highest Performance Circuit

Change probability is 50%



PMOS **NMOS**