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Design methodology for determining the number of stages in a cascaded time amplifier to minimize area consumption

Kiichi Niitsu[1a)], **Naohiro Harigai**[2], **and Haruo Kobayashi**[2]

[1] *Department of Electrical Engineering and Computer Science, Graduate School of Engineering, Nagoya University, Furo-cho, Chikusa-ku, Nagoya 464–8603, Japan*

[2] *Division of Electronics and Informatics, Faculty of Science and Technology, Gunma University, 1–5–1 Tenjin-cho, Kiryu, Gunma 376–8515, Japan*

a) *niitsu@nuee.nagoya-u.ac.jp*

Abstract: This paper describes a design methodology for determining the number of stages in a cascaded time amplifier to minimize the area consumption. The total area consumption is categorized into three parts, which allows mathematical analysis and optimization to be performed. A combination of the proposed mathematical analysis and 2D mapping can determine the number of stages to minimize the area consumption.

Keywords: time amplifier, CMOS, integrated circuits, design methodology, design for testability

Classification: Integrated circuits

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1 Introduction

CMOS device scaling has been improving the available time resolution, which raises the possibility of developing better time-resolved circuits. In a time-resolved circuit design, one of the most important components is the time amplifier (TA).

The principle of a TA was proposed in 2003 [1]. Since then, many tech-

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niques for the design of TAs have been reported, such as a cascaded architecture [2] and a closed-loop architecture [3].

The cascaded architecture is expected to be used for high-gain time amplification. For example, the cascaded architecture has already been adopted for high-resolution on-chip jitter measurement in order to obtain high-gain characteristics [4]. Although TAs consists of only several gates and require small area occupation in usual situation, high-gain TAs require considerable footprint, which is fatal for cost-severe on-chip BIST application. For example, the previous design [4] result in 176% additional area overhead (from 490 μm^2 to 1350 μm^2) due to high-gain TA implementation. However, there has been no report on a design methodology for the determining the optimal number of stages in a cascaded TA. This paper introduces design guidelines for optimizing the design of a cascaded TA from a mathematical background.

2 Design of each stage's gain in cascaded TA

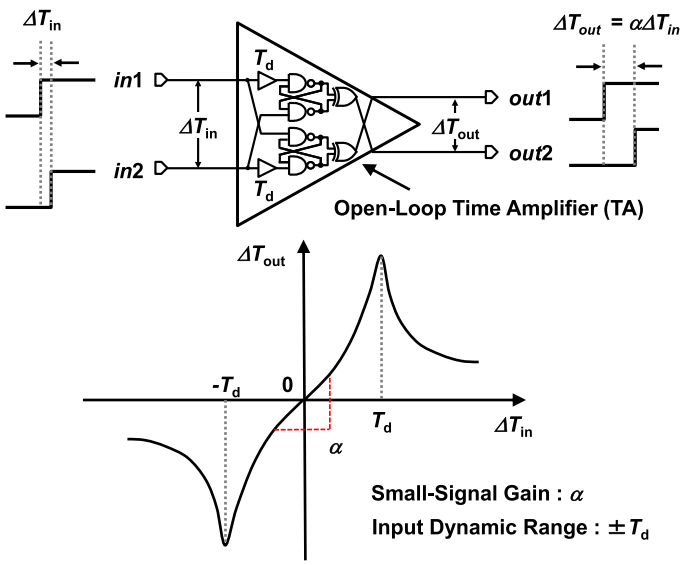

Fig. 1. Schematic of the open-loop time amplifier (TA) [1].

Figure 1 shows a schematic of an open-loop TA [1]. The circuit is composed of delay cells, NAND-SR latches, and XOR gates. The small-signal gain, α, can be expressed by the following equation:

$$\alpha = \frac{2C}{g_m \cdot T_d} \tag{1}$$

Here, g_m is the transconductance of the metastable NAND gate, C is the output capacitance of the NAND gate, and T_d is the delay of the delay cell. For constant transistor sizes for the NAND and XOR gates, the gain and input dynamic range can be changed by adjusting C and T_d.

Figure 2 shows a schematic of a two-stage TA. The gains of each TA are

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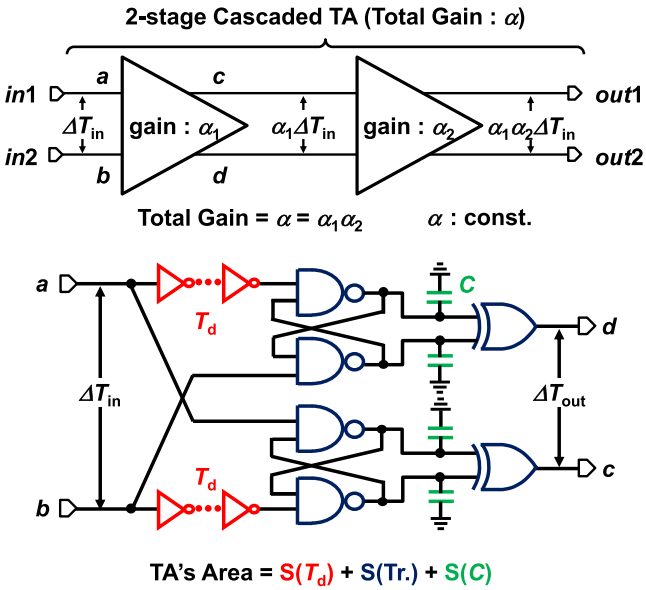

Fig. 2. Schematic of 2-stage cascaded TA.

as follows:

$$\alpha = \alpha_1 \cdot \alpha_2, \quad \alpha : const. \tag{2}$$

$$\alpha_1 = \frac{2C_1}{g_m \cdot T_d} \tag{3}$$

$$\alpha_2 = \frac{2C_2}{g_m \cdot T_d} = \frac{\alpha}{\alpha_1} \tag{4}$$

The area consumption of a TA can be mainly categorized into that of the delay cell, $S(T_d)$; that of the NAND and XOR gates, $S(Tr)$; and that of the output capacitor, $S(C)$. $S(T_d)$ is determined by the required input dynamic range and is constant for all stages. Meanwhile, $S(Tr)$ is determined by the implementation process, and $S(C)$ is determined by the gain.

Under the above conditions, the total area occupied by a two-stage cascaded TA can be expressed as

$$\begin{aligned} S_{2stage} &= S\left(T_{d1}\right) + S\left(T_{r1}\right) + S\left(C_1\right) \\ &\quad + S\left(T_{d2}\right) + S\left(T_{r2}\right) + S\left(C_2\right) \end{aligned} \tag{5}$$

$$S\left(T_{d1}\right), S\left(T_{d2}\right), S\left(T_{r1}\right), S\left(T_{r2}\right) : const.$$

$$S\left(C_1\right) \propto \alpha_1, S\left(C_2\right) \propto \alpha_2$$

$$S_{2stage} = a\left(\alpha_1 + \alpha_2\right) + b = a\left(\alpha_1 + \frac{\alpha}{\alpha_1}\right) + b,$$

$$a, b : const. \tag{6}$$

The design consideration for minimizing the total area can be written as

$$\frac{\partial S_{2stage}}{\partial \alpha_1} = \left(1 - \frac{\alpha}{\alpha_1^2}\right) S\left(C\right) = 0$$

$$\therefore 1 - \frac{\alpha}{\alpha_1^2} = 0 \quad \rightarrow \quad \alpha = \alpha_1^2 \quad \rightarrow \quad \alpha_1 = \alpha_2 \tag{7}$$

The above expression suggests that the gains should be constant for each stage in the TA in order to minimize the area consumption. This gain design methodology can also be applied to cases with more than three stages.

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3 Design methodology for determining the number of stages in a cascaded TA

The occupied area of the TA, S, can be expressed as

$$\begin{aligned} S &= S(T_r) + S(T_d) + S(C) \\ S(T_d) &= a_p \cdot T_d \cdot S(T_r) \\ S(C) &= a_p \cdot b_p \cdot T_d \cdot S(T_r) \end{aligned} \tag{8}$$

Here, a_p is an index term for implementation process and b_p is an index term for the area efficiency for implementing the capacitor for the output of the NAND gate. Since the delay lines are consisted by the transistors, the area occupation of the delay lines can be expressed by the multiplication of that of the NAND and XOR gates.

A schematic of an n-stage TA is shown in Fig. 3. As stated in the previous section, each stage's gain is designed to be $\sqrt[n]{\alpha}$, where the total gain is α. Since the input time differences of the latter-stages' TAs are amplified by the former-stages' TA, the delay cells of all TAs have to be $\sqrt[n]{\alpha^{n-1}}$ times larger than the input time difference, T_d. In other words, the input dynamic range of each-stage TA is $\sqrt[n]{\alpha}$-times smaller than the output time difference, $\alpha T_d = \sqrt[n]{\alpha^n} T_d$. Under this condition, the total area consumption of an n-stage TA, S_n can be expressed as

$$\begin{aligned} S_n &= n\left\{S(T_r) + \sqrt[n]{\alpha^{n-1}} \cdot S(T_d) + \sqrt[n]{\alpha} \cdot S(C)\right\} \\ &= n\left\{1 + \sqrt[n]{\alpha^{n-1}} \cdot a_p \cdot T_d + \sqrt[n]{\alpha} \cdot a_p \cdot b_p \cdot T_d\right\} S(T_r) \end{aligned} \tag{9}$$

The deviation of the total area, S_n can be expressed as

$$\begin{aligned} \frac{\partial S_n}{\partial n} &= n\left\{1 + \sqrt[n]{\alpha^{n-1}} \cdot a_p \cdot T_d + \sqrt[n]{\alpha} \cdot a_p \cdot b_p \cdot T_d\right\} S(T_r) \\ &\quad + \left\{\sqrt[n]{\alpha^{n-1}} - \sqrt[n]{\alpha} \cdot b_p\right\} \frac{1}{n} \ln\alpha \cdot a_p \cdot T_d \cdot S(T_r) \\ &= 0 \end{aligned} \tag{10}$$

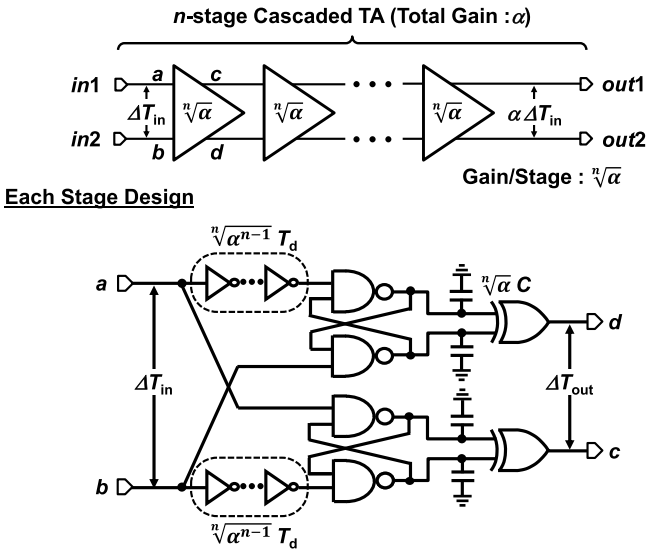

Fig. 3. Schematic of n-stage cascaded TA.

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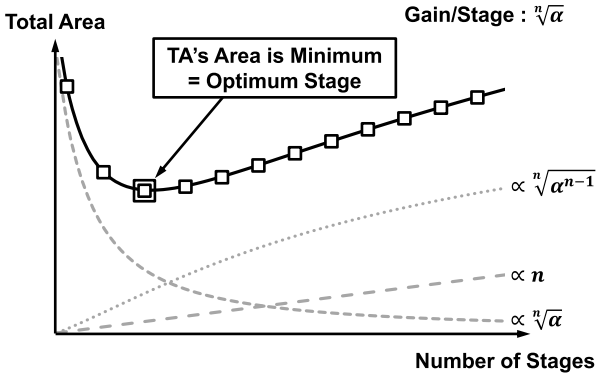

Fig. 4. Conceptual image of the design methodology for determining the optimum number of stages.

A conceptual image of the design methodology for determining the optimum number of stages is depicted in Fig. 4. The total area consumption is proportional to $n\sqrt[n]{\alpha}$, and the number of stages producing the minimum value is thus the optimum number of stages.

4 Optimization of the number of stages in a cascaded TA

This section introduces the design methodology for optimizing the number of stages in a cascaded TA after process porting such as from 90 nm CMOS to 65 nm CMOS and modification of the specification.

4.1 Design optimization at process porting

In process porting, a_p and b_p change while the design specification (the input dynamic range and total gain) is assumed to be constant. From (10), this optimum point can be derived as

$$b_p = \frac{1 + \sqrt[n]{\alpha^{n-1}} \cdot a_p \cdot T_d \left(1 + \frac{1}{n}\ln\alpha\right)}{\sqrt[n]{\alpha} \cdot a_p \cdot T_d \left(\frac{1}{n}\ln\alpha - 1\right)} \tag{11}$$

From (11), a 2D mapping of the design optimization after process porting can be depicted as shown in Fig. 5. In this graph, the gain and input dynamic range are fixed at 100 and 10 ps, respectively. Finally, the number of stages can be optimized analytically by referring to 2D mappings such as that in Fig. 5.

4.2 Design optimization for modification of the specification

When the specification is modified, the total gain α and the input dynamic range T_d change while a_p and b_p are assumed to be constant. From (10), this optimum point can be derived as

$$T_d = \frac{1}{\left\{\left(\frac{1}{n}\ln\alpha - 1\right)\sqrt[n]{\alpha} \cdot b_p - \left(\frac{1}{n}\ln\alpha + 1\right)\sqrt[n]{\alpha^{n-1}}\right\} a_p} \tag{12}$$

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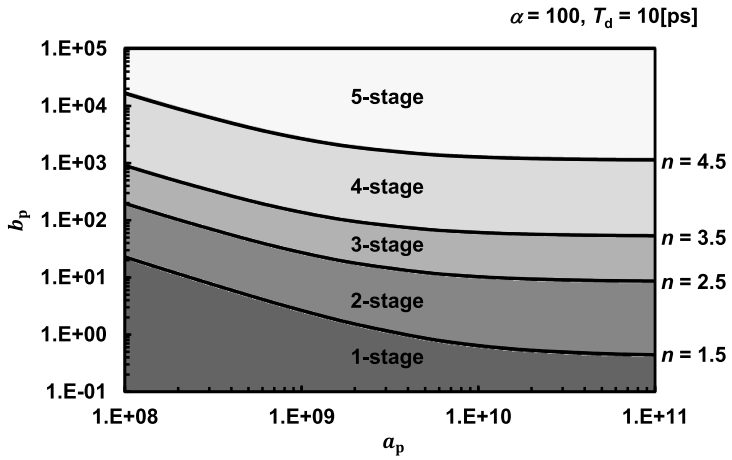

Fig. 5. Design optimization for process porting.

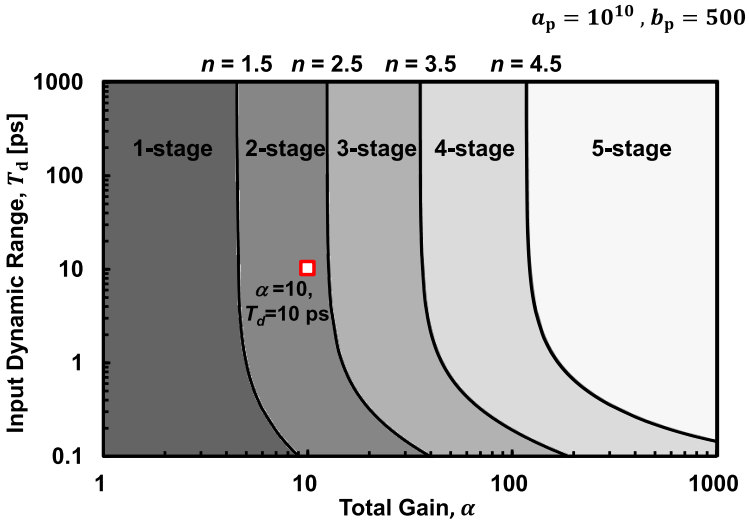

Fig. 6. Design optimization for modification of the specification.

From (12), a 2D mapping of design optimization at modification of the specification can be depicted as shown in Fig. 6. In this graph, a_p and b_p are fixed at 10^{10} and 500, respectively. These indexes are approximately determined by referring the state-of-the-art process of 65-nm CMOS technology. Finally, the number of stages after modification of the specification can be optimized analytically by referring the 2D mapping such as Fig. 6.

The application of Fig. 6 is as follows. For example, when the input dynamic range and gain are 10 ps and 10, respectively, the point marked by red square is referred. The point is included in the area where the optimum number of stages is two. This means that the optimum number of stages is two for area minimization. By process the above steps, we can minimize the area consumption of the cascaded open-loop time amplifier.

4.3 Verification of the effectiveness of the proposed optimization

This subsection shows the verification of the effectiveness of the proposed design optimization. For verifying the effectiveness, we have implemented

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the time amplifiers with typical specifications for on-chip jitter measurement application.

Figure 7 shows the occupied area dependence on the number of stages. The characteristic curve indicates that there is an optimum point in the number of stages and the optimum number of stages is two as expected in the previous sub-section.

4.4 Discussion

The combination of subsections 4.1 and 4.2 forms a feasible design methodology for minimizing the area. This section introduces a simplified approach to estimate the optimum number of stages in specific situations.

Assuming that the total gain, α is sufficiently large, the area of the output capacitances of the NAND gates, $S(C)$ is dominant. Under this assumption, the optimum number of stages can be determined theoretically using simple mathematical analysis.

$$S_n \approx n \cdot \sqrt[n]{\alpha} \cdot a_p \cdot b_p \cdot T_d \cdot S\left(T_r\right) \tag{13}$$

$$\begin{aligned} \frac{\partial S_n}{\partial n} &= \left\{ \sqrt[n]{\alpha} + n \cdot \sqrt[n]{\alpha} \cdot \ln \alpha \cdot \left(-\frac{1}{n^2}\right) \right\} \\ &\quad \cdot a_p \cdot b_p \cdot T_d \cdot S\left(T_r\right) = 0 \\ \therefore \left\{ \sqrt[n]{\alpha} - \frac{1}{n} \cdot \sqrt[n]{\alpha} \cdot \ln \alpha \right\} = 0 &\quad \rightarrow \quad 1 - \frac{1}{n} \ln \alpha = 0 \\ &\quad \rightarrow \quad n = \ln \alpha \end{aligned} \tag{14}$$

Therefore, the optimum number of stages can be determined from only the total gain α when the area of the capacitance is dominant. In general, the scaling speed of the capacitance is slower than that of the transistors; therefore, this approximate analysis will be effective for future scaled technologies.

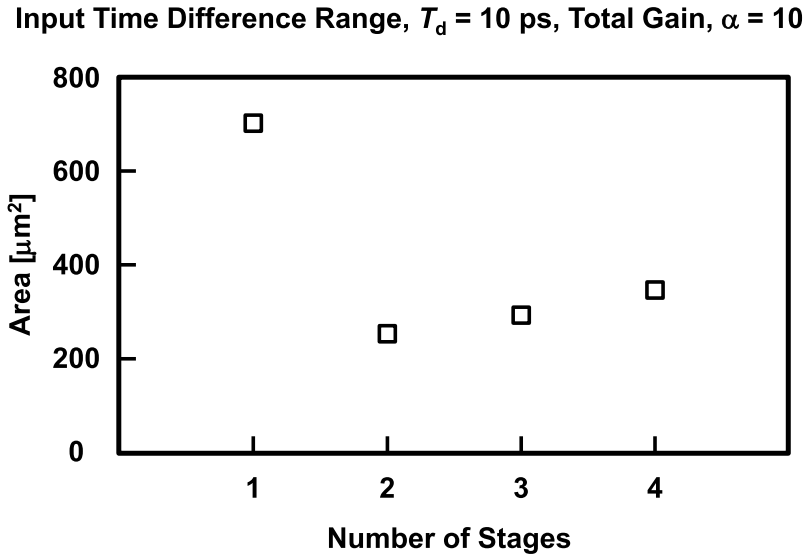

Fig. 7. Occupied area dependence on number of stages.

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5 Conclusion

The design methodology for optimizing the number of stages in a cascaded TA was demonstrated. The total area consumption was categorized into three parts (delay cells, output capacitance, logic gates), which made mathematical analysis and design optimization feasible. Finally a combination of the proposed mathematical analysis combined and 2D mapping yielded the number of stages for minimizing the area consumption.

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