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An Analysis of Stochastic Self-Calibration of TDC Using Two Ring Oscillators

Kentaroh Katoh
Dept. of Electrical Engineering of
Tsuruoka National College of Technology
Tsuruoka, Yamagata 263–8522 Japan
Email: katoh_kentaroh@yahoo.co.jp

Yuta Doi, Satoshi Ito,
Haruo Kobayashi, Ensi Li, and
Nobukazu Takai
Division of Electronics and Informatics,
Gunma University
Kiryu, Gunma 376–8515 Japan
Email: {k_haruo,takai}@el.gunma-u.ac.jp

Osamu Kobayashi
Semiconductor Technology
Academic Research Center (STARC)
Yokohama 222-0033 Japan
Email: kobayashi.osamu@starc.or.jp

***Abstract*—This paper presents a theoretical analysis of the stochastic calibration of TDC using two ring oscillators. Designers of TDC with the calibration function have to decide the design parameters to guarantee the convergence of error and valid calibration time. The basic theory of the calibration is useful to decide these parameters and the policy on the calibration design. The performance of the stochastic calibration depends on the design parameters, the frequencies of the two ring oscillators, the number of the stages, the buffer delay, and so on. This work analyzes explicitly the relation between these parameters and the performance of the calibration with simulation-based analysis. Simulation results reveal that the convergence of the calibration is guaranteed when both of the cycles of the two ring oscillators are the prime cycles. The histogram of each bin converges to the corresponding buffer delay value in a well-behaved manner; the *DNL* measurement error decreases monotonically in proportion to the increase of the number of the times of the measurement. In other words, the required number of the measurement times is in proportion to the required accuracy of calibration. This result is applied to the calibration of VDL-based TDC, too.**

I. Introduction

A Time-to-Digital-Converter (TDC) measures the time interval between two edges, and time resolution of several picoseconds can be achieved when the TDC is implemented with an advanced CMOS process. TDC applications include phase comparators of all-digital PLLs, sensor interface circuits, modulation circuits, demodulation circuits, as well as TDC-based ADCs [1], [2], [3], [4], [5], [6], [7], [8], [9]. The TDC will play an increasingly important role in the nano-CMOS era, because it is well suited to implementation with fine digital CMOS processes; a TDC consists mostly of digital circuitry, and resolution improves as switching speed increases.

Although the resolution of TDC is high, the linearity of TDC is lower. Therefore, self-calibration technique for high linearity is required. Ito et al. proposed the stochastic self-calibration technique of TDC using two ring oscillators [10]. Because this calibration technique is fully digital, it can be easily implemented on SOC fabricated with nanometer technology. Because this technique requires two ring oscillators unlike the method from [11], [12], the cost is lower.

This paper analyzes the stochastic calibration of TDC using two ring oscillators theoretically. Designers of TDC with the calibration function have to decide design parameters to guarantee the convergence of error and valid calibration time. The basic theory of the calibration is useful to decide these parameters and the policy on the calibration design. The convergence of the stochastic calibration depends on the uniformity of the differential delay sequence. The uniformity of the differential delay sequence depends on the design parameters, the frequencies of the two ring oscillators, the number of the stages, the buffer delay and so on. This work analyzes explicitly the relation between these parameters and the performance of the calibration with simulation-based analysis.

The rest of the paper is organized as follows. Section II describes the preliminaries for the following explanation. Section III explains the stochastic calibration using two ring oscillators. Section IV shows the simulation results. Finally, section V concludes the paper.

II. Preliminaries

In this work, we assume the basic TDC. Figure 1 (a) shows an example of the architecture of the basic TDC with four stages. The TDC is composed of four positive edge triggered D-type flip flops and an upper delay line and a lower clock line. The delay line is inserted four buffers with uniform delay. Each stage of a TDC is composed of a flip flop and a buffer. Suppose the two input signals are START and STOP. The START is the input of the upper delay line. The STOP is the input of the clock line. The delay of the buffer of each stage is τ. The TDC measures the time interval between a transition from START and a transition from STOP. The resolution is equal to delay of a buffer.

In case of vernier delay line (VDL), buffers are inserted to the clock line, too. Each stage of VDL is composed of a flip flop, an upper buffer, and a lower buffer [13]. When delay of an upper buffer is τ_1 and the delay of a lower buffer is τ_2, the resolution Δ is equal to $\tau_1 - \tau_2$. The function of

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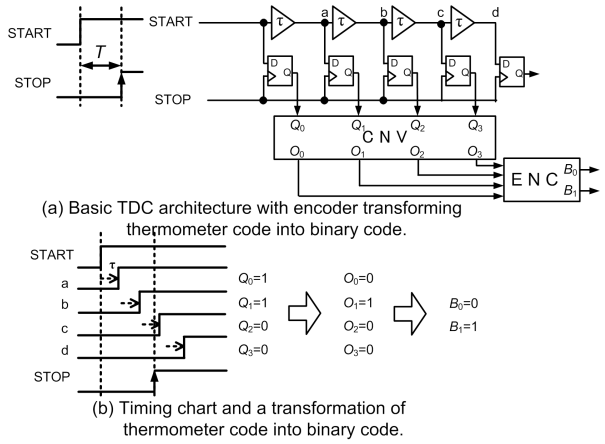

Figure 1. Basic 2-bit TDC.

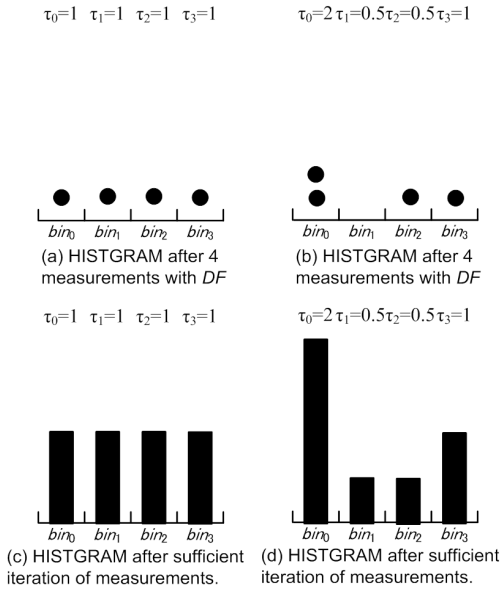

Figure 2. Basics.

VDL is equivalent to that of the basic TDC with the buffers with the delay Δ.

Figure 1 (b) shows the timing chart of the basic TDC when the time interval between a transition signal from START and a transition signal from STOP is 2. After the measurement, the converter CNV transforms the result of the thermometer code $Q_0Q_1Q_2Q_3 = 1100$ into the corresponding SW code $O_0O_1O_2O_3 = 0100$. The SW code is transformed into the corresponding binary code $B_0B_1 = 01$ by the encoder ENC.

III. Stochastic Self-Calibration Using Two Ring Oscillators

This section explains the stochastic self-calibration of TDC using two ring oscillators. Subsection III-A describes the basics. Subsection III-B shows the TDC with the stochastic self-calibration function. Subsection III-C explains the calibration sequence. Subsection III-D shows the characteristics of the differential delay sequence generated by the two ring oscillators.

A. Basics

In the stochastic calibration, the differential delays generated by the two ring oscillators are measured consecutively with TDC. The histogram is constructed with the measurement results. The variation of the delay of the buffer of each stage is estimated with the constructed histogram. Figure 2 shows the basics. All the buffers on the delay line of the TDCs of Fig. 2 (a) and (c) have the uniform delay 1. On the other hand, the buffers of the TDCs of Fig. 2 (b) and (d) have varied delay. The delay of the buffers of the first, the second, the third, and the fourth stages are 2, 0.5, 0.5, 1, respectively. Each delay of the differential delay sequence $DF = \{1, 2, 3, 4\}$ is applied to the TDC to measure it sequentially one by one. After each measurement, the bin corresponding to the measurement result is incremented. In case of the ideal TDC, the length of the bins bin_0, bin_1, bin_2, and bin_3 become 1 after the four times measurement (Fig. 2 (a)). On the other hand, in case of the TDC with varied delay, the bin of the first stage bin_0 is incremented after the measurement of the differential delays 1 and 2. The bin of the 3rd stage bin_2 is incremented after the measurement of the differential delay 3. The bin of the 4th stage bin_3 is incremented after the measurement of the differential delay 4. Consequently the length of the bin_0, bin_1, bin_2, and bin_3 are 2,0,1,1, respectively after the four times measurement. As a buffer delay of a stage is larger, the length of the bin of the stage is longer. After sufficient measurement times with the delay sequence following uniform distribution whose lower limit is 0 and upper limit is 4, the length of the bin is proportional to the amount of the delay of the stage. Accordingly the variation of delay of the buffer of each stage can be estimated from the constructed histogram.

B. TDC with Stochastic Self-Calibration Function Using Two Ring Oscillators

Figure 3 shows the 8 stage TDC with stochastic self-calibration function using two ring oscillators. The upper part is TDC, the bottom part is the sub-circuit for the construction of the histogram. The input START is connected to an input of the 2-to-1 multiplexer MUX_0. The output of MUX_0 is connected to the left-side edge of the delay line. The right-side edge of the delay line is feed-back to another input of MUX_0 through an inverter. The delay of the buffer of the ith stage $(0 \leq i \leq 7)$ is τ_i, and the delay of the inverter is τ_u.

The input STOP is connected to an input of the 2-to-1

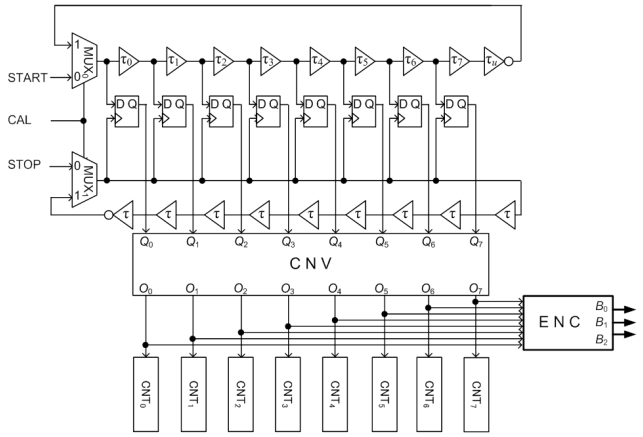

Figure 3. 3-bit TDC with stochastic self-calibration function using two ring oscillators.

multiplexer MUX_1. The output of MUX_1 is connected to the left-side edge of the clock line. The right-side edge of the clock line is feed-back to another input of MUX_1 through eight buffers and an inverter. The delay of the buffers is τ, and the delay of the inverter is τ_b. The input CAL controls the MUX_0 and MUX_1. When CAL = 1, the upper delay line and the lower clock line are configured to the ring oscillators for the calibration. The outputs of the flip flops are connected to the corresponding inputs of CNV $Q_0 - Q_7$. The outputs of CNV $O_0 - O_7$ are connected to the inputs of ENC and the inputs of the counters CNT_i $(0 \leq i \leq 7)$ which count the number of the value 1 to construct the histogram.

C. Calibration Sequence

In the stochastic calibration, the set of the differential delay generated by the two ring oscillators is measured consecutively with TDC. From the measurement result, the histogram is constructed to estimate the variation of the buffers on the delay line of the TDC. The calibration sequence is as follows.

Step 1 Set CAL to 0. Initialize counter values to 0.

Step 2 Set CAL to 1. Initialize $i \leftarrow 1$. Then the calibration starts.

Step 3 Execute ith measurement.

Step 4 When i is equal to the number of the iteration of the delay measurements N_{MEAS}, finish. Otherwise increment i and go to Step 3.

D. Characteristics of the differential delay sequence

The characteristics of the differential delay sequence depends on the cycle of the upper ring oscillator T_0, the one of the lower ring oscillator T_1, and the initial differential delay d when the calibration starts. Figures 4-6 show some differential delay sequences. As shown in Fig. 4 and Fig. 5, the difference of T_0 and T_1 gives the difference of the differential delay sequence. As shown in Fig. 6 the differential delay sequence has only two values, 5 and 10 when $T_0 = 10$ and $T_1 = 5$. The cycle T_0 is the multiple of T_1. In other word, the frequency of the upper ring oscillator is a sub-harmonic frequency of that of the lower ring oscillator. This phenomenon is quite similar to the bunching effect of the random repetitive sampling mode of digital oscilloscope [14]. The difference of the parameters influences on the calibration time and the convergence of the calibration.

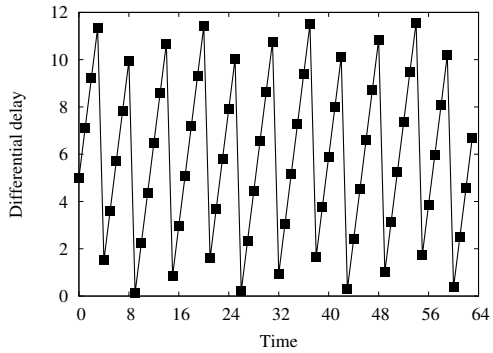

Figure 4. Differential delay sequence ($N_{STG} = 8, T_0 = 11.93, T_1 = 2.11, d = 5$).

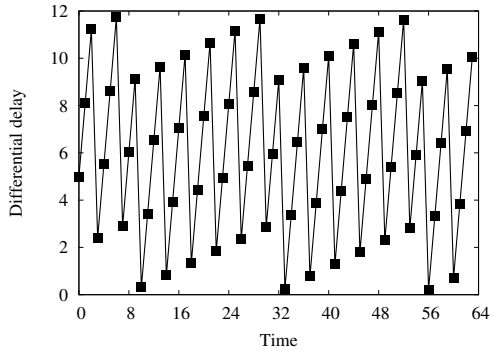

Figure 5. Differential delay sequence ($N_{STG} = 8, T_0 = 11.93, T_1 = 3.11, d = 5$).

IV. Simulation Results

This section verifies the stochastic self-calibration using two ring oscillators with the simulator implemented with C language quantitatively.

Subsection IV-A explains the simulation setup. The characteristics of the calibration depend on the cycle of the upper ring oscillator and the cycle of the lower ring oscillator. Subsection IV-B evaluates the oscillation cycle specification. The characteristics of the calibration depend on the initial differential delay, too. Subsection IV-C evaluates the initial differential delay specification. The

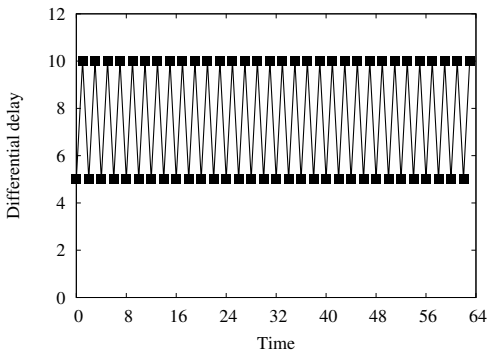

Figure 6. Differential delay sequence ($N_{STG} = 8, T_0 = 10, T_1 = 5, d = 5$).

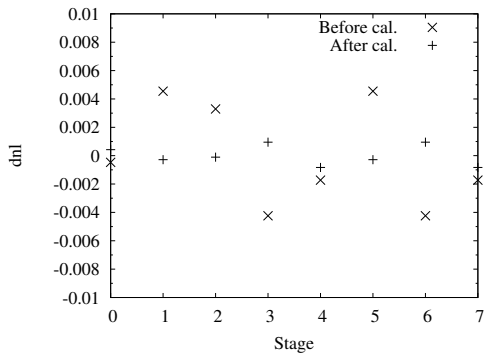

Figure 7. *dnl* error distribution of an 3-bit TDC before calibration and after calibration (T_0=11.93, T_1 = 2.11, d=0, N_E=699).

proposed calibration requires the dedicated counters for the construction of the histogram. The extra area depends on the bit length. In Subsection IV-D, we estimate the bit length of the counters.

A. Simulation Setup

In this evaluation, we assume that the ideal delay of a buffer on the delay line is 1. We add variations following gaussian distribution to the buffers. The 3σ of the distribution is 10%. The number of the stage N_{STG} is 8, 16, 32, 64, 128. The differential non-linearity error is defined. When b_{ij} is the length of the bin of the ith stage after j times measurement, the differential non-linearity error of stage i $(1 \leq i \leq N_{MEAS} - 1)$ after j times measurement dnl_{ij} is expressed as the following formula.

$$dnl_{ij} = \frac{\tau_i}{\sum_{i=1}^{N_{STG}-2} \tau_i} - \frac{b_{ij}}{\sum_{i=1}^{N_{STG}-2} b_{ij}} \quad (1)$$

The differential non-linearity error after jth measurement DNL_j is expressed as the following formula.

$$DNL_j = max(|dnl_{1j}|, \cdots, |dnl_{(N_{MEAS}-2)j}|) \quad (2)$$

In the equations (1) and (2), the first and the last stages are ignored because the length of the histogram of these stages can be illegal value. As calibration process proceeds, DNL_j is convergent within the target error *DNL*. When $DNL_{N_{MEAS}-1} > DNL$, the calibration is fail, otherwise the calibration is success. When multiple calibrations are performed, the convergent probability to a target error *DNL* is defined as follows.

$$P_E(DNL) = N_{SCAL}/N_{CAL} \times 100.0$$

, where $P_E(DNL)$ is the convergent probability, N_{CAL} is the calibration times, and N_{SCAL} is the times that the calibration is succeeded. Let $N_E(TDC, T_0, T_1, d, DNL)$ be the required measurement times where *TDC* is the target TDC, the T_0 and T_1 are the cycles of the upper and the lower ring oscillators respectively, d is the initial differential delay, and *DNL* is the target error. When the calibration is fail, $N_E(TDC, T_0, T_1, d, DNL) = 0$. The $N_E(TDC, T_0, T_1, d, DNL)$ is obtained with the following routine.

Step 1 Initialize $i \leftarrow 1$.
Step 2 Execute ith measurement.
Step 3 Calculate DNL_i.
Step 4 If $e > DNL_i$, the value of N_E is i. If i is equal to N_{MEAS}, the value of N_E is 0. Otherwise, increment i and go to Step 2.

The *dnl* error distribution of a 3-bit TDC before calibration and after calibration is shown in Fig. 7.

The set of the prime cycle T_{Pni} of which integer part is i is defined as follows.

$$T_{Pni} = \{d | d = p/10^n, 10^n \times i < p < 10^n(i+1), p \in P, n \in N\}$$

, where P is the set of prime numbers and n is the decimal digit. The inverse of the prime cycle is defined as the prime frequency. In this evaluation, n is set to 2. The influence of RMS jitter is ignored for theoretical analysis.

B. Specification of Cycle of Lower Ring Oscillator

We evaluate the T_1 specification on the following cases of the combination of the cycles of the upper and the lower ring oscillators.

$Case1$ Both of T_0 and T_1 are prime cycles.
$Case2$ T_0 is multiple of T_1.
$Case3$ Arbitrary values of T_0 and T_1.

The maximum value of the differential delay generated by the two ring oscillators is equal to the width of T_0. Therefore, T_0 is fixed. The T_1 is swept up in a range. Let TS_1 be the set of the cycles of the lower ring oscillator. To generate the differential delay sequence following uniform distribution, T_0 should be larger than the largest measureable delay $1.1 \times N_{STG}$. We decide the fixed value of T_0 and TS_1

which is the set of T_1 for the calibration on the above three cases as follows.

$Case1 T_0 = T_{p0}$. The TS_1 includes all the prime cycles in the range between T_{min} and T_{max}.

$Case2 T_0 = T_{max}$. The TS_1 includes all the dividers in the range between T_{min} and T_{max}.

$Case3 T_0 = T_{max}$. The TS_1 includes all the cycles in the range between T_{min} and T_{max}.

The T_{min} and T_{max} are the upper and the lower limits of the range, respectively. The cycle T_{p0} is the maximum prime cycle in the range.

Table I shows the parameter setup of this evaluation. 100 multiple TDCs ($TDC_0 - TDC_{99}$) are generated randomly. With all the combination of T_0 and T_1 picked up from TS_1 the calibration is performed to calculate the convergent probability on $Case1$, $Case2$, $Case3$ in each TDC. The target error *DNL* is 1/1,024. The initial differential delay d is 0.

Table II shows the result. All the convergent probability of $Case1$ is 100 %. All the convergent probability of $Case2$ is 0 %. The convergent probability is 100 % when both of T_0 and T_1 are the prime cycles, while the convergent probability is 0 % when T_0 is a multiple of T_1. In $Case3$, the convergent probability increases as T_{STG} increases. It means that the convergent probability is better as the number of stages is larger when T_1 is an element picked up from TS_1. When T_{STG} =128, $P_{E(1/1024)}$ is 77.7 %. It means that the probability of the convergence of the calibration is 77.7 % when $T_0 = 132$, and a lower cycle T_1 is randomly chosen from TS_1. We conclude that 100 % convergence is guaranteed when both of T_0 and T_1 are the prime cycles, otherwise is not guaranteed.

Next we evaluate the specification of the required number of times of measurement for the convergence to the target error. In this evaluation, $TS_1 = \{T_{10}, T_{11}, \cdot \cdot \cdot, T_{1(N_{TDC}-1)}\}$. When the combination of the cycles is a pair of T_0 and $T_{1i} (0 \leq i \leq N_{TDC}-1)$, the required measurement N_{Ei} is expressed as the following formula.

$$N_{Ei} = \begin{cases} \sum_{j=0}^{N_{TDC}} N_E(T_0, T_{1j}, TDC_i, d, e)/N_{SCAL} \\ (N_{SCAL} \neq 0), \\ 0 \quad (N_{SCAL} = 0) \end{cases}$$

, where N_{SCAL} is the number of TDCs that calibrations are convergent. The average number of the times of the delay measurement N_{Eave} is expressed as the following formula.

$$N_{Eave} = \begin{cases} \sum_{i=0}^{N_{TDC}} N_{Ei}/N_{STDC} \quad (N_{STDC} \neq 0), \\ 0 \ (N_{STDC} = 0) \end{cases}$$

, where N_{STDC} is the sum of TDC that $N_{Ei} \neq 0$. The target error *DNL* is 1/128, 1/256, 1/512, 1/1,024. The initial differential delay d is 0. Figure 8 represents the *DNL*-N_{Eave} specification in case of $Case1$. The horizontal axis is *DNL*. The vertical axis is N_{Eave}. This graph demonstrates that approximately N_{Eave} increases in proportion to the decrease of *DNL*. As N_{STG} increases, the curves move up to the vertical direction.

Figure 9 shows the $DNL - N_E$ specification. The T_0 is fixed to 12.0. Four T_1s are randomly chosen from TS_1. Then the four curves a, b, c, d are plotted. The number of the maximum delay measurement times N_{MEAS} is 10,000. Accordingly, if a curve sticks to N_{MEAS}, then the calibration fails on the point. The curve a fails to converge in $DNL = 1/1,024$. The curve b fails to converge in $DNL = 1/256, 1/512, 1/1,024$. The curves c and d succeed to converge in $DNL = 1/128, 1/256, 1/512, 1/1,024$. Like this, the variance of the curves is large when T_0 and T_1 are not prime cycles.

Table I
PARAMETER SETUP OF EVALUATION OF SPECIFICATION OF T_1.

N_{STG}	T_{min}	T_{max}	T_{p0}
8	2	12	11.93
16	2	18	17.89
32	2	36	35.93
64	2	68	67.93
128	2	132	131.87

Table II
CONVERGENT RATIO($d = 0, e = 1/1,024$).

Case	T_{STG}				
	8	16	32	64	128
$Case1$	100.0	100.0	100.0	100.0	100.0
$Case2$	0.0	0.0	0.0	0.0	0.0
$Case3$	37.5	44.0	57.1	75.9	77.7

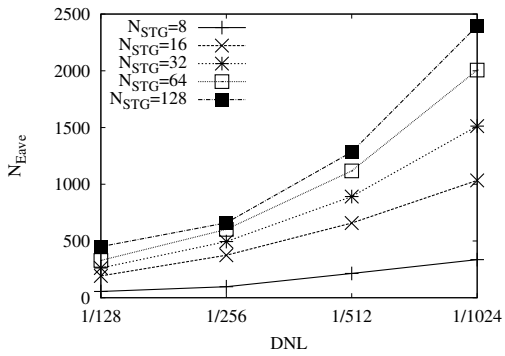

Figure 8. *DNL*-N_{Eave} specification ($Case1$).

C. Specification of Initial Differential Delay

The characteristics of the differential delay sequence depend on the initial differential delay. We evaluate the d specification of the required measurement N_E. With the pair of T_0 and T_1 which guarantees the convergence when

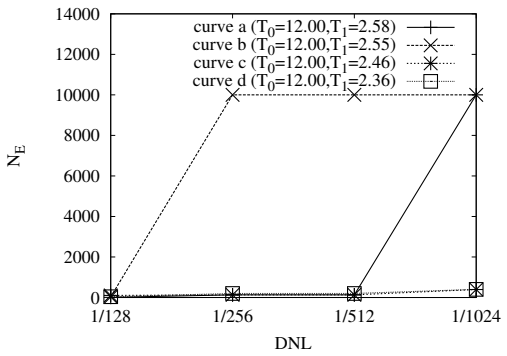

Figure 9. *DNL*-N_E specification ($Case2$).

$d = 0$, we perform the multiple calibrations consecutively with sweeping up d from 0 to T_0. Figure 10 shows the curve of d specification when $T_{STG} = 64$, $T_{p0} = 67.93$, and T_1 is 2.11. The horizontal axis is d. The vertical axis is the required measurement times N_E for the convergence to *DNL* $= 1/128, 1/256, 1/512, 1/1,024$. This result shows that N_E does not depend on d.

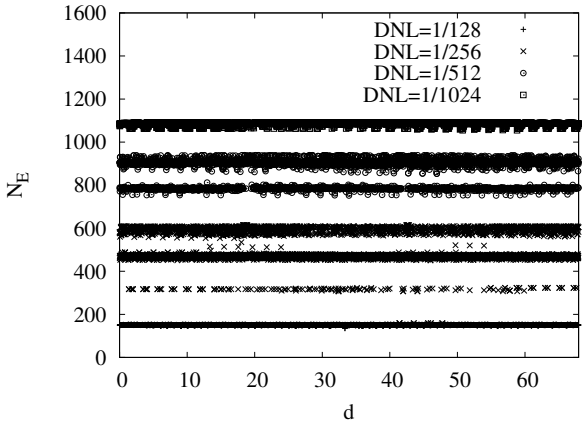

Figure 10. d-N_E specification ($N_{STG} = 64, T_0 = 67.93, T_1 = 2.11$).

D. Bit Length of Counters

When 3σ of the distribution of the buffer delays is 0.1, the required bit length of the counter of each stage L_{CNT} is expressed as the following formula.

$$L_{CNT} = \log_2\lceil 1.1 \times N_E / N_{STG} \rceil.$$

According to the result of the value of N_{Eave} shown in Fig. 8, the required bit length of each counter is calculated. The target error *DNL* is 1/1,024. Table III shows the result. The required bit length is around 5-7 bit. The required bit length tends to decrease as N_{STG} increases.

V. Conclusions

In this paper, we have analyzed the TDC with the stochastic self-calibration using two ring oscillators. Here, we summarize this study.

1) The histogram of each bin converges to the corresponding buffer delay value in a well-behaved manner; the *DNL* measurement error decreases monotonically in proportion to the increase of the number of the times of the measurement.
2) Accordingly, the required number of the measurement times is in proportion to the required accuracy of the calibration.
3) When both of the frequencies of the two ring oscillators are not the prime frequencies, the convergence of the calibration is not guaranteed. The simulation results show that the convergent probability is 77.7 % when $N_{STG} = 128$. In other words, 22.3 % are not convergent.
4) According to the above results, we get the following conclusions.
   - Both of the frequencies of the two ring oscillators should be the prime frequencies.
   - When both of the frequencies are the prime frequencies, we estimate the required number of the times of measurement from the target error *DNL*.

Sometimes, the ring oscillators are infected with the injection lock [15]. In this paper, we ignore this effect for theoretical analysis. We will consider it in the future work. The two frequency generators are implemented by the two ring oscillators. However the waveform include considerable amount of jitter. It gives bad influences on the convergence of the calibration. We will consider the strategy to reuse the existing PLL with lower jitter as a frequency generator in a future work. A SOC usually includes scan design in its logic block. If TDC is implemented around the logic block, we can reuse the scan chains as the counters to reduce the extra area.

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Table III
BIT LENGTH OF COUNTERS (*DNL* $= 1/1,024$).

N_{STG}	8	16	32	64	128
N_{Eave}	336.0	1,033.9	1,512.4	2,006.5	2,396.0
L_{CNT}	6	7	6	6	5

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