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# An Analysis of Stochastic Self-Calibration of TDC Using Two Ring Oscillators

Kentaroh Katoh, Yuta Doi, Satoshi Ito, Haruo Kobayashi,
Ensi Li, Nobukazu Takai, Osamu Kobayashi

群馬大学
GUNMA UNIVERSITY

# Contents

- Background
  - Motivation
  - TDC
  - Abstract of Stochastic Calibration
  - Aim of Study
- Preliminaries for Simulation
- Simulation Results
- Conclusion

# Motivation

Advanced CMOS Process

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Variation → Timing Errors

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Serious Timing-Related Problems

# TDC for solution of timing-related problems

**Examples of Timing-Related Problems**

Jitter of High-Speed Serial Interface

Delay Fault of Logic Circuit

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**Solution**

On-Chip Delay Measurement

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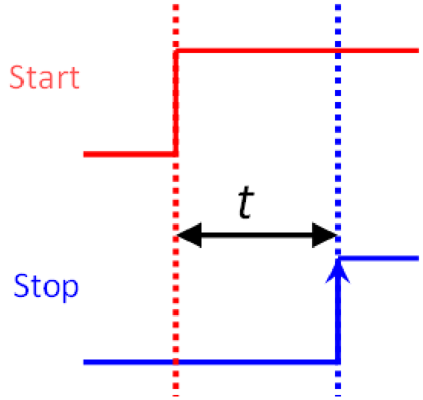
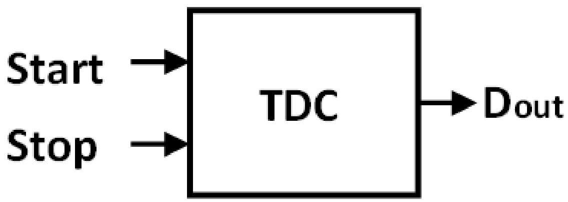
**TDC** (Time to Digital Converter)

# TDC (Time to Digital Converter)

- An On-Chip Delay Measurement Circuit
- Time Interval ⟹ Digital Value

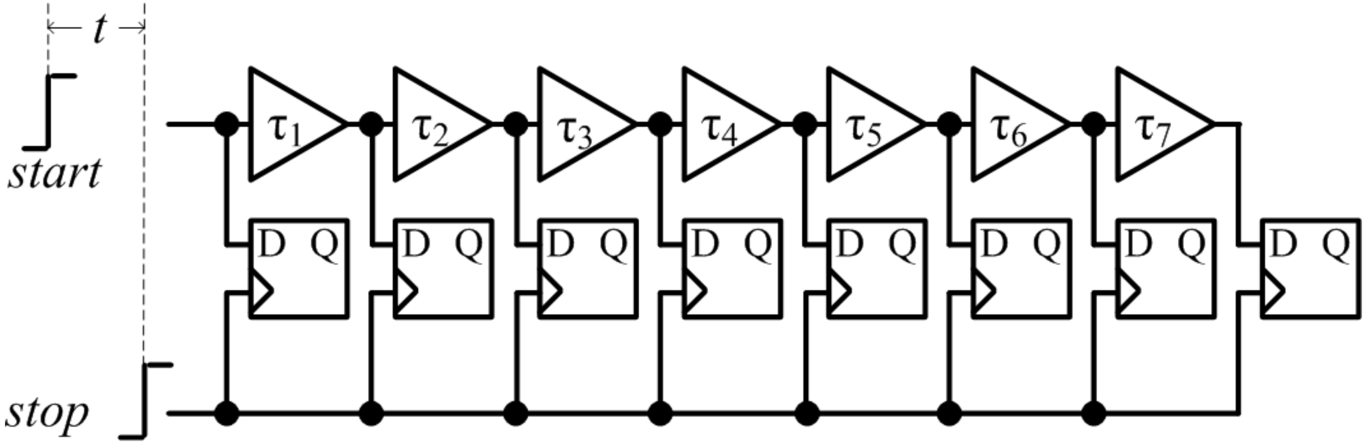



- Consists of CMOS digital elements

  ⟹ can be embedded in advanced VLSI

# Basic TDC




| $t$ | TDC Code | $t$ | TDC Code |
|---|---|---|---|
| $0 < t < \tau_1$ | 10000000 | $\tau_4 < t < \tau_5$ | 11111000 |
| $\tau_1 < t < \tau_2$ | 11000000 | $\tau_5 < t < \tau_6$ | 11111100 |
| $\tau_2 < t < \tau_3$ | 11100000 | $\tau_6 < t < \tau_7$ | 11111110 |
| $\tau_3 < t < \tau_4$ | 11110000 | $\tau_7 < t$ | 11111111 |

# Problems of TDC

Advanced CMOS Process

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Variation ⇨ Delay Variation of Buffers

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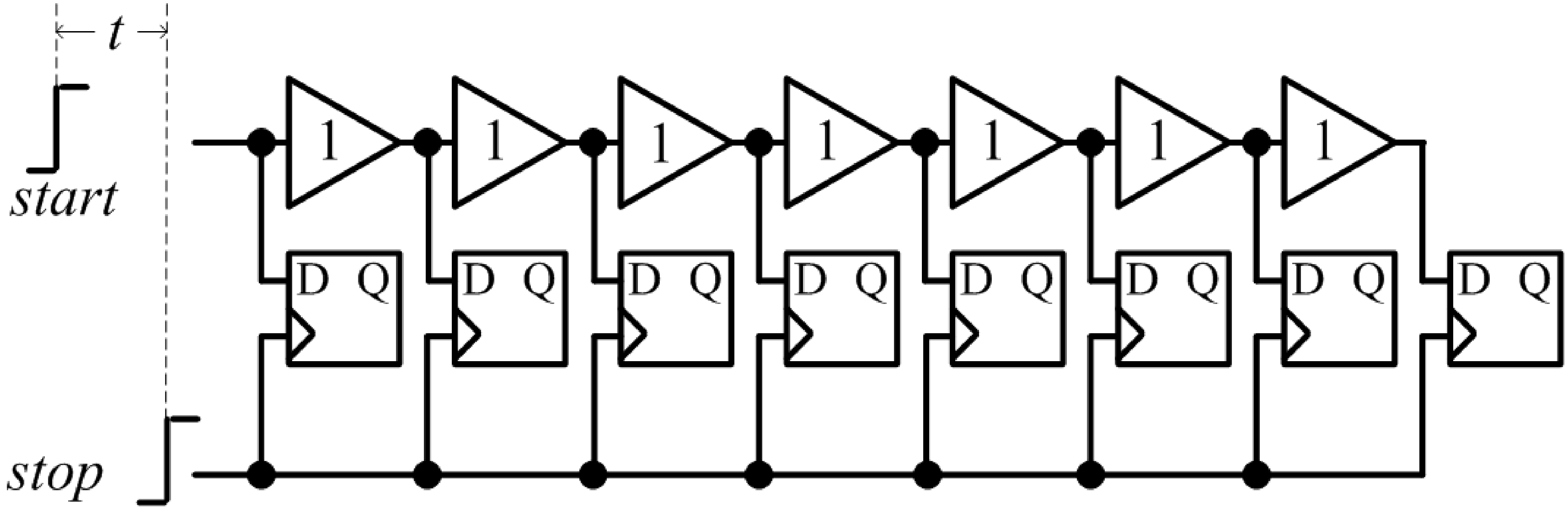
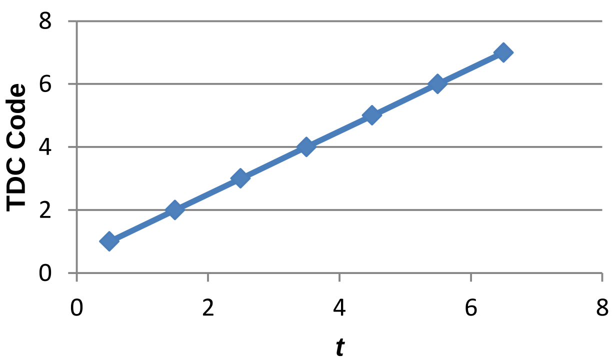
Non-linearity Characteristics ⇨ Problem

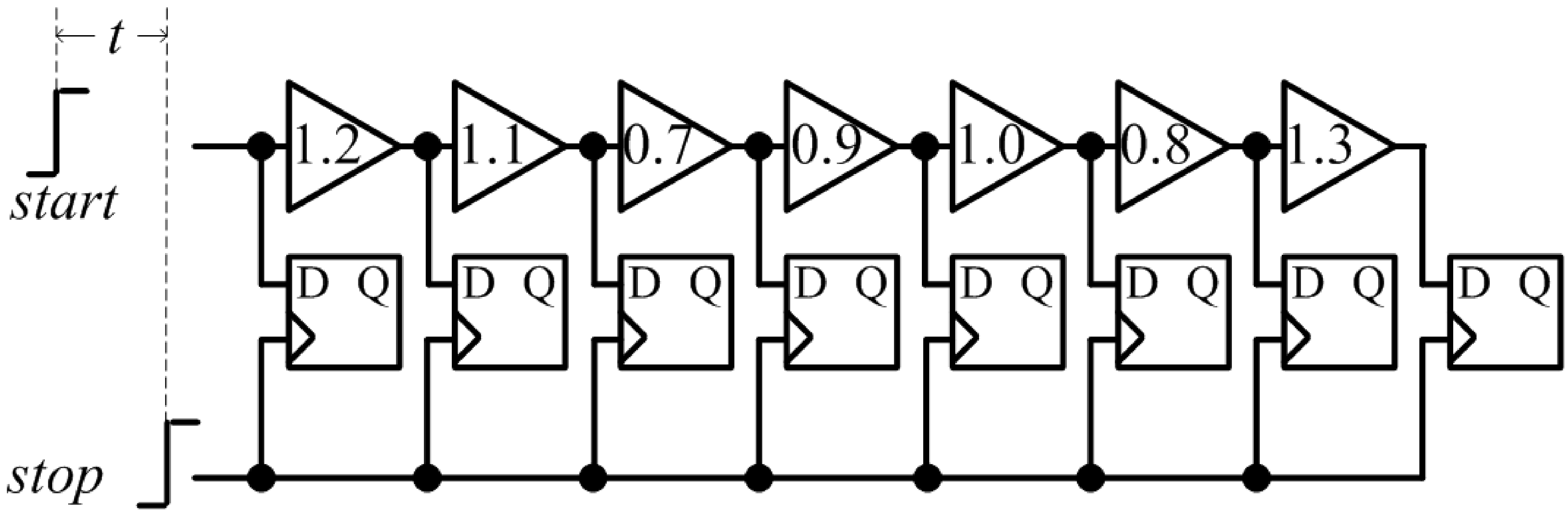
# Problems of TDC (Cont.)




| *t* | TDC Code | *t* | TDC Code |
|---|---|---|---|
| 0.0 < *t* < 1.0 | 10000000 | 4.0 < *t* < 5.0 | 11111000 |
| 1.0 < *t* < 2.0 | 11000000 | 5.0 < *t* < 6.0 | 11111100 |
| 2.0 < *t* < 3.0 | 11100000 | 6.0 < *t* < 7.0 | 11111110 |
| 3.0 < *t* < 4.0 | 11110000 | 7.0 < *t* | 11111111 |



# Problems of TDC (Cont.)




| *t* | TDC Code | *t* | TDC Code |
|---|---|---|---|
| 0.0 < *t* < 1.0 | 10000000 | 4.0 < *t* < 5.0 | 11111000 |
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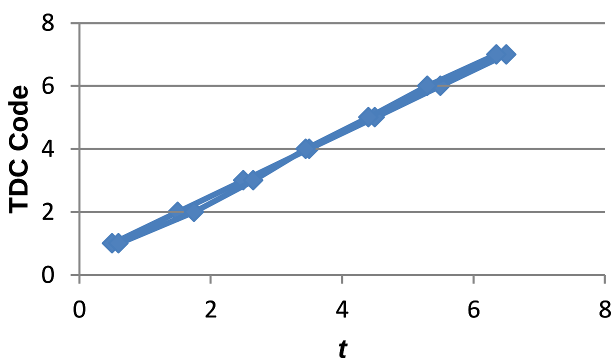
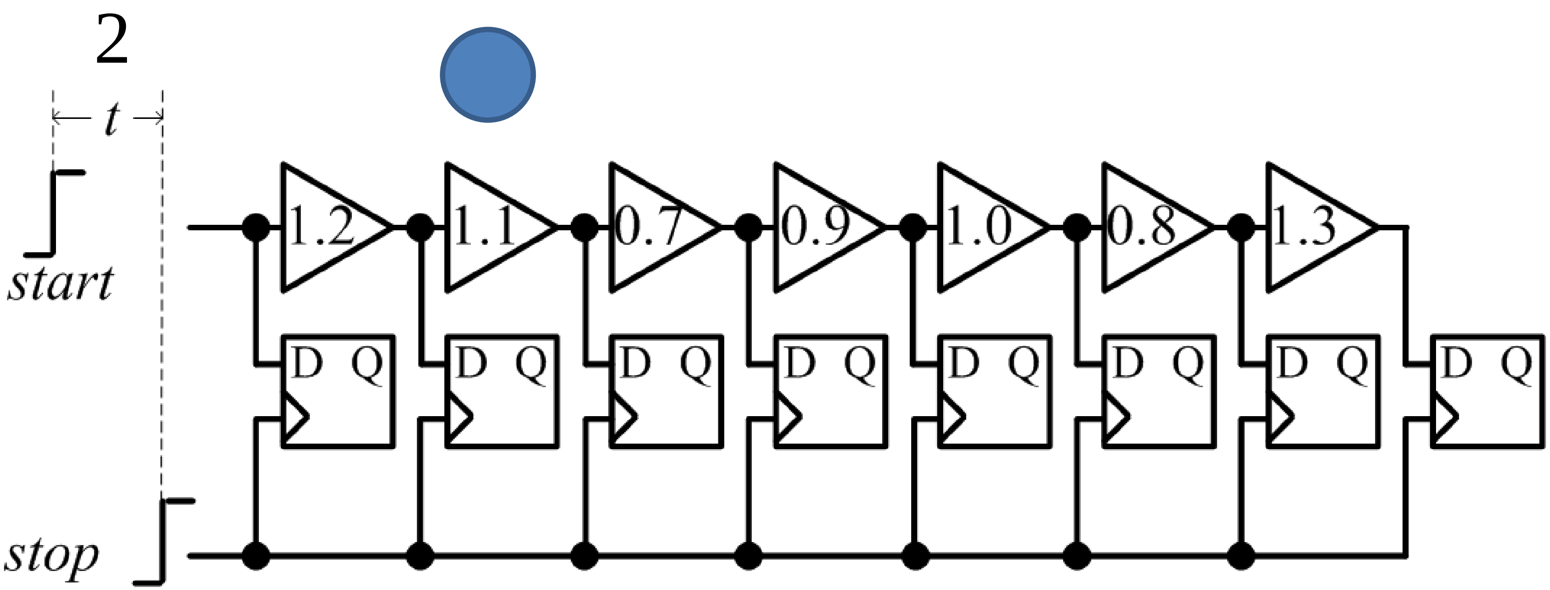


# Basics of stochastic calibration

- Stochastic Calibration

  → Applied Histogram Method
- Stochastic Time Interval is launched from
- *start* and *stop* input



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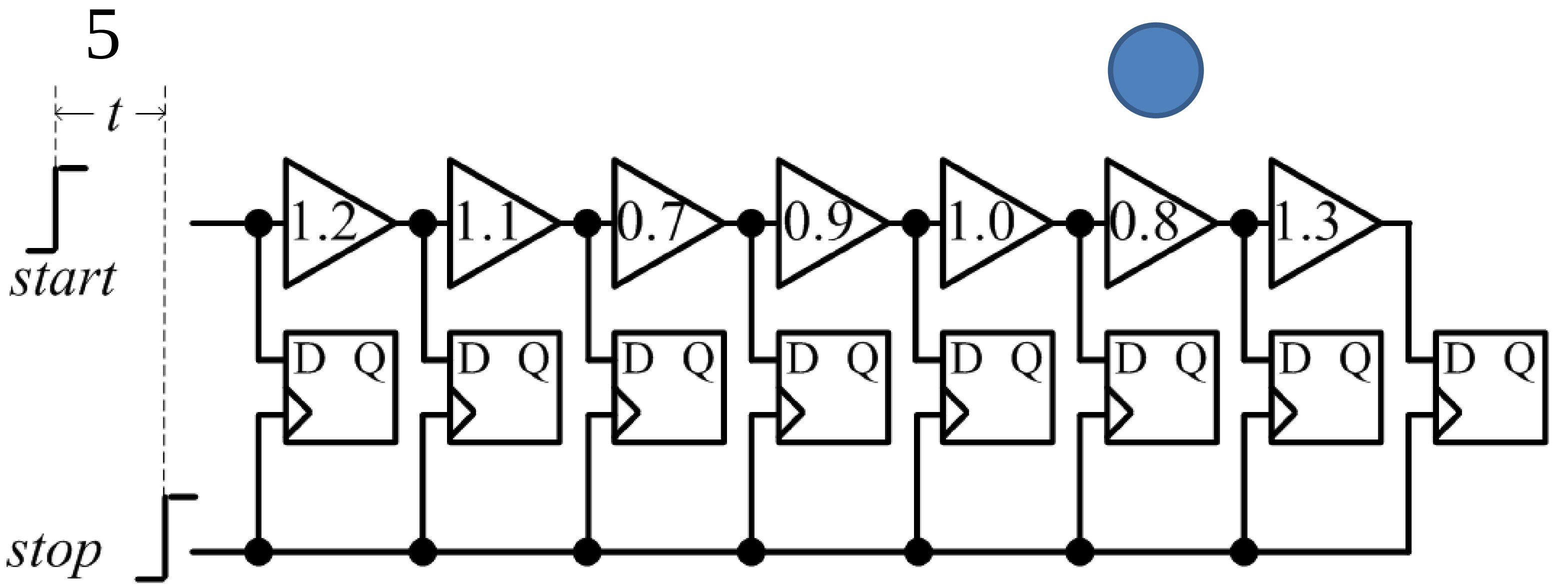

# Basics of stochastic calibration

- Stochastic Calibration

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- Stochastic Time Interval is launched from
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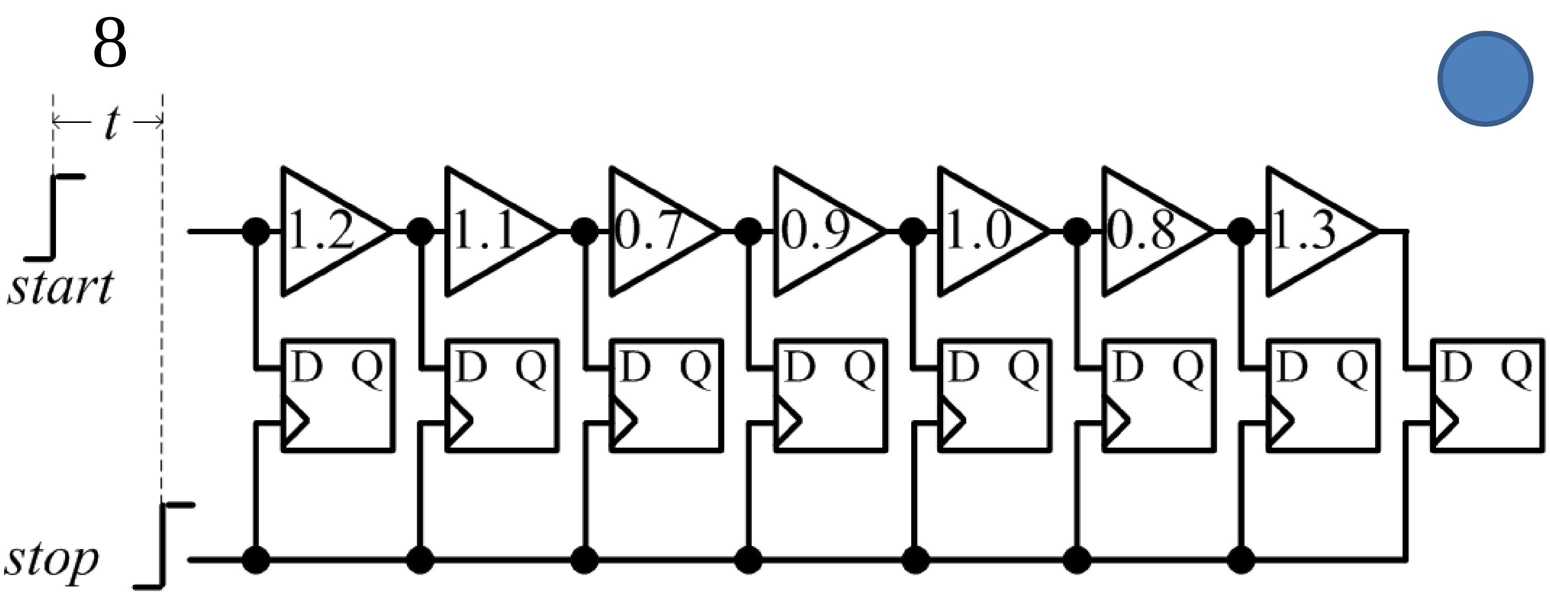
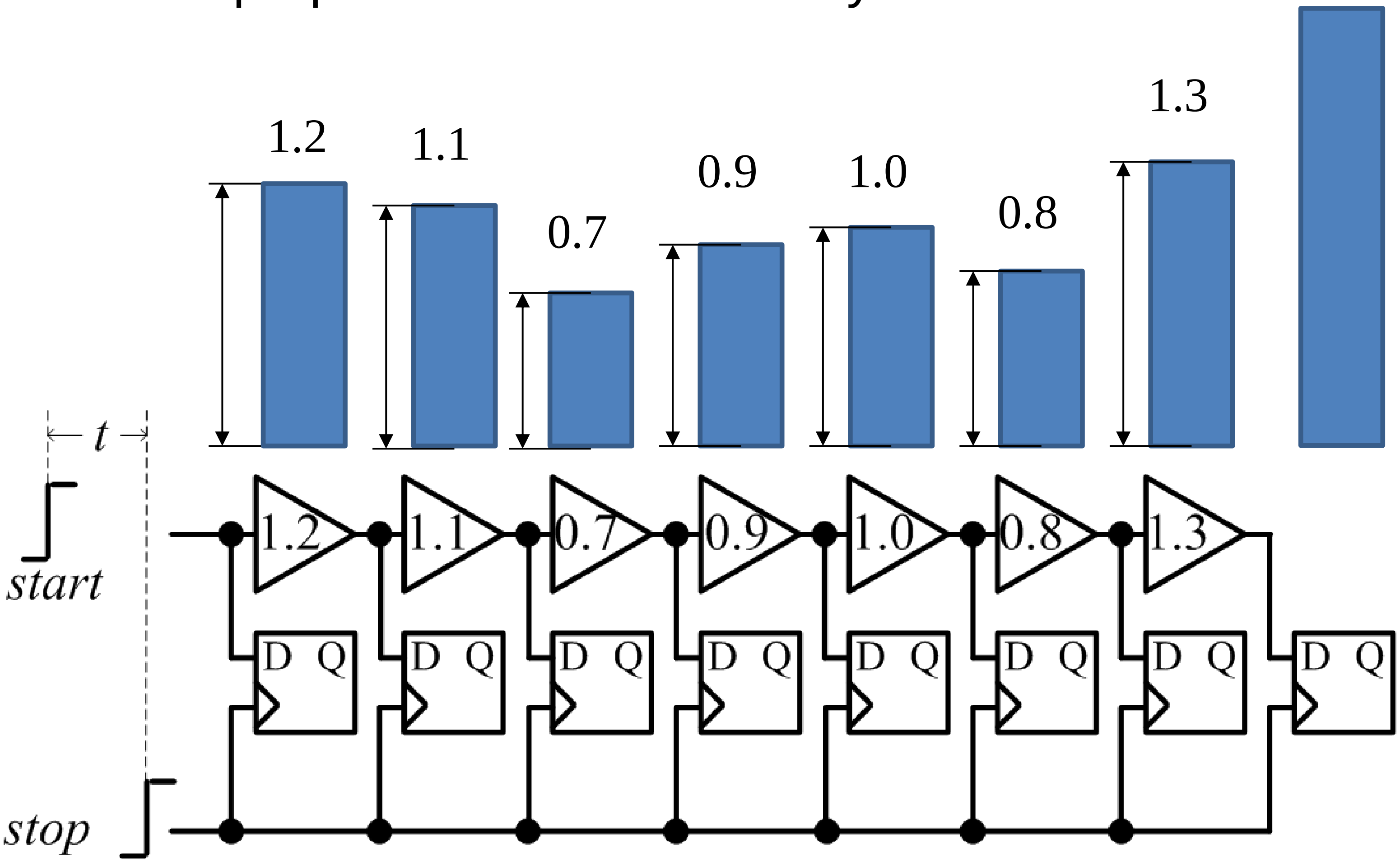


# Basics of stochastic calibration

- When Distribution of time interval is uniform
- Each length of each bin is convergent in proportion to relative delay of each buffer



# Basics of stochastic calibration 2

- Time interval following uniform dist.

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- Two ring oscillators with no correlation

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- Generate time interval following uniform dist. with low extra area

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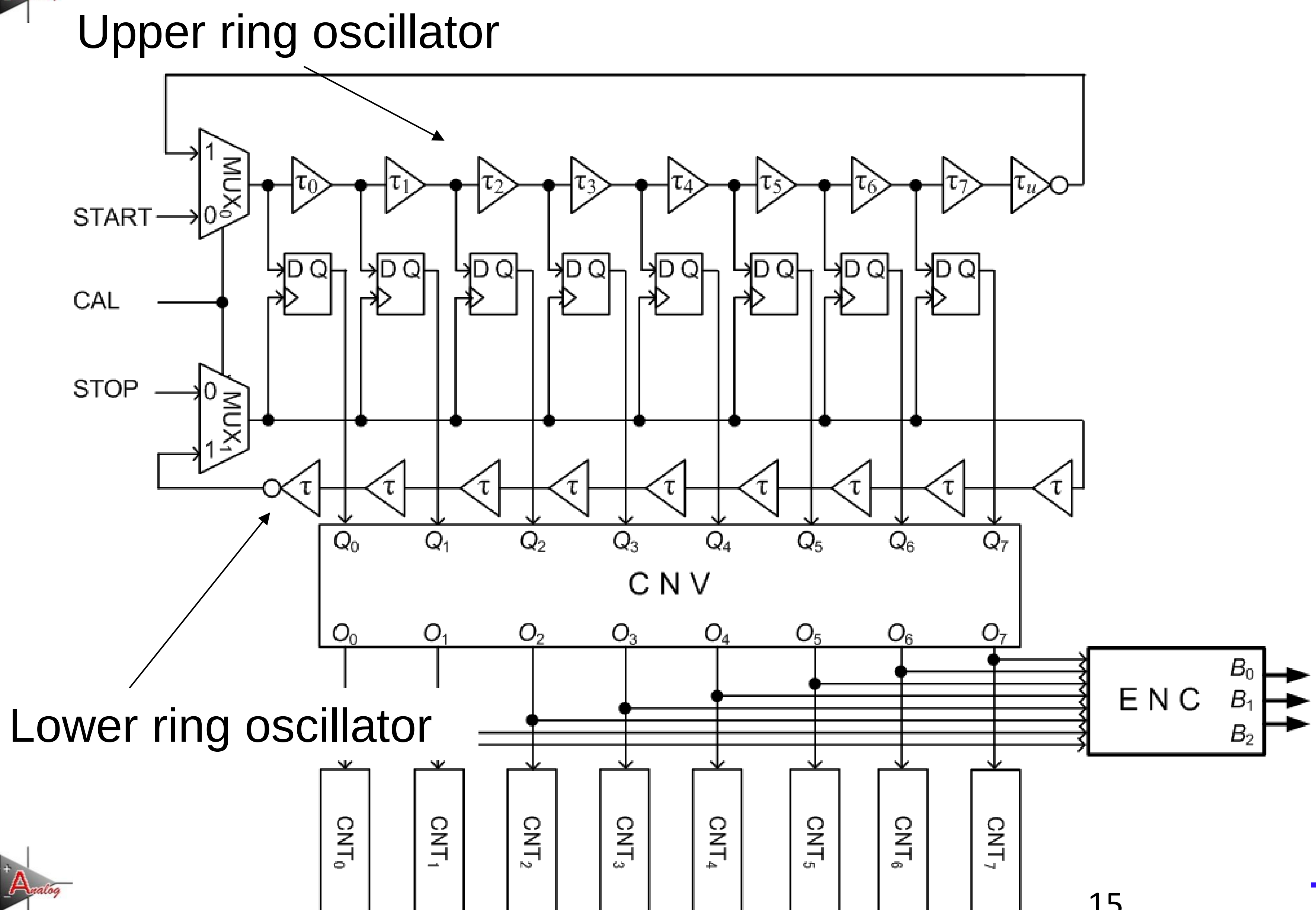
- Apply two ring oscillators as generator of time interval

# Stochastic calibration architecture [10]



# Calibration and design parameters

- Calibration Parameters
  - Probability of convergence
  - Time required for convergence

  depend on
- Design Parameters
  - Cycles of ring oscillators
  - Number of stages
  - Phase difference of ring oscillators

# Aim of study

- For top-down design of calibration
- designer need relation between calibration parameters and design parameters

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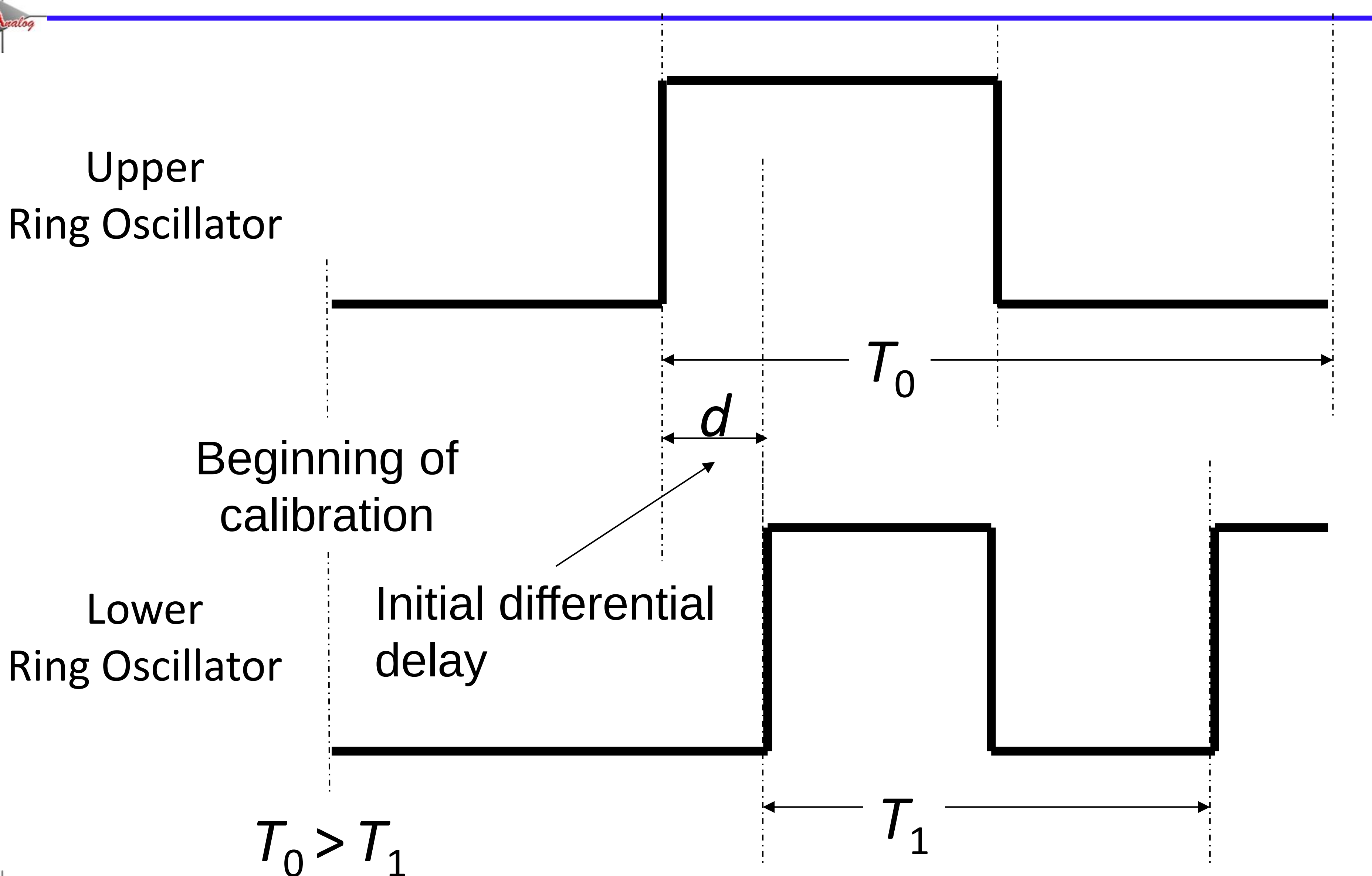
- Analyze relation between calibration parameters and design parameters to get **guideline of calibration design**

# Contents

# Definition of cycles of two ring oscillators



# Definition of DNL

$$dnl_{ij} = \frac{T_i}{\sum_{i=1}^{N_{STG}-2} T_i} - \frac{b_{ij}}{\sum_{i=1}^{N_{STG}-2} b_{ij}}$$

$$DNL_j = \max(|dnl_{1j}|, \cdots, |dnl_{(N_{MEAS-2})j}|)$$

$dnl_{ij}$:differential non-linearity error of *i*-th stage after *j*-th sampling

$DNL_j$: differential non-linearity error after *j*-th sampling

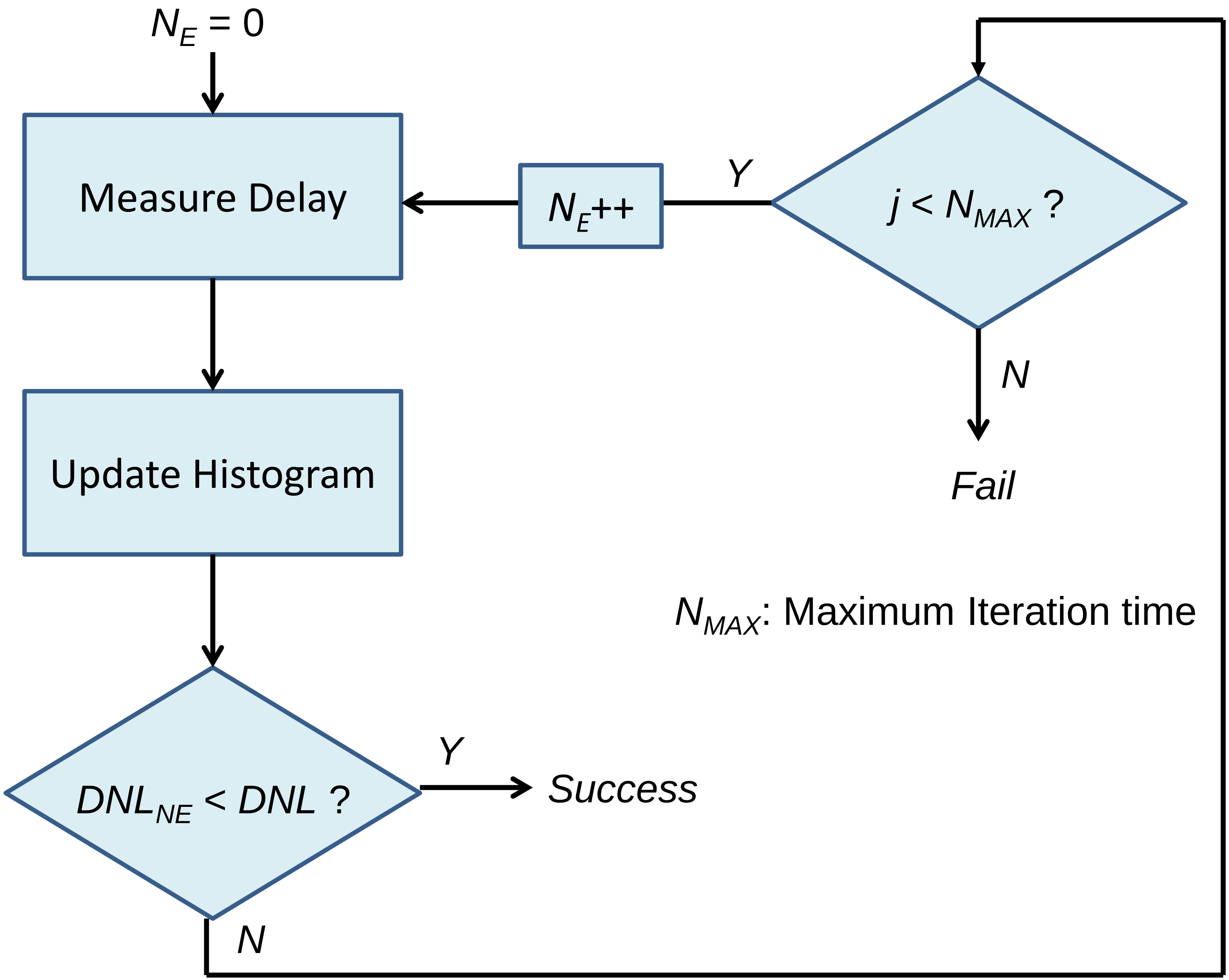
$T_i$ :Delay of buffer of *i*-th buffer

$b_{ij}$ :Length of bin of *i*-th stage after *j*-th sampling

# Definition of required measurement for convergence

- $N_E(TDC, T_0, T_1, d, DNL)$ : Number of required measurement for convergence of TDC within target DNL when cycles of upper and lower ring oscillator are $T_0$ and $T_1$.

# Calculation of $N_E$



# Definition of convergent probability

- Convergent probability $P_E(DNL)$: Probability of success of calibration within a pre-defined error DNL when calibration is performed multiple times

$$P_E(DNL) = N_{SCAL} / N_{CAL} \times 100.0$$

$N_{SCAL}$: Times of which calibration is success
$N_{CAL}$: Execution times of calibration

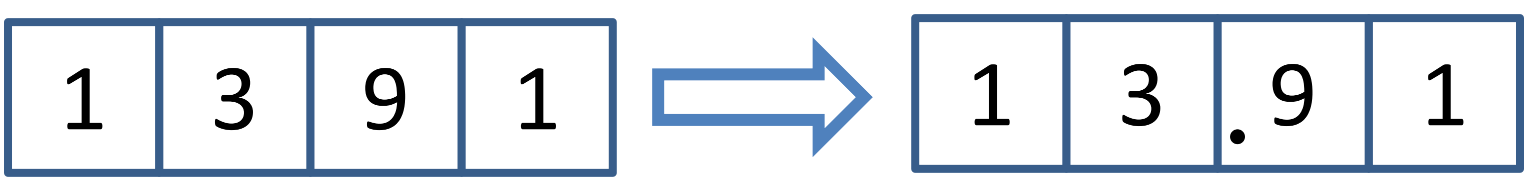
# Definition of prime cycles

- A prime cycle *c* is defined as follows

$$c = p / 10^n$$

$p$: prime number
$n$: number of figures of the fraction part

$n = 2$




Prime number → Prime cycle

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# Experiments

- Design Parameters
  - Cycles of two ring oscillators ($T_0$, $T_1$) VS
    - Convergent probability ($P_E$)
    - Required measurement time to convergent ($N_E$)
  - Initial differential delay ($d$) VS
    - Required measurement time to convergent ($N_E$)
  - Bit length of each counter

# Experimental setup

- Buffer delay is set to 1 (unit delay)
- Varied 100 TDCs ($TDC_0$-$TDC_{99}$) are constructed
- Variation is 10% of buffer delay following gaussian distribution
- Maximum delay measurement times:$N_{MAX}=2^{14}$
- Number of figure of fraction: $n=2$

# Cycle of two ring oscillators ($T_0$, $T_1$) Spec.

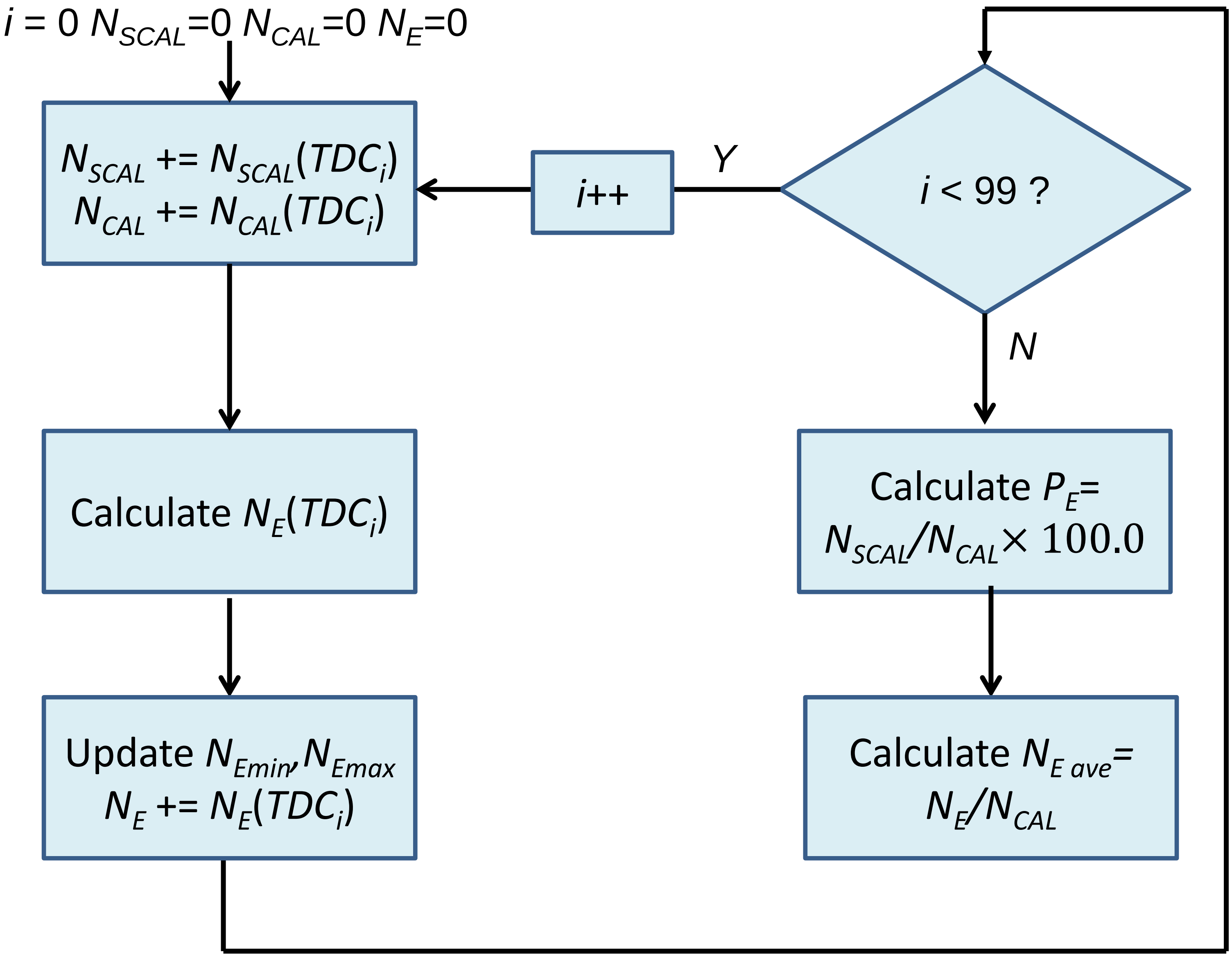
- $T_0 > T_1$
- Evaluate in following three cases
  - Case 1 : Both $T_0$ and $T_1$ are prime cycles
  - Case 2 : $T_0$ is multiple of $T_1$
  - Case 3 : Arbitrary values of $T_0$ and $T_1$

# Cycle of two ring oscillators ($T_0$, $T_1$) Spec. 2

- Parameter set up
  - $N_{STG}$ : 8 16 32 64 128
  - Upper ring oscillator cycle $T_0$ is fixed to $T_{p0}$
  - Lower ring oscillator cycle $T_1$ is swept up from $T_{min}$ to $T_{max}$
  - *DNL* 1/1,024
  - Calibrate multiple times and calculate $P_E$ and $N_E$
  - Initial differential delay $d$ 0

| $N_{STG}$ | $T_{min}$ | $T_{max}$ | $T_{p0}$ |
|---|---|---|---|
| 8 | 2 | 12 | 11.93 |
| 16 | 2 | 18 | 17.89 |
| 32 | 2 | 36 | 35.93 |
| 64 | 2 | 68 | 67.93 |
| 128 | 2 | 132 | 131.87 |

# Simulation Sequence



# Cycle of two ring oscillators ($T_0$, $T_1$) Spec. 3

- Convergent probability $P_E$ spec.

| Case | $N_{STG}$ | | | | |
|---|---|---|---|---|---|
| | 8 | 16 | 32 | 64 | 128 |
| Case 1 | 100.0 | 100.0 | 100.0 | 100.0 | 100.0 |
| Case 2 | 0.0 | 0.0 | 0.0 | 0.0 | 0.0 |
| Case 3 | 38.6 | 43.9 | 56.4 | 75.8 | 78.5 |

# Cycle of two ring oscillators ($T_0$, $T_1$) Spec. 4

- Required Measurement Time $N_E$ spec.

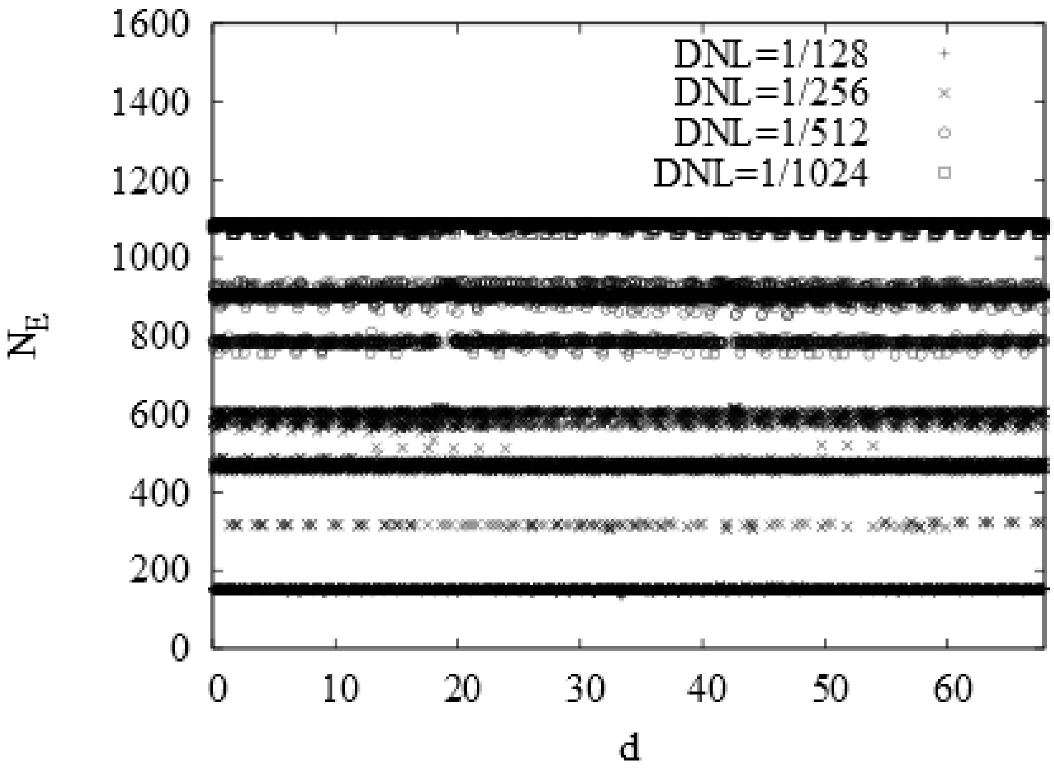
| $N_E$ | Case | $N_{STG}$ | | | | |
|---|---|---|---|---|---|---|
| | | 8 | 16 | 32 | 64 | 128 |
| $N_{Emin}$ | Case 1 | 367 | 517 | 605 | 772 | 802 |
| | Case 2 | 0 | 0 | 0 | 0 | 0 |
| | Case 3 | 359 | 464 | 640 | 731 | 984 |
| $N_{Eave}$ | Case 1 | 633.1 | 1,060.0 | 1,509.6 | 1,976.3 | 2,323.3 |
| | Case 2 | 0 | 0 | 0 | 0 | 0 |
| | Case 3 | 648.7 | 1,052.4 | 1,303.8 | 1,724.8 | 1,911.7 |
| $N_{Emax}$ | Case 1 | 798 | 1,597 | 3,178 | 6,324 | 10,000 |
| | Case 2 | 0 | 0 | 0 | 0 | 0 |
| | Case 3 | 3,427 | 10,000 | 10,000 | 6,381 | 10,000 |

# Initial differential delay specification

- Parameter setup
  - $T_0$ ⇒ $T_{p0}$, $T_1$ ⇒ 2.11 fixed
  - $d$ is swept up from 0 to $T_0$
  - $N_{Eave}$ is calculated
  - $DNL$ = 1/128, 1/256, 1/512, 1/1,024

# Initial differential delay specification

- Result



# Bit length of each counter

- Calculate bit length of each counter with the following equation assuming 10% variation
- DNL 1/1,024

$$L_{CNT} = \log_2 \lceil 1.1 \times N_E / N_{STG} \rceil$$

| $N_{STG}$ | 8 | 16 | 32 | 64 | 128 |
|---|---|---|---|---|---|
| $L_{CNT}$ | 9 | 10 | 9 | 7 | 7 |

# Conclusion

- Analyze the relation between calibration parameters and design parameters
- Analyze not with mathematical analysis but with computer simulation ⇒ higher accuracy
- Get the following two conclusions
  - Both of the frequencies of the two ring oscillators should be the prime frequencies
  - When both of the frequencies are the prime frequencies, we estimate the required number of the times of measurement from the target DNL.

# Questions

- Q. プロセスばらつきを考慮しなかったのはなぜか？
- A. 本研究は設計者への設計ガイドラインを目的としており，特に設計パラメータとキャリブレーション特性の関係について研究を行っているため.