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Digital Compensation for Timing Mismatches in Interleaved ADCs

Ru Yi, Minghui Wu, Koji Asami†, Haruo Kobayashi
Ramin Khatami, Atsuhiro Katayama, Isao Shimizu, Kentaroh Katoh‡,
Division of Electronics and Informatics, Gunma University 376-8515 Japan email: k_haruo@el.gunma-u.ac.jp
† Advantest Corporation, Gunma R&D Center 370-0718 Japan
‡ Tsuruoka National College of Technology, Yamagata 997-8511 Japan

***Abstract*—This paper describes a digital method of reducing timing mismatch effects in time-interleaved ADCs used in ATE systems: we use cross-correlation among channel ADC outputs to detect channel timing skew, and make successive-approximation adjustments to our proposed linear-phase-digital delay filter to compensate for the timing skew. Simulation results validate the effectiveness of the proposed method. We found that using multi-tone input signals with cross-correlation of outputs provided a more robust way of detecting timing skew than using a single-tone input signal. Since our proposed approach is fully digital, it is reliable, and suitable for fine CMOS implementation.**

Keywords: Interleaved ADCs, Timing Skew, Cross-Correlation, Linear Phase Digital Filter, Digital Error Correction, ATE System

I. Introduction

A high-sampling-rate ADC can be implemented with relatively slow circuitry by using multiple time- interleaved ADCs, (Fig.1) [1-7], and this approach is widely used in Automatic Test Equipment (ATE) systems. In such an ADC, several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate. However, mismatches among the channel ADCs — such as offset, gain and bandwidth mismatches, as well as timing skew of the clocks distributed to the channels — degrade SNDR and SFDR of the ADC system as a whole [1].

This paper discusses the most important problem, timing skew, in a time-interleaved ADC system used for sampling high frequency waveforms. We describe our method of using cross-correlation among channel ADC outputs to detect inter-channel skew and our method of compensating for its effects using our previously proposed digital delay filter. We describe the principles and operation, and provide Matlab simulation results.

Hereafter, we will use the following notations:
M: number of channel ADCs in the ADC system,
f_{noise}: pattern noise frequency of the ADC output,
f_{in}: input frequency applied to the ADC system,
f_s: sampling frequency of the ADC system,
T_s: sampling period of the ADC system ($T_s = 1/f_s$).
f_s/M: sampling frequency of each channel ADC.

II. Timing Skew Problem in Time-Interleaved ADC

There are two types of timing errors in an interleaved ADC system: clock jitter (random error) and clock skew (systematic error). Clock jitter effects are unavoidable in any ADC system, but the interleaved architecture also suffers from clock skew effects. Suppose that the clocks $CK_1, CK_2, \ldots, CK_M$ have skews $dt_1, dt_2, \ldots, dt_M$. These skews cause noise (spurious output which is like phase modulation (PM) noise) in the ADC system, and the largest errors in the time domain occur when the input signal has the largest slew rate, or crosses zero. For a sinusoidal input of frequency f_{in}, the envelope of the error signal is largest at zero-crossings with a period of M/f_s. In the frequency domain, the basic error occurs with a period of M/f_s, and the magnitude of the error is modulated by the input frequency f_{in}; the (spurious spectrum) noise peaks are at

$$f_{noise} = -f_{in} + \frac{k}{M} f_s \ (k = 1, 2, 3, ...).$$

Note that SNDR degrades as f_{in} increases.

Suppose that the clocks CK_1, CK_2, …, CK_M have skews dt_1, dt_2, …, dt_M. If the input signal $V_{in}(t)$ is sampled at time $t + dt$ instead of time t, then we have a sampling error

$$e(t) = V_{in}(t + dt) - V_{in}(t)$$

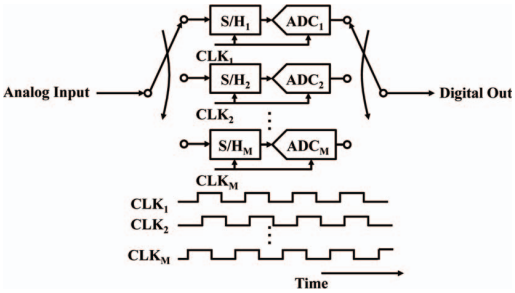

Fig. 1. M-channel time-interleaved ADC.

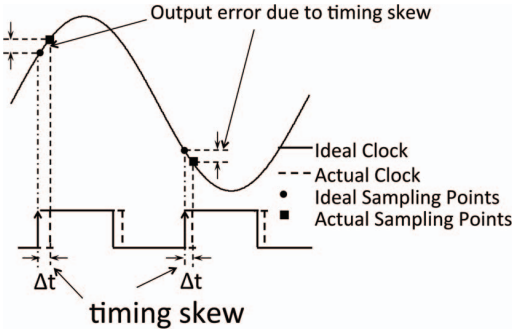

Fig. 2. ADC output error caused by timing skew.

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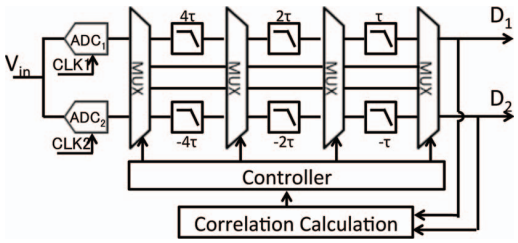


Fig. 3. Block diagram of the proposed technique.

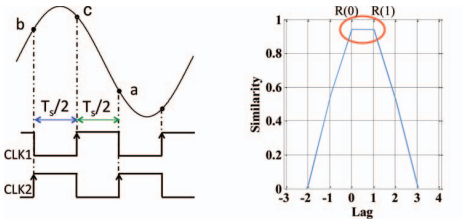


Fig. 4. Cross-correlation between ADC1 and ADC2 outputs when there is no timing skew.

which can be approximated by $e(t) \approx [dV_{in}(t))/dt]dt$ (Fig.2). This skew causes so-called pattern noise in the ADC system, and in the time domain the largest error occurs when the input signal has the largest slew rate. The effect of timing skew in a time-interleaved ADC system is most serious for high frequency and large amplitude analog signal measurements, when the slew rate $(dV_{in}(t)/dt)$ is highest.

III. Proposed Method of Timing Skew Effect Reduction

We first analyze a 2-channel interleaved ADC, and extend this analysis to a 4-channel ADC in Section V. Fig.3 shows a block diagram of our proposed timing skew compensation system.

Multiplexers and digital delay filters [5], [6] are used to apply delays of $\pm 4\tau$, $\pm 2\tau$ $\pm\tau$ to channel ADC1, ADC2 outputs (here τ can be set to an arbitrarily small value.) We use a digital signal processor to perform cross-correlation, and a digital controller to control the selection signals of the multiplexers. The skew compensation procedure for Fig.3 is as follows:

1) For both ADC1 and ADC2 outputs, the delay filters are deselected by the multiplexers ("through" is selected).
2) The digital signal processor calculates the cross-correlation between D_1 and D_2 in Fig.3. A comparison of R(0) and R(1) shows whether the phase shift of CLK2 relative to CLK1 is greater or less than π (Figs.4,5).
3) Based on this information, the digital controller sets the selection signals of the first and second multiplexers for "ADC1 with 4τ delay filter and ADC2 with -4τ" or for "ADC1 with -4τ and ADC2 with 4τ", to compensate for timing skew effects between CLK1 and CLK2.
4) The digital signal processor then calculates the cross-correlation between D_1 and D_2.
5) Based on a comparison of R(0) and R(1), the digital controller then sets the selection signals of the second and third multiplexers for "ADC1 with 2τ delay filter and ADC2 with -2τ" or for "ADC1 with -2τ and ADC2 with 2τ".
6) The digital signal processor then calculates the cross-correlation between D_1 and D_2.
7) Based on a comparison of R(0) and R(1), the digital controller then sets the selection signals of the third and fourth multiplexers for "ADC1 with τ delay filter and ADC2 with $-\tau$" or for "ADC1 with $-\tau$ and ADC2 with τ".

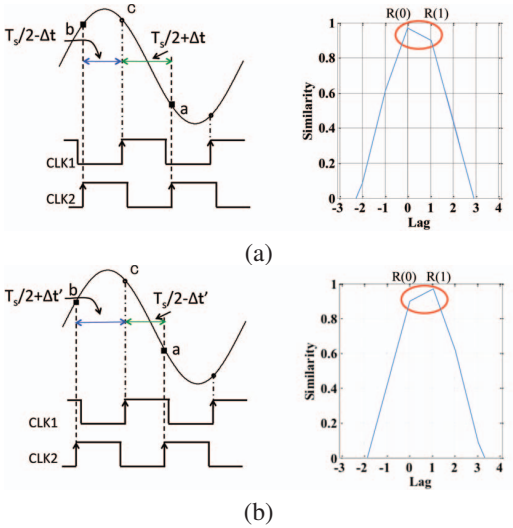


Fig. 5. Cross-correlation between ADC1 and ADC2 outputs when there is timing skew. (a) Case 1. (b) Case 2.

Digital compensation for timing skew to within $\pm\tau$ can be realized. In the example above, we have described 3-step successive approximation, but of course this method can be extended to a general N-step binary-search successive approximation.

The timing skew detection and compensation techniques are explained in detail below:

A. Skew Detection using Cross-Correlation

Signal processing theory tells us that cross-correlation indicates the similarity between two time sequence series f, g and it is defined as follows.

(1) For continuous-time cross-correlation:

$$(f * g)(t) = \int_{-\infty}^{\infty} f^*(\tau)g(t+\tau)d\tau. \quad (1)$$

(2) For discrete-time cross-correlation:

$$R(n) = (f * g)(n) = \sum_{m=-\infty}^{\infty} f^*[m]g[n+m]. \quad (2)$$

Here f^* is the complex conjugate of f.

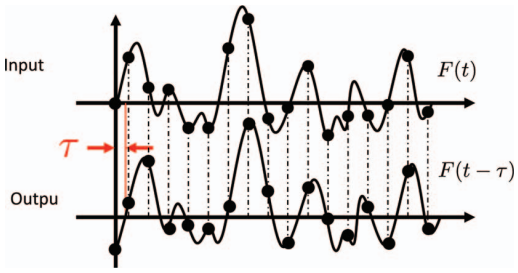


Fig. 6. Linear phase characteristics.

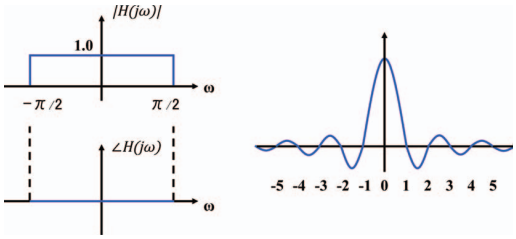


Fig. 7. (a) Ideal analog filter frequency response. (b) Impulse response.

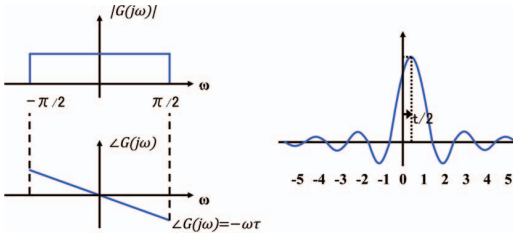


Fig. 8. (a) Ideal analog filter frequency response with phase rotation. (b) Impulse response (time-shifted $sinc$ function.)

If there is no timing skew in a 2-channel interleaved ADC system, then the sampling timing is shifted exactly by $T_s/2$ between channel ADCs 1 and 2, and in this case the cross-correlation values between b and c and that between c and a are the same (Fig.4). However, in an actual interleaved ADC system, a finite skew dt is unavoidable; timing shift from c to a is $T_s/2-dt$ and that from b to c is $T_s/2+dt$ and the cross-correlation values are different, as illustrated in Fig.5 [4]. If $dt>0$ then $R(0)>R(1)$; otherwise $R(0)\leq R(1)$. Thus the relative size of $R(0)$ and $R(1)$ values tells us if dt is positive or negative.

B. Skew Effect Compensation using Digital Delay Filter

Fine timing skew adjustments are frequently used in ATE systems, where linear phase characteristics are desired to preserve signal waveforms in the time domain (Fig.6). Digital techniques are preferred for timing skew compensation because they are stable, reliable, and easy to implement compared with analog techniques. However, conventional linear phase digital filters cannot be applied to fine timing skew adjustment because their delay time resolution is limited. We have previously proposed a digital filter with novel linear phase condition, and shown that its delay time resolution can be arbitrary fine (i.e., its group delay can be set with arbitrary small time resolution). An ideal linear phase digital filter would have an infinite number of taps, but we can create a close approximation with a finite number of taps by using a window function.

In this section, we show the extended linear phase characteristics for digital filters which do not necessarily have odd or even coefficient symmetry, and show that the time resolution of the group delay can be arbitrary small. For simplicity, we first discuss this without considering causality. Let us consider the ideal analog filter shown in Fig.7.

If we shift the impulse response in Fig.7(b) by τ, we have the waveform of (Fig.8(b)). By applying a Fourier transform to it, we obtain its frequency characteristic as shown in Fig.8(a). We see that the gain characteristic is the same as that in Fig.7(a) but the phase characteristic slope is rotated by $\exp(-j\omega\tau)$; this can be explained by the Fourier transform time-shift property. We call this filter in Fig.8 an ideal delay filter.

We convolve an FIR digital filter whose characteristics we would like to use for frequency compensation to this ideal delay filter with a delay of τ. We shift the FIR digital filter impulse response by τ; the ideal number of filter taps would be infinite, but we use a finite number with an appropriate window function.

We here incorporate delay filters with delays of $\pm 3\tau$, $\pm 2\tau$ and $\pm\tau$ to allow timing skew to be corrected within a range -15τ to 15τ with a time resolution of τ, and show Matlab simulation results in Section IV.

IV. Simulation Results

We have performed Matlab simulations to confirm the effectiveness of the proposed method with a 2-channel interleaved ADC. Timing skew dt is $0.002T_s$, and a three-tone signal is used in the skew detection. Table I shows the simulation conditions, and Fig.9 shows the operation.

TABLE I
Simulation Conditions

Timing skew	$+0.002T_s$
Number of filter taps	21
Window function	Blackman
τ for digital delay filter	$0.001T_s$

A. Skew Detection using Cross-Correlation

We used a three-tone signal as the calibration input because we found that the cross-correlation is more sensitive to timing skew than with single-tone sinewave input (see Section V).

B. Skew Effect Compensation using Digital Delay Filter

Fig.10 (a) shows the output power spectrum of a 2-channel interleaved ADC without timing skew. Fig.10 (b) shows the spectrum *before* timing skew compensation, and Fig.10 (c)

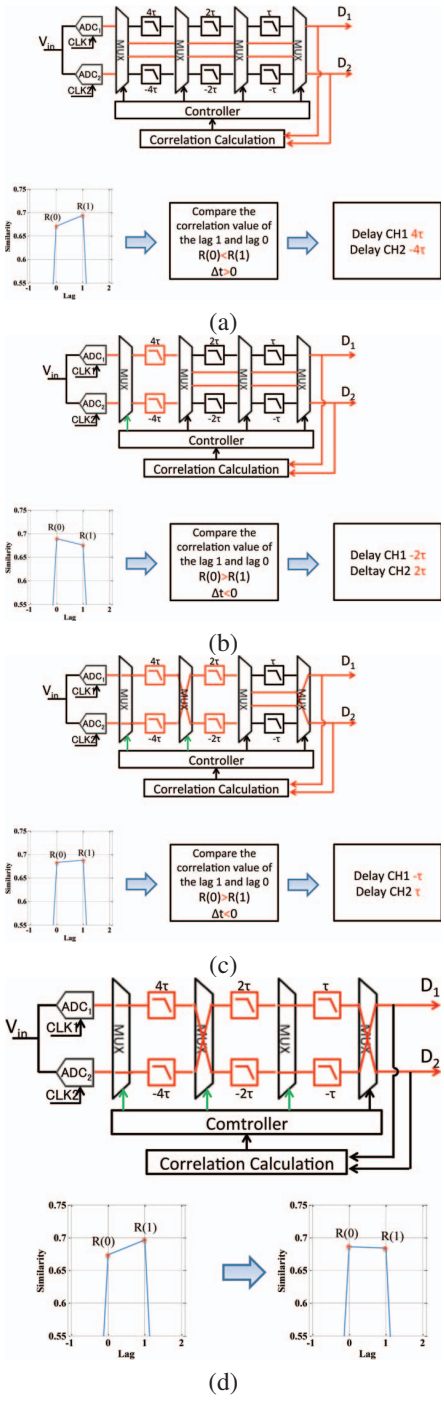


Fig. 9. Simulation results for condition 1. From top to bottom: before compensation, compensation step 1 with 4τ, step 2 with 2τ, step 3 with τ.

shows it *after* skew compensation; we see that spurious components are suppressed and have confirmed that our proposed method is effective.

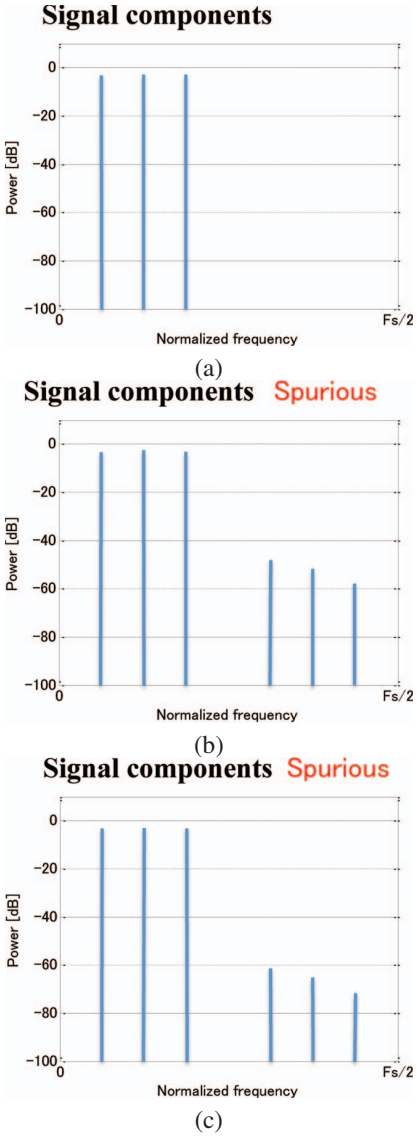


Fig. 10. Simulation results in frequency domain for condition 1. (a) No skew. (b) Skew without compensation. (c) Skew with skew compensation.

V. Discussions

A. Skew Compensation Adjustment

Skew compensation adjustment may be performed in the foreground or in the background.

(1) Foreground Skew Compensation Adjustment: The normal operation of the ADC is stopped for skew compensation adjustment, and skew compensation adjustment is started. Then a specific input is applied for the adjustment steps.

(2) Background Skew Compensation Adjustment: Skew compensation is adjusted during the normal operation of the ADC. This is desirable from the viewpoint of not stopping normal operation —however, convergence of the skew compensation is strongly dependent on the input signal during this adjustment step.

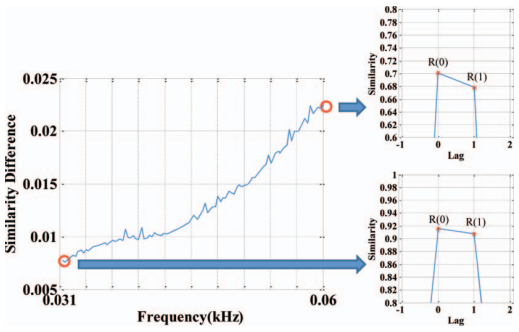


Fig. 11. Cross-correlation versus single-tone input frequency f_{in}.

B. Input Signal for Skew Compensation Adjustment

We consider that foreground skew compensation adjustment is practical in ATE system applications. We have investigated input signals suitable for skew compensation adjustment, and our conclusions are as follows.

(1) Single-tone Signal : In the single-tone input case, we found that that as the input frequency f_{in} increases, the cross-correlation is more sensitive to timing skew (Fig.11).

(2) Multi-tone Signal : For multi-tone input, we found that the cross-correlation is more sensitive to timing skew than for a sinusoidal input (Figs.12, 13); for multi-tone input, convergence is better even if the input signal includes noise.

Fig. 12 shows input signal waveforms used for compensation adjustment, where T_s is normalized as 2, and the initial phases of multi-tones to obtain minimum crest-factor are considered as follows [7], [8], [9]:

$$
\begin{aligned}
f_1(t) &= \frac{7\sqrt{2}}{10}\sin(0.051\pi t+\frac{\pi}{4}).\\
f_2(t) &= \frac{4\sqrt{2}}{11}[\sin(0.051\pi t+\frac{\pi}{4})+\sin(0.143\pi t+\frac{3}{4}\pi)].\\
f_3(t) &= \frac{\sqrt{2}}{4}[\sin(0.051\pi t+\frac{\pi}{4})+\sin(0.143\pi t+\frac{7}{12}\pi)\\
&+ \sin(0.255\pi t+\frac{19}{12}\pi)].\\
f_4(t) &= \frac{2\sqrt{2}}{9}[\sin(0.051\pi t+\frac{\pi}{4})+\sin(0.143\pi t+\frac{1}{2}\pi)\\
&+ \sin(0.255\pi t+\frac{3}{4}\pi)+\sin(0.341\pi t+\frac{5}{2}\pi)].
\end{aligned}
$$

For multi-tone inputs, a multi-tone signal with controlled phases can be generated using an arbitrary waveform generator [10].

Fig.13 shows the cross correlation difference $|R(0)-R(1)|$ with respect to timing skew $\delta t/T_s$ obtained using $f_1(t)$, $f_2(t)$, $f_3(t)$, $f_4(t)$, and we see multi-tone signals are better.

C. Extension to 4-channel Interleaved ADC

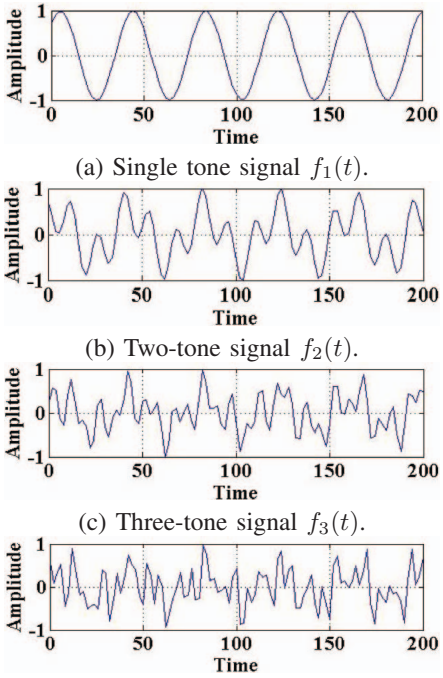
Our proposed method can be extended to the 4-channel interleaved ADC case, and we consider two methods.

Method 1 :

1) Compensate for timing skew between channels ADC1 and ADC3 using the proposed method.
2) Also compensate for timing skew between channels ADC2 and ADC4 using the proposed method.
3) Compare R(0) values for ADC1 and ADC2, and those of ADC3 and ADC2. Then compensate for timing skew between ADC1 and ADC3 as well as between ADC2 and ADC4.

Method 2 :

1) Compensate for timing skew between channels ADC1 and ADC3 using the proposed method.
2) Compare R(0) values for ADC1 and ADC2, and those for ADC3 and ADC2. Then compensate for the timing skew of ADC2.



(a) Single tone signal $f_1(t)$.

(b) Two-tone signal $f_2(t)$.

(c) Three-tone signal $f_3(t)$.

(d) Four-tone signal $f_4(t)$.

Fig. 12. Input signal waveforms for foreground compensation adjustment.

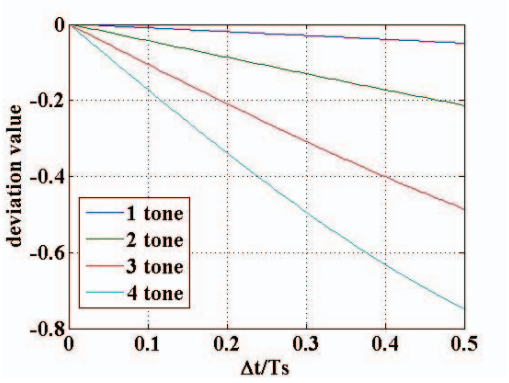
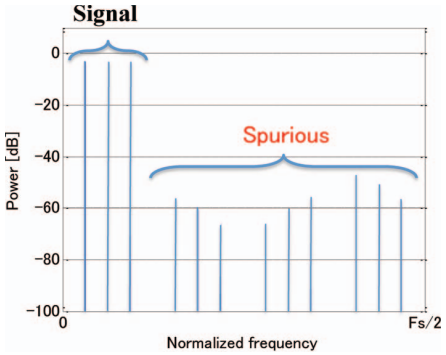
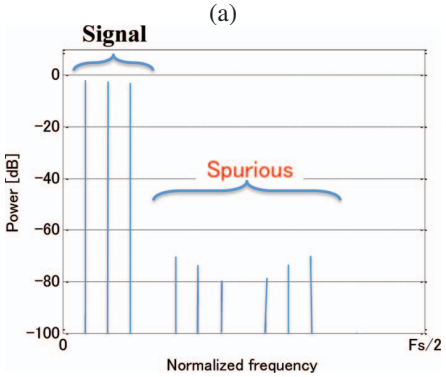


Fig. 13. Cross correlation differences ($|R(0)-R(1)|$) for timing skew detection with 1-tone, 2-tone, 3-tone and 4-tone input signals.



(a)



(b)

Fig. 14. 4-channel interleaved ADC output power spectrum with timing skew for three-tone input. (a) Before compensation. (b) After compensation using method 2.

3) Also compare R(0) values for ADC1 and ADC4, and R(1) for ADC3 and ADC4. Then compensate for the timing skew of ADC4.

According to our simulation, both methods work well, but method 2 is slightly better. Fig.14 (a) shows the output power spectrum of a 4-channel interleaved ADC with timing skew *before* compensation, and Fig.14 (b) shows *after* compensation using method 2; we see that spurious components are suppressed.

D. Non-Binary Search

We show a binary-search algorithm in Fig.3. However a non-binary search algorithm [11], [12] is also possible; this might use more hardware, but is more robust and reliable in the presence of input signal noise.

E. Implementation Issues

We need to investigate FPGA design for skew detection and compensation circuits. We also need to clarify the optimum ADC resolution and optimum minimum time resolution τ for applying our method. Our method requires some digital hardware with high-speed clocks; this might be acceptable in our target application, ATE systems, but might not be acceptable in consumer applications. Furthermore, acceptable compensation convergence time needs to be evaluated in practical applications.

VI. Conclusion

We have proposed a fully digital method of compensation for timing skew effects in a time-interleaved ADC system. We use cross-correlation among channel ADC outputs to detect timing skew, and use successive approximation to adjust our proposed digital delay filters to compensate for timing skew. We have shown that using a multi-tone input signal provides more robust timing skew detection by cross-correlation, and discussed a 4-channel interleaved ADC system as well as a 2-channel system. We have described configuration and operation, and demonstrated the effectiveness of this approach by Matlab simulation. Our proposed method is fully digital and hence it is expected to be stable and reliable.

We consider the followings as our future research:

- Application of our approach to background calibration.
- Extension of our approach to the bandwidth mismatch compensation [1].
- Combination of our method with gain, offset compensation methods.
- Silicon proof of our approach.

We thank Keith Wilkinson for improving the manuscript.

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