A Single Supply Bootsrapped Boost Regulator
for Energy Harvesting Applications

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Abstract A single-supply, low power bootstrapped boost regulator is introduced that can start up with an input voltage of 240mV and achieve a maximum efficiency of 96.9%. The proposed circuit uses a fixed-frequency oscillator to initially start up the circuit and a constant-on-time style hysteretic control scheme in steady-state operation. Hysteretic control helps increase system efficiency compared to using a conventional Pulse-Width-Modulated control scheme. The effectiveness of this approach is shown through Spectre simulation results.

Keywords Energy Harvesting, Boost Regulator, CMOS, Hysteretic Control

1. Introduction

Recently there have been great advances in the realm of Energy Harvesting. Using vibrational, thermal, and solar transducers, small amounts of power can be captured by latent energy sources [1–9]. While previous works have shown that capturing power from these micro-power sources is feasible, each approach has drawbacks. Some approaches require an external battery [1] or a storage capacitor [2] with a voltage of several volts to bias the control circuitry. Others have designed their circuits with external bias circuitry [3] or require a mechanical switch in order to start up the converter [4]. Furthermore, previous works also are not suitable to drive realistic loads, as their maximum load capability is in the μW range [1–6].

In order to address these issues, we have created a single-supply, low-power boost circuit that is only operational when its input source is large enough to bootstrap the system. Our circuit is also optimized to provide several mW of power, which would be suitable to drive a low-power Micro-Controller Unit (MCU). Additionally, our circuit is designed to maximize efficiency, which, in a real-world application, would increase the maximum amount of energy that is available to the load.

2. Proposed Circuit Operation

2.1. Block Diagram

A block diagram of the proposed circuit is shown in Fig. 1. The components L, M_N, M_P and C_O form the core of a basic boost converter. Since the output voltage V_O will be well regulated and larger than the input, it is suitable for supplying power to the internal control circuitry: namely the voltage loop comparator, one shot and voltage reference. In order to initially raise the output voltage

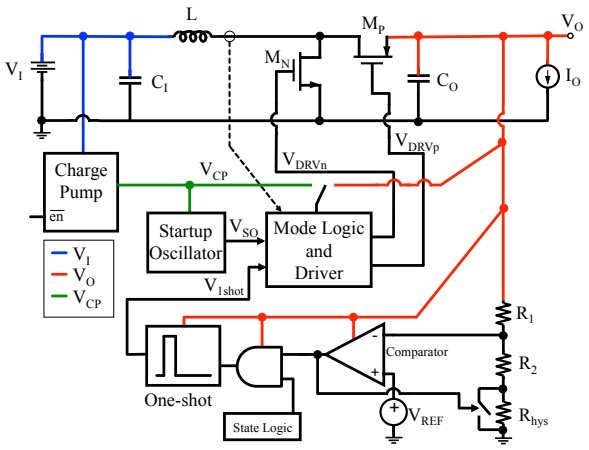


Figure 1: Bootstrapped boost converter block diagram.

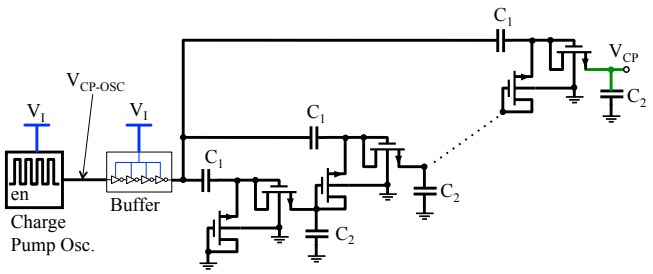


Figure 2: Full charge pump schematic.

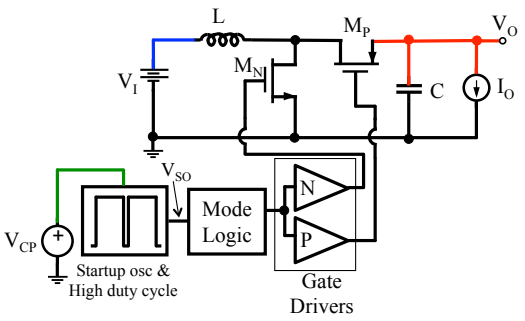


Figure 3: Startup circuitry connected to drivers and output switches.

however, we are using a charge pump circuit that can operate from a very low input voltage. The output of this charge pump is then fed to a fixed-frequency startup oscillator and to the main drivers that commutate the switches and raise the output voltage to bias the internal circuitry. Once the output voltage has reached an acceptable level, the charge pump and startup oscillator are stopped, and the driver power source switches to the output voltage. When this handoff is complete, the circuit begins running in a constant-on-time hysteretic mode. The input voltage V_I, output voltage V_O and charge pump output voltage V_{CP} are highlighted in different colors to help easily understand the voltage domains present in the proposed circuit.

2.2. Startup Charge Pump

The proposed circuit is being designed in a 0.18μm CMOS process that supports NMOS native–V_t (V_t = -0.02V) and low–V_t (V_{tp} = -0.13V, V_{tn} = 0.27V) along with nominal ($V_{tp} = V_{tn}$ = 0.44V) transistors. In order to reduce leakage current however, nominal V_t devices are used as the output drivers and switches. Because the threshold voltage of the nominal devices is greater than 400mV, an on-chip charge pump is used to ensure that the system can operate with V_I less than the switch threshold voltage.

Fig. 2 shows the complete charge pump schematic. A high-frequency ring oscillator is fed through a buffer before connecting to a diode-connected native–V_t NMOS charge pump, similar to the approach in [10]. Unlike the previous work, our system relies on an oscillator signal generated on-chip and is connected to the output switch drivers, which require a large amount of power to operate. Because of these drawbacks, while using a 10 stage design, our charge pump achieves a peak voltage of only 950mV from a 300mV source. In our implementation of this charge pump, all native-V_t NMOS transistors are designed with a size of 40μm/500nm, C_1 capacitors are 5pF metal-metal capacitors and C_2 are 40pF NMOS capacitors.

2.3. Startup Oscillator and Driver

In order to raise the output voltage to an appreciable value to bias the hysteretic control circuitry, a high-duty-cycle oscillator is applied to the gate driver circuitry for the switch transistors, powered by the charge pump described in Section 2.2. Using a ring oscillator running at a frequency of 100kHz, this low-frequency clock is modified to run at a very high duty cycle (83%).

Note that the duty cycle of the converter must be less than 100% to ensure that current from the inductor is transferred to the output capacitor, and hence the output voltage can rise. The schematic of this high-duty-cycle system connected to the drivers and output switches is shown in Fig. 3.

2.4. Voltage Reference

Since the proposed circuit operates with an output voltage around 1.0V which is used to drive the control circuitry, the reference voltage (labelled V_{REF} in Fig. 1) must also run from a very low input voltage. Due to its low input voltage requirement and the ability to create a reference voltage less than a typical 1.2V bandgap, we have modified the Banba bandgap reference described in [11]. In order to save space, we have incorporated an area mismatch of 8x to 1x between the two PNP bipolar junction transistors. This has an added benefit that the transistors can be easily laid out in a 3x3 grid.

Additionally, we have adjusted the reference voltage output to

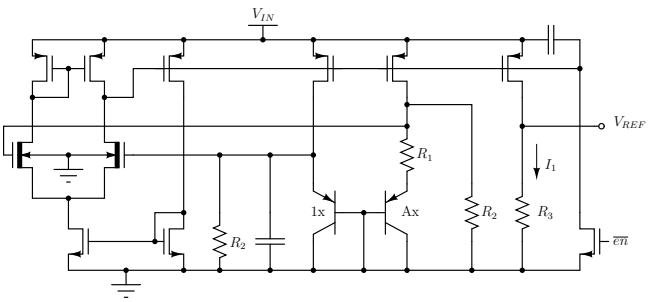


Figure 4: Banba bandgap voltage reference.

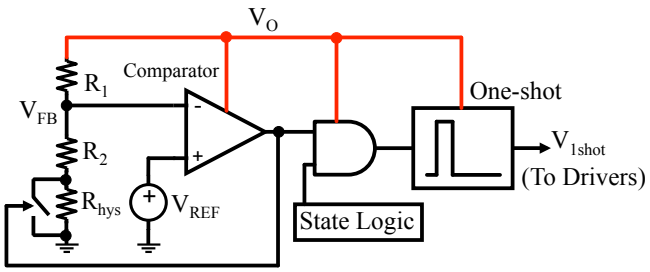


Figure 5: Hysteretic control schematic.

250mV, which is better suited to our application. Due to this change in parameters, the values of the resistors are also changed compared with the previous work, with $R_1 = 180k\Omega$, $R_2 = 2.07M\Omega$ and $R_3 = 371k\Omega$ in the proposed circuit. The full voltage reference schematic is shown in Fig. 4

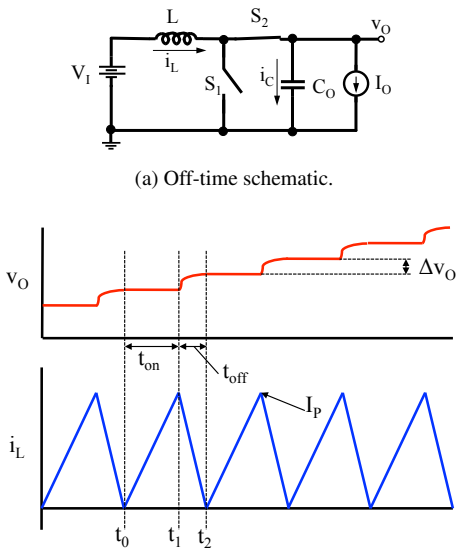
2.5. Hysteretic Control

The main control loop for the proposed circuit is implemented using the constant-on-time control scheme shown in Fig. 5. If the feedback voltage is below the reference voltage, the one-shot circuit will trigger, causing the NMOS switch to turn on for a fixed period of time. At the same time, the switch across R_{hys} will close, effectively setting the voltage threshold to a higher level and adding a predictable amount of positive hysteresis. Once the one-shot times out, the NMOS turns off and the PMOS turns on, until the current through the inductor reaches 0. At this point, the same process repeats until V_O reaches the comparator threshold, at which point the circuit goes into a low-power coasting mode and the R_{hys} switch turns off, returning the circuit to its lower threshold as it waits for the output voltage to fall again.

2.5.1. Output Voltage Ripple

By examining Fig. 6 and assuming the output current I_O is zero, a closed-form expression can be developed for the output voltage ripple, Δv_O. Note that Fig. 6b shows the on-time system while the NMOS and PMOS are commutating ON and OFF, hence here is no "Coasting" time. In the zero-load condition, the output voltage of the constant on-time regulator only increases when the inductor is discharging, and hence, transferring its energy to the output capacitor. During this time (t_1 to t_2), switch S_1 is OFF while S_2 is ON as shown in Fig. 6a.

During t_{off}, when the current from the inductor flows to the output capacitor and load, the output voltage will increase for each cycle. Assuming the load current, I_O is zero, This change in output voltage, Δv_O, can be derived as shown in (1).



(a) Off-time schematic.

(b) Switching inductor current and output voltage.

Figure 6: Constant on-time voltage ripple analysis.

$$\begin{aligned}\Delta v_O &= \frac{1}{C_O}\int_{t_1}^{t_2}\left[I_P - \frac{V_O - V_I}{L}(t - t_1)\right]\mathrm{d}t \\ &= \frac{I_P^2 L}{2C_O(V_O - V_I)} \end{aligned} \quad (1)$$

Using the relation that I_P=V_I t_{on}/L, (1) can be simplified to the more readable expression shown in (2).

$$\Delta v_O = t_{on}^2 \frac{V_I^2}{2LC_O(V_O - V_I)} \quad (2)$$

2.5.2. Maximum Load Current

Using the superposition principle, the output voltage ripple including effects from the load current I_O can be written as:

$$\Delta v_O = t_{on}^2 \frac{V_I^2}{2LC_O(V_O - V_I)} - \frac{I_O\,(t_{on} + t_{off})}{C_O}. \quad (3)$$

And since the output voltage ripple will be zero at the maximum output current (i.e. the output voltage cannot increase), the maximum load is as shown in (4).

$$I_{O(max)} = t_{on}\frac{V_I^2}{2LV_O}. \quad (4)$$

3. Simulation Results

3.1. Simulation Schematic

Simulations have been performed on the circuit shown in Fig. 7, with an on-time during hysteretic mode of t_{on} = 1.5μs and the NMOS and PMOS switches sized at 5mm / 0.18μm and 10mm / 0.18μm, respectively. Since circuit parasitics have a large effect on

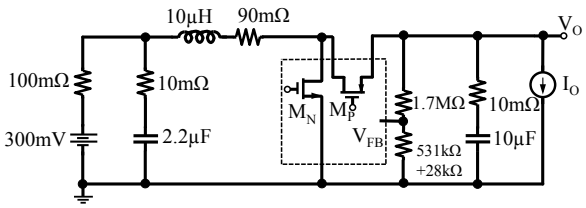
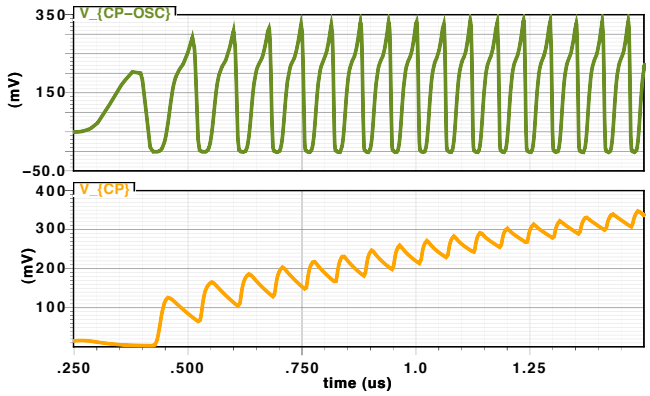


Figure 7: Simulation schematic.

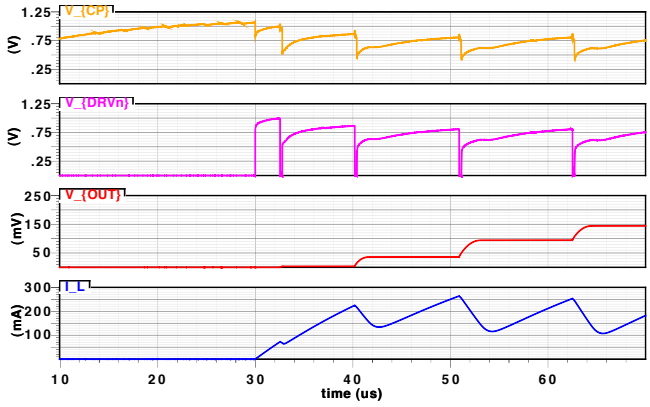
the operation of a boost regulator, parasitic resistances have been included wherever possible. Note that the dashed box in the middle of Fig. 7 shows the internal (transistor-level) circuitry, while everything outside this box is an external component. All internal schematics are transistor-level circuits with no ideal components.

3.2. Startup Results

The initial startup of the regulator, using the charge pump circuitry and oscillator described in Sec. 2.2 is shown in Fig. 8. Once the charge pump oscillator starts switching, the output of the charge pump gradually rises (Fig. 8a). Once the charge pump output is large enough to run the startup oscillator and drivers, the main switches start commutating, and the output voltage V_O slowly rises as shown in Fig. 8b. Once V_O has risen to the reference point, the constant-on time controller takes over.



(a) Initial V_{CP} startup.



(b) V_{CP} driving switch transistors.

Figure 8: Charge pump startup simulation.

3.3. Steady State Operation

Fig. 9 shows the steady-state operation of the proposed circuit. Starting from the far left of the figure, both switches are off and the output voltage is slowly coasting downward, with a slope determined by the output load current. During the coast time however, the hysteretic comparator is still watching V_O, and as soon as it reaches the lower threshold of the comparator, the constant-on time control is enabled. Until the comparator reaches its upper threshold, the circuit turns on the NMOS (and hence charges the inductor) for a fixed amount of time, then turns off the NMOS (and hence turns on the PMOS) until the inductor current reaches 0. When the upper threshold of the comparator is finally reached, both switches are turned off and the circuit re-enters the coasting mode, as was previously shown in the state diagram of Fig. **??**.

3.4. Efficiency

The total end-to-end efficiency of the proposed circuit is shown in Fig. 10. While the efficiency drops off slightly at lower load, it remains above 95% for most of the load range, reaching a maximum of 97% at a load of 6.2mW. The high efficiency in the proposed circuit is a virtue of the fact that switching losses are very low, and the control circuitry consumes very little quiescent current. Note that this data comes from simulation results, and the efficiency values for an actual circuit will likely be lower, due to various parasitic components that are difficult to model in simulation. A comparison between our peak efficiency and maximum load with recently published papers in the field of energy harvesting is shown in Fig 11.

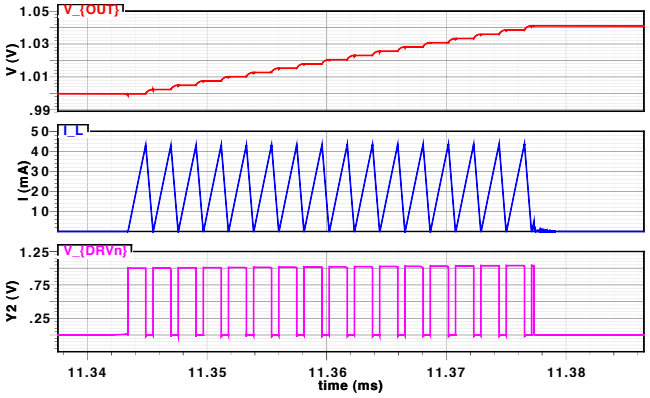


Figure 9: Steady state operation simulation.

4. Test Chip

A test chip comprising all the components of the charge pump startup circuit (i.e. those shown in Fig. 2) were taped out in a 0.18μ process from TSMC. A photomicrograph of the test chip is shown in Fig. 12.

4.1. Lab Setup

Using the lab setup shown in Fig. 13, bench measurements were performed with the part in a QFP64 package, mounted on a breakout board.

As expected, with an input voltage of 330mV, the charge pump oscillator switches between 0V and 330mV. Including the effect of loading the buffer with a large capacitance oscilloscope probe (as described above), the circuit operates at a frequency of about 30MHz in this condition. The shape of the switching waveform and the operating frequency are similar to what was predicted in the simulation shown in Fig 8a.

4.2. Charge Pump Transfer Function

In order to test the real-world performance of the charge pump, the chip was tested both with no load and with a 100kΩ resistive load. Results from these experiments are shown in Fig. 14.

As expected, with no load there is a decent amount of gain, and the output voltage rises to almost 2V with an input voltage of 340mV, corresponding to a gain of about 6 V/V. With a resistive load however, the output voltage rises slower for a given input voltage, but it still seems that the output voltage would rise high enough to start switching the part.

4.3. Bench and Simulation Comparison

Disregarding loading, the shape of the ring oscillator signal in the test chip is the same as the simulated result, shown previously in Fig. 8a. The frequency of the oscillator is different from the simulated value, but this can be explained by two different phenomena. First, capacitive loading of the driver output will cause the oscillator to run slower. Second, the ring oscillator architecture of the circuit is very sensitive to the input voltage and the threshold voltage of the transistors—any small variation from the simulated values will have a large effect on the actual oscillation frequency.

In the actual application, this charge pump output would be applied to an oscillator and the main switch drivers, as shown previously in Fig. 3. Unfortunately it is difficult to model this condition without the actual circuit that the charge pump would be powering. But data from this test chip shows that the charge pump oscillator functions, and that the diode-connected native-NMOS charge pump stages can work together to create a high enough output voltage to startup the circuit.

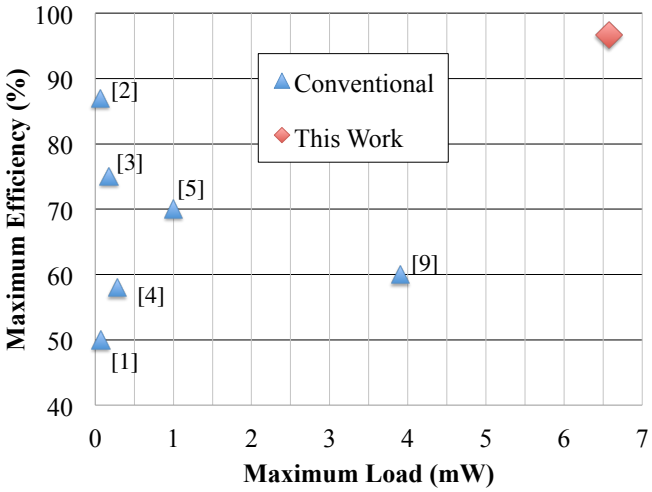


Figure 11: Comparison of maximum efficiency and output power with cited papers.

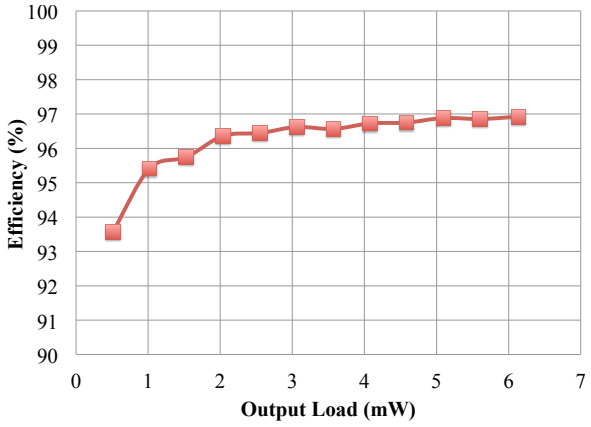


Figure 10: Efficiency over load range.

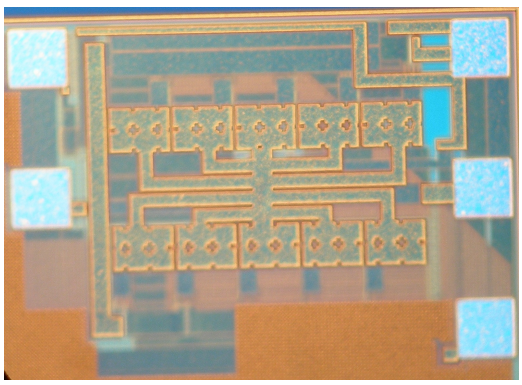


Figure 12: Charge pump test chip.

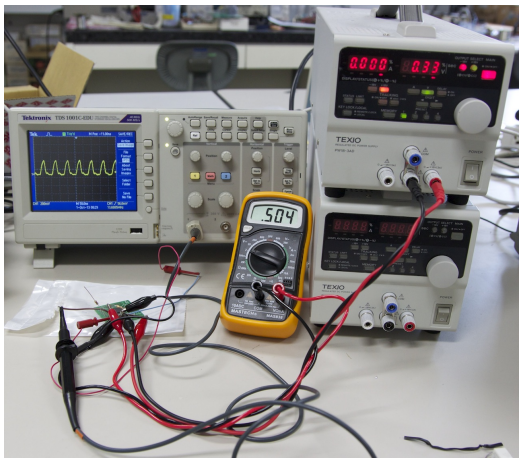


Figure 13: Charge pump lab setup.

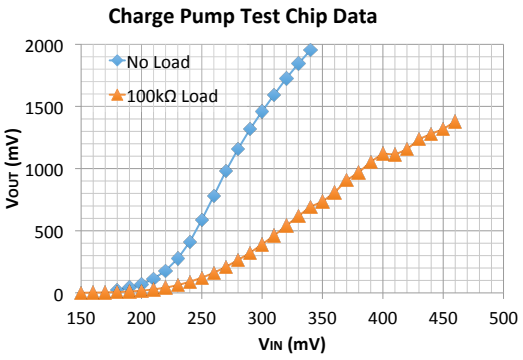


Figure 14: Test chip transfer function with and without load.

5. Conclusion

We have introduced a low-power boost regulator that is optimized for energy harvesting applications. While previously presented papers have shown that it is possible to convert energy from extremely low-power input sources, these papers have not designed their circuits to work with a realistic load nor to maximize the system efficiency. Compared to previously presented approaches, our circuit can handle enough output load to power a typical microcontroller system, while maximizing the end-to-end efficiency over the entire load range. Finally, the circuit we have introduced accomplishes all of this while only requiring three external components: an input capacitor, an output capacitor, and an inductor.

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