Noise-Shaping Cyclic ADC Architecture

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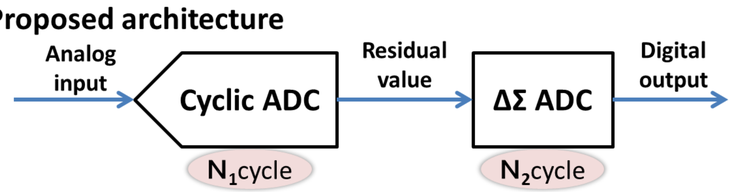
Research Background

Real world signals are analog
ADCs are essential for digital signal processing

Research Objective

Good trade-off among speed, precision and power with simple circuitry

Proposed architecture



Pipelined cyclic ADC and ΔΣ ADC

Cyclic ADC Problem

- Low noise for MSB (high power)
- The same circuit is used for latter stages

Not effective for power and chip area

Configuration of Noise-Shaping Cyclic ADC

ΔΣ ADC accumulates quantization error of cyclic ADC

ΔΣ ADC
- Low power
- Fast operation

Cyclic ADC Operation

- Medium power
- Medium operation

Residue voltage Vout (n) of nth-stage

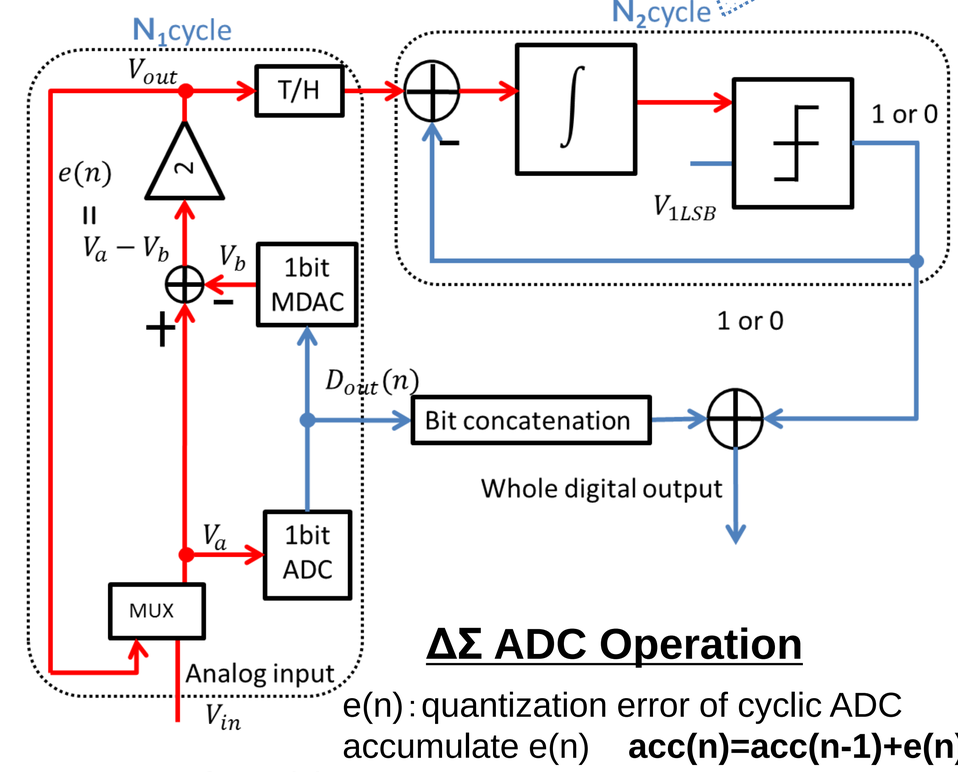
Vout(n) = 2^n × (Vin - K(n) × Vref)

Digital output

K(n) = (1/2)Dout(1)+(1/4)Dout(2)
+(1/8)Dout(3)+⋯+(1/2^n)Dout(n)

where **Dout(n)=1 (Va(n) ≥ Vref/2)**

Dout(n)=0 (Va(n) < Vref/2)

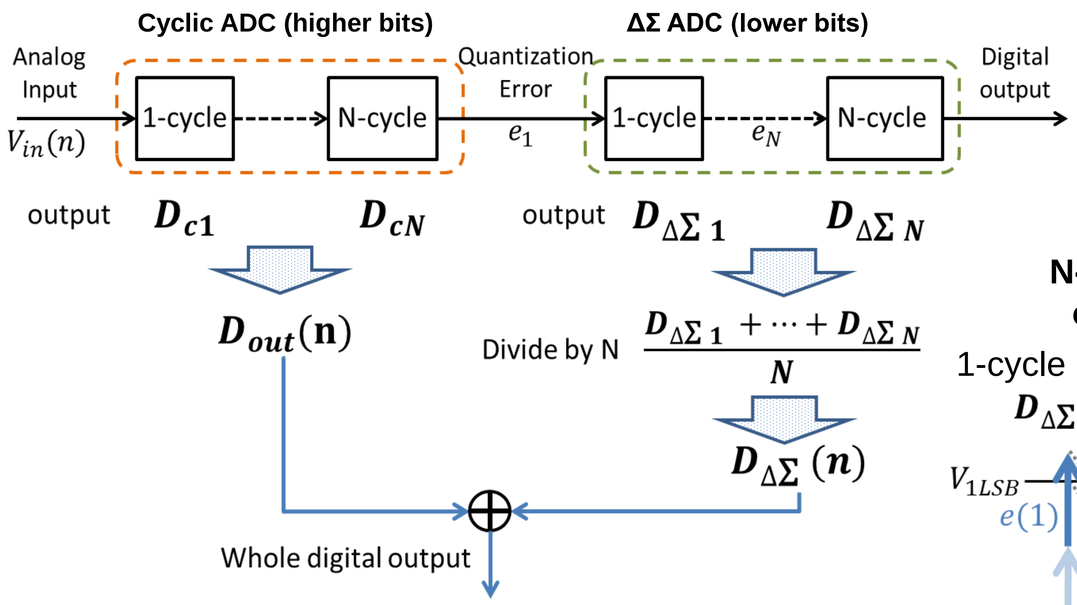


ΔΣ ADC Operation

e(n) : quantization error of cyclic ADC
accumulate e(n) **acc(n)=acc(n-1)+e(n)**

If acc(n) > V_{1LSB}
acc(n) ⇒ acc(n) – V_{1LSB} , Dout (n) ⇒Dout (n)+1

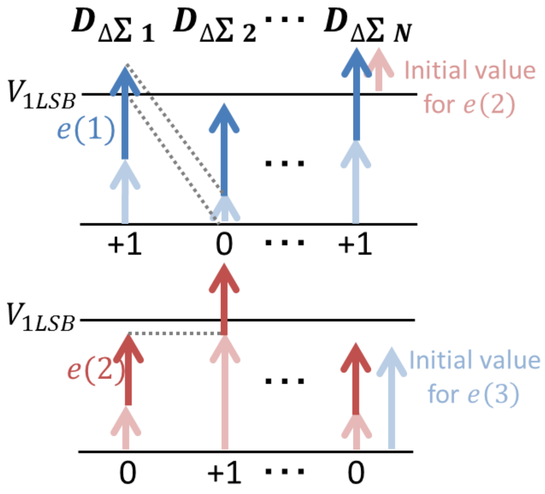
ΔΣ ADC Multiple-Cycle Algorithm



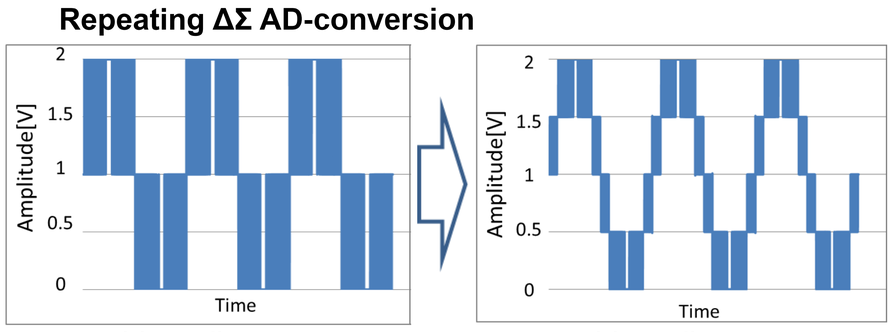
N-time comparison of e(n) and V_{1LSB}

1-cycle 2-cycle ⋯ N-cycle

$D_{\Delta\Sigma 1}$ $D_{\Delta\Sigma 2}$ ⋯ $D_{\Delta\Sigma N}$



Repeating ΔΣ AD-conversion



1bit-cyclic ADC + 1-cycle ΔΣ ADC

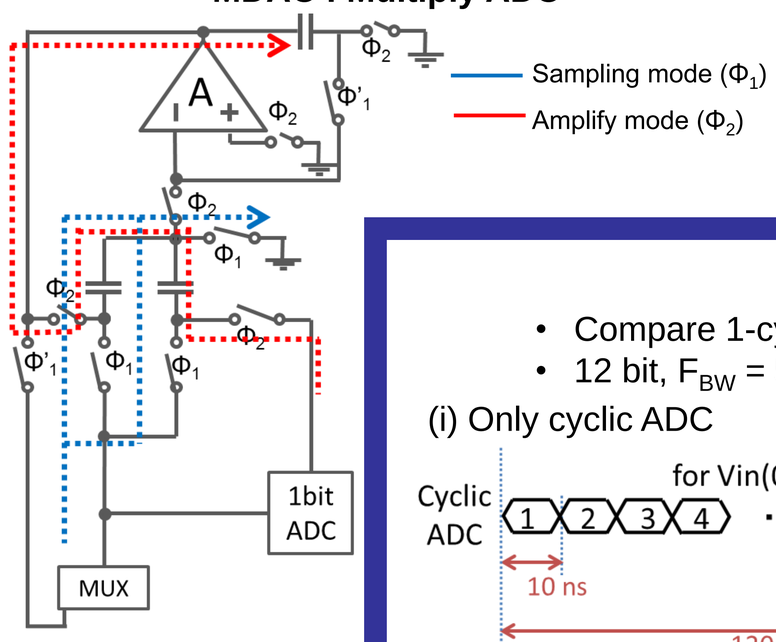
1bit-cyclic ADC + 2-cycle ΔΣ ADC

Resolution Increase

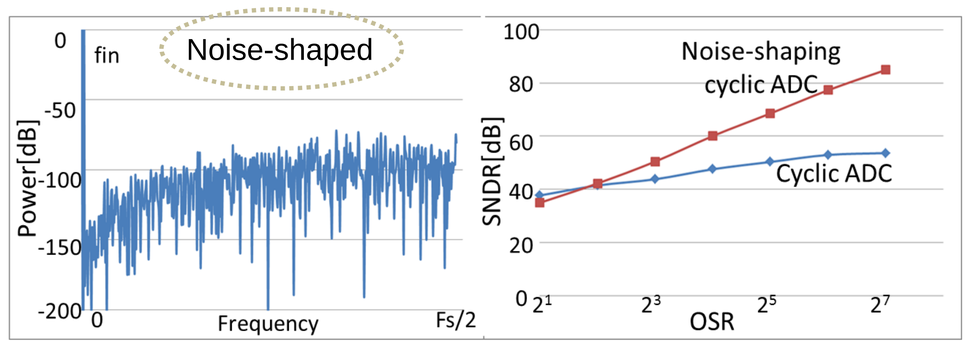
- MDAC is slow, power hungry
  → for higher bits
- ΔΣ ADC is fast, low-power, not very linear
  → for lower bits
  → Higher clock frequency

Pipelined cyclic ADC and ΔΣ ADC
→ High resolution,
Medium speed, Low power

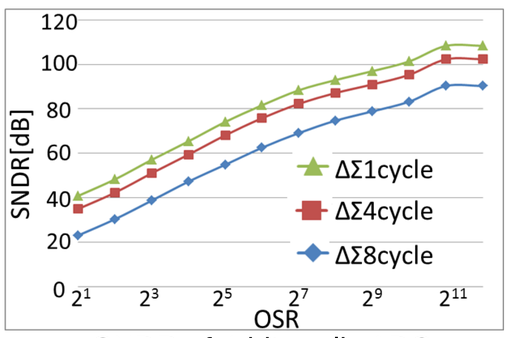
MDAC : Multiply ADC



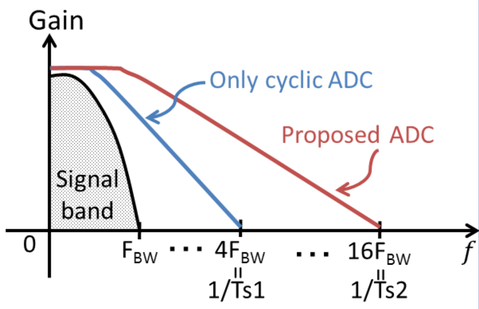
MATLAB Simulation



Power spectrum of noise-shaping cyclic ADC



SNDR of 4-bit cyclic ADC, multiple ΔΣADC



Relaxed anti-alias analog filter

SNDR, ENOB improve

Noise shaping cyclic ADC ΔΣADC multiple operation

N_1-cycle Cyclic ADC, N_2-cycle ΔΣADC ($N_2=2^{M2}$)

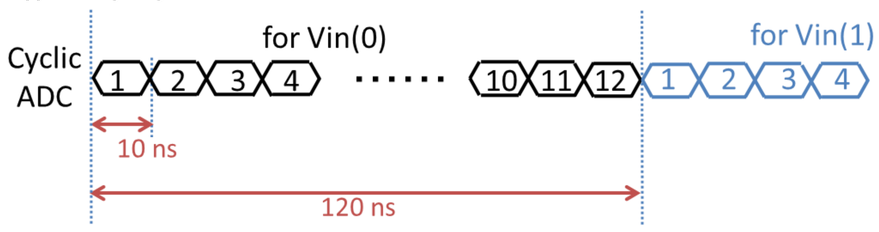
SNDR=6 × (N_1+M_2)+2+9 × OSR [dB]

ENOB=(N_1+M_2)+1.5 × OSR [bits]

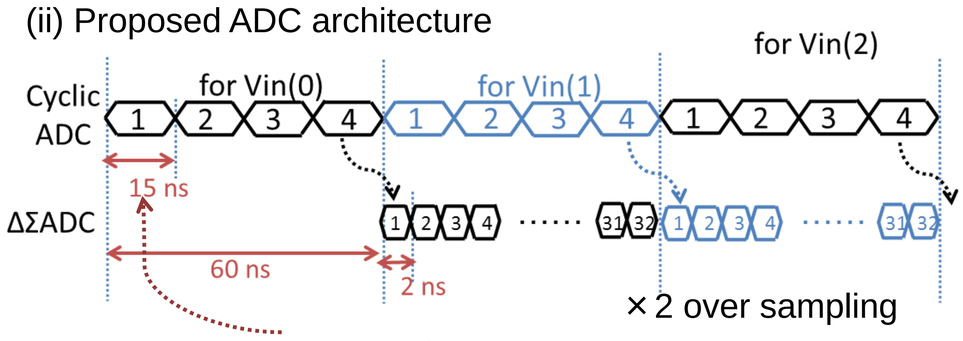
Positioning of proposed ADC

- Compare 1-cycle cyclic ADC operation time
- 12 bit, F_{BW} = 500 kHz, OSR=4, $F_s/(2F_{bw})$=OSR

(i) Only cyclic ADC



(ii) Proposed ADC architecture



× 2 over sampling

× 1.5 MDAC settling time

Proposed ADC

- MDAC settling time
  → 1.5 times longer
- × 2 oversampling
  →Noise performance reduction
  →Relaxed anti-alias analog filter

Small overhead of continuous-time ΔΣADC

Power Reduction

Conclusion

ADC architecture proposal

- Pipeline of cyclic ADC and ΔΣ ADC.
- Noise-shaping of cyclic ADC quantization error by ΔΣ ADC
- High resolution, medium speed, low power
  →Power, chip area efficient
- Reconfigurable for different combinations of speed, precision, and power