Delta-Sigma Digital-to-Time Converter and its Application to SSCG

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Abstract This paper proposes an innovative method of converting digital signal to time-domain analog signal, which fully enjoys robustness and digital circuit friendliness. This technique utilizes a digital delta-sigma ($\Delta\Sigma$) modulator following a digital-to-time converter (DTC) circuit with various modulation methods. As an application of the proposed method, novel spread-spectrum clock generation (SSCG) algorithms (such as for DC-DC converters) have been investigated which can select the noise spectrum spread bands; e.g., they can exclude the noise spectrum spread in AM, FM radio bands. The proposed circuit takes advantage of digital technology, which is simple, fast (reachable at high clock frequency) and flexible (programmable).

Keywords Digital-to-Time Converter, $\Delta\Sigma$, Spread Spectrum Clock Generation, Time-Domain, EMI, Band Selection

1. Introduction

Constant miniaturization, speeding up and rising frequency of semiconductor devices in recent years have accelerated usage and application of oversampling methods [1]. The delta-sigma method opens up broad range of analyzing signal in the time domain possibility. Handling signal processing in time domain, does not just enhance processing signal in fully digitized circuit which has been the trend in recent years [2]. Benefits of signal processing in time domain has caught so many eyes in recent years and lead to many new fields opening like: Time to Digital Converter (TDC) which is time-domain equivalent of delta-sigma digital-to-analog converters (Fig. 1a).

This paper proposes a simple method of converting the digital signal to the timing signal, which is basically DAC correspondent in time domain; this technique utilizes a digital delta-sigma ($\Delta\Sigma$) modulator following a DTC circuit with various modulation methods. As an application of the proposed method, novel spread-spectrum clock generation (SSCG) algorithms (such as for DC-DC converters) have been investigated which can select the noise spectrum spread bands; e.g., they can exclude the noise spectrum spread e.g., in AM, FM radio bands (Fig.2). This can be used as an EMI reduction technique [3]-[10].

In section 2, we explain the concept and theory of the proposed delta-sigma DTC. In section 3, we present applications of the proposed DTC to SSCG for EMI reduction. The proposed method can be implemented fully digital circuit and select the noise spectrum spread bands, which could be called as a second generation SSCG. We show several modulation methods with their simulation results. Section 4 provides conclusion.

2. Principle of $\Delta\Sigma$DTC

2.1. Fundamental Theory

Traditionally, information has been processed and encoded in the voltage domain; however, more recently information encoding in time domain has considerably gained popularity. Data conversion in theory is simply the process of working with signals in different domains. The DTC is a converter device which maps a digital value to a timing signal.

Basic distinction between DTC and DAC is the domains where they function; the DTC operates in time domain, whereas the DAC operates in voltage domain. The process of converting signal from digital to analog (or vice versa) usually involves many techniques including filtering and smoothing of the signal before and after the conversion. In this regard, our proposed DTC is in full compliance with its conventional methods. The DTC includes a digital $\Delta\Sigma$ converter (Fig. 3); here, samples are interpolated with an analog low pass filter (LPF). In time domain, a LPF is used to smooth the

signal by cutting high frequency components.

The delta-sigma DTC idea is - to our knowkedge- only used for very recent work [11] which employs DTC driven phase signal conversion for automatic test equipment (ATE) applications. This work differs in two main points from it; First, our proposed methods apply pulse cycle and width modulation with some innovative ways in addition to phase modulation, and also utilize an asynchronous counter to perform as a low pass filter in time domain which - due to its digital nature - is very simple compared to PLL.

Now we introduce timing pulse definition. An electric pulse wave is a periodic square waveform which alternates at a steady frequency between two fixed points. Thus the pulse frequency, position and width are the fundamental characteristics which define a pulse. We will deal with all these three elements to form our DTC signal. T, ϕ, τ_p in Fig. 4 are index names for the pulse cycle period (or reciprocal of frequency), position (or phase) and width, respectively.

2.2. PCM$\Delta\Sigma$DTC

We consider Pulse Cycle Modulation (PCM), which is a manipulation of representing each timing signal pulse cycle (Figs. 5, 6). For example, digital "0" is mapped to a time signal with cyclic period of T while "1" is with 2T; then in case of digital inputs sequence D=10110, the output signal is shown in Fig. 5. Block diagram of the $\Delta\Sigma$ PCM DTC is illustrated in Fig. 6. Because of unlimited variable periods which we can choose from frequency, PCMDTC could be superior to other following methods in regard to multi-bit modulation.

2.3. PPM$\Delta\Sigma$DTC

Pulse Position Modulation (PPM) $\Delta\Sigma$ DTC encodes each digital signal value by shifting output pulse signal beginning position Figs. 7, 8). So for instance, if we have output pulse with the frequency of f, digital "0" is mapped to pulse with zero shifting position ($phase = 0$), and digital "1" is mapped to pulse with shifting position of a constant C (where $C \leq T$). A sample modulation of digital value similar to PCMDTC (10110) is shown in Fig. 7.

Two major differences and benefits of PPMDTC compared to the previous method are as follows: First, output signal length is independent of numbers of "0"'s and "1"'s. Second, it consists of only a delay element and an digital multiplexer (Fig. 8). This circuit capability of handling high-frequency signal in digital circuit might be game changer factor to choose it over other methods in applications.

2.4. PWM$\Delta\Sigma$DTC

Pulse Width Modulation (PWM) DTC changes the output signal width based on digital input value (Figs. 9, 10). It implementation may be a little bit complex, but but its benefits surface up when it is used in conjuncture with other methods, which we will discuss later in this section.

2.5. PRJ$\Delta\Sigma$DTC

Pseudo Random Jitter (PRJ) DTC is very similar to pulse cycle modulator (PCM), because, like PCM, the major distinction between two timing output signals for two distinct digital inputs are pulse frequency (cycle period). However in PRJ, output signal frequency changes arbitrarily between two (or more for multi-bit DTCs) constant values 12. This technique can be achieved by randomly delaying output signal so that it looks like a big jitter in output pulse. Fig. 11 shows a sample output of PRJ DTC for a digital input sequence of 10110.

2.6. Compound Methods

We can extend our proposed DTC methods by combining of PCM, PPM, PWM or randomly changing any of three main characteristic(cycle, position and width) for more effective SSCGs.

3. Spread Spectrum Techniques

3.1. Spread Spectrum Technique Introduction

One of the biggest obstacles in miniaturization, higher operating frequency and packaging all system in a single chip, arguably is Electro-Magnetic Interference (EMI) [9]. EMI does not just degrade or limit the effective performance of the circuit, but also it hardens manufacturers struggle to keep up with law and regulations enforced by different countries (like FCC).

It is well-known that, during system development, critical signal-integrity and EMI simulations are difficult, time-consuming, and error-prone due to their reliance on hard-to-predict models and parameter extractions. Fig. 13 shows noise spectrum power of a typical digital system; noise spectrum peaks appear in base band and they are harmonic frequencies. Constant frequency intervals are due to the system clock, in fact, EMI main source in digital circuits is clock signal. Although limitation of interfering signal power in higher frequency ($\geq$230MHz) is slightly looser (Fig.14), it is becoming constantly harder to contain those circuits below the threshold without significant shielding, which results in adding to circuit size.

3.2. Spread Spectrum Clock Generator

Spreading spectrum techniques of the clock signal have been widely used for EMI reduction in digital processor and DC-DC converter areas. Their conventional methods use frequency-modulating the system clock with a low-frequency signal as well as other modulation schemes. This approach creates frequency spectrum with sideband harmonics. Intentionally broad-banding the narrow-band repetitive system clock simultaneously reduces the peak spectral energy in both the fundamental and the harmonic frequencies. If the clock frequency spreads widely, the peak power is reduced and EMI problem is suppressed. However, in many applications some signal bands (such as AM, FM radio frequency bands) are important and it is not desirable for the spread clock frequency components enter into the bands.

We present here that SSCGs with our proposed delta-sigma DTC methods can adjust emission bands and excluding (or surpassing) noise emission in specific bands.

4. Simulation Results

Effectiveness of the proposed delta-sigma DTC methods applied to SSCG has been verified by numerical simulation.

4.1. SSCG Simulation Methodology

Sine wave with frequency of f_s/N, sampled in N points with sampling frequency f_s is fed to DTC as digital input. After being noise-shaped by a first-order delta-sigma converter, output has been digital-to-time modulated according to the relevant method. Original clock (without sigma-delta DTC modulation) signal base peak power and its harmonics reach to 66dB (Fig. 15).

4.2. SSCG using PCM$\Delta\Sigma$DTC

Spread spectrum with PCM DTC suppresses spectrum peak significantly and also creates notches at some locations. The power spectrum of previously introduced signal by various DTC has been presented in Fig. 16, where we derive that notch locations are given by eq.(1). Here we assume that periods T_H and T_L corresponding to digital signals "1" and "0" are integer (n_H, n_L) multiples of constant minimum base period (T_C), respectively.

$$f_{notch} = \frac{K \times (n_H + n_L)}{2|n_H - n_L|} f_s \tag{1}$$

where: $K = |n_H - n_L| - 1, |n_H - n_L| - 2, \cdots, 1.$
n_H and n_L are positive integers,
defined as $n_H = T_H/T_C$, $n_L = T_L/T_C$.

4.3. SSCG using PPM$\Delta\Sigma$DTC

Spread spectrum power of the PPM DTC method is illustrated in Fig. 17. If we assume that each pulse period (T_H, T_L) is integer (n_H, n_L) multiple of base period T_C and each pulse phase (ϕ_H, ϕ_L corresponding to digital signals "1", "0" respectively) are integer (q_H, q_L) multiples of constant minimum base period (T_C), then we observe that PPM DTC has capability to lower noise in particular bandwidth given by eq.(2), although PPM DTC influence on signals peaks may not be sufficient.

$$f_{notch} = \frac{K}{|q_H - q_L|} f_s \tag{2}$$

where $K = |q_H - q_L| - 1, |q_H - q_L| - 2, \cdots, 1.$
q_H and q_H are positive integers,
defined as $q_H = n_H(\phi_H/2\pi), \quad q_L = n_L(\phi_L/2\pi).$

4.4. SSCG using PWM$\Delta\Sigma$DTC results

Fig. 18 shows the demonstration of PWM method; in the same manner as PPM DTC, PWM may not have any notable performance on peak reduction, but it creates deep notches in certain bands pretty well, whose locations are given by eq.(3).

$$f_{notch} = \frac{K}{|m_H - m_L|} f_s \tag{3}$$

where $K = |m_H - m_L| - 1, |m_H - m_L| - 2, \cdots, 1.$
m_H and m_L are positive integers,
defined as $m_H = \frac{\tau_H}{T_C}, \quad m_L = \frac{\tau_L}{T_C}.$

4.5. SSCG using PRJ$\Delta\Sigma$DTC

Finally, Fig. 19 illustrates sample signal of generated/modulated PRJDTC. We observe that this method is very effective in lowering system signals peaks and yields notch if carefully designed. Set the pulse period corresponding to digital "0" to be T_L which is integer (n_L) multiples of constant minimum base period (T_C), and also design so that the pulse period corresponding to digital value "1" arbitrarily alters between T_{H1} and T_{H2}, which are integers (n_{H1} , n_{H2}) multiples of T_C. Then we found that the notch frequency locations are determined by eq.(4).

$$f_{notch} \simeq K(\frac{4n_L + p + q}{4G}) f_s \tag{4}$$

where $K = G - 1, G - 2, \cdots, 1.$
Here G is the greatest common divisor between p and q
and $p = |n_{H1} - n_L|, q = |n_{H2} - n_L|.$

For the matter of completeness in Fig. 20 a compound method of PWMDTC + PRJDTC is shown. We notice the affect of PWM DTC in hammering signal high in side bands of the notches in Fig. 20a.

5. Conclusion

We have introduced and demonstrated proposed delta-sigma DTC methods which bring digital signal to timing signal. These methods are fully implementable only using digital circuitry with suitability for higher frequency circuits application. Their effectiveness and expected results have been verified by computational simulations.We have also applied our proposed methods to easy and yet practical spectrum spread clock generator. We expect that our proposed DTC methods will find a lot of other applications in addition to SSCG.

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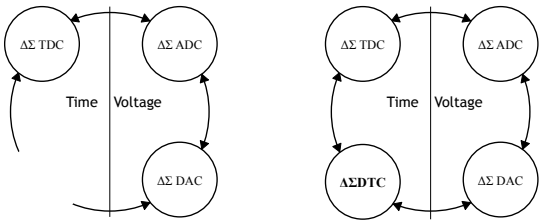


(a) (b)

Figure 1: $\Delta\Sigma$ converters in time and voltage domains, and positioning of $\Delta\Sigma$ DTC.

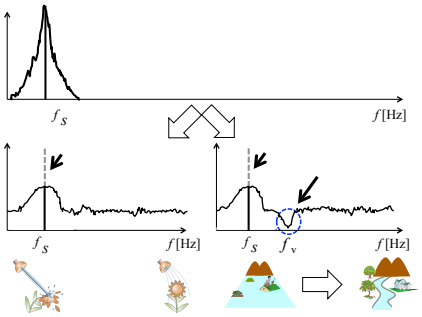
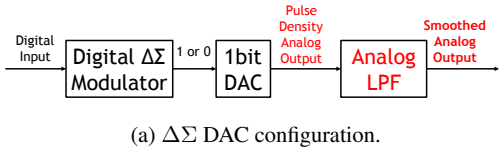
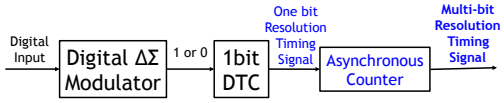


Figure 2: Spread spectrum technique.



(a) $\Delta\Sigma$ DAC configuration.



(b) $\Delta\Sigma$ DTC configuration.

Figure 3: $\Delta\Sigma DAC$ and $\Delta\Sigma$ DTC analogy.

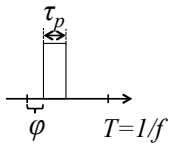
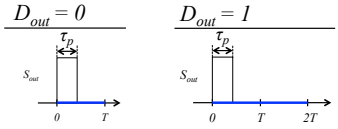
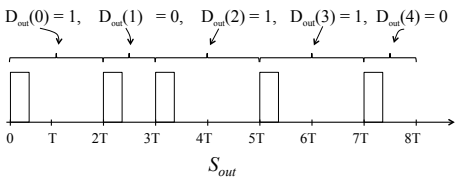


Figure 4: Pulse model used for $\Delta\Sigma$ DTC modulation.

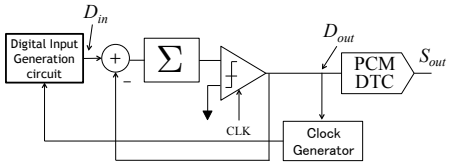


(a) Time signal representation for digital "1" & "0".

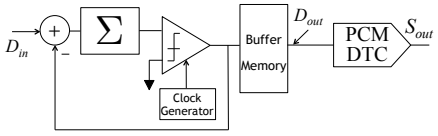


(b) Time signal of 10110 by represented by above time signals.

Figure 5: PCMDTC Example

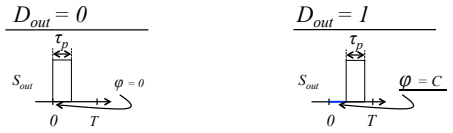


(a) PCM (ΔΣ) DTC block diagram.

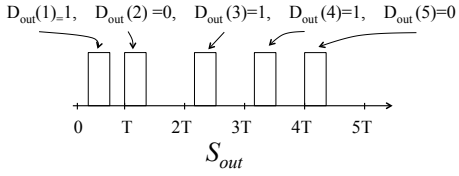


(b) Alternative PCM (ΔΣ) DTC block diagram.

Figure 6: PCMDTC circuit block diagram.



(a) Time signal representation for digital “1" & “0".



(b) Time signal of 10110 represented by the above time signals.

Figure 7: PPMDTC example.

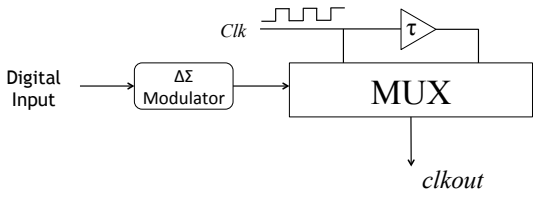
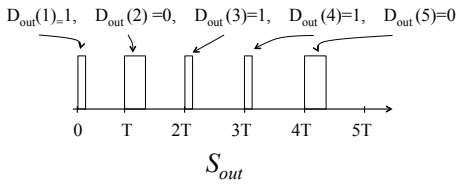


Figure 8: PPMDTC circuit block diagram.

(a) Time signal representation for digital “1" and “0".



(b) Time signal of 10110 represented by the above time signals.

Figure 9: PWMDTC example

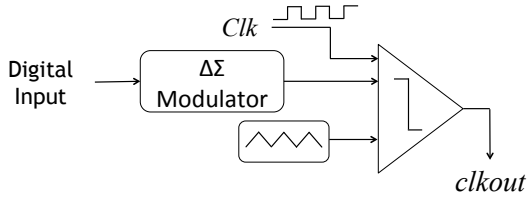
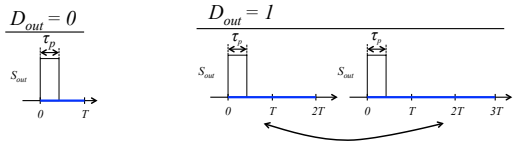
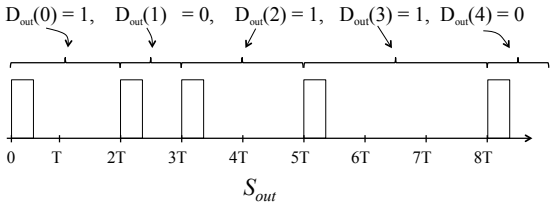


Figure 10: PWMDTC circuit block diagram.



(a) Time signal representation for digital “high" and “low".



(b) Time signal of 10110 represented by the above time signals.

Figure 11: PRJDTC example.

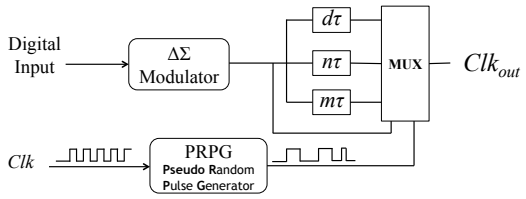


Figure 12: PRJDTC circuit block diagram.

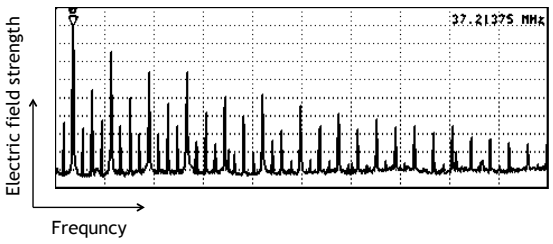


Figure 13: Typical Digital System EMI Noise Spectrum

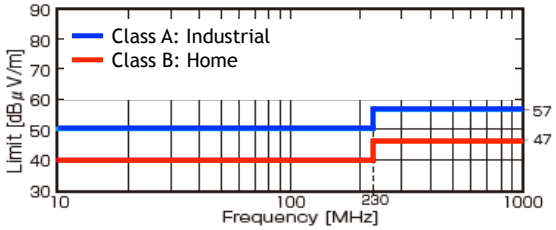


Figure 14: EMI power regulation.

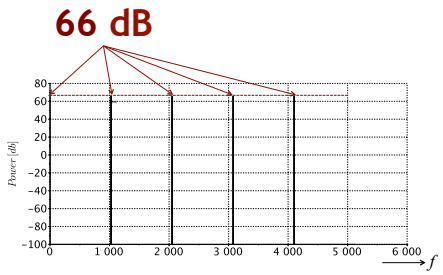
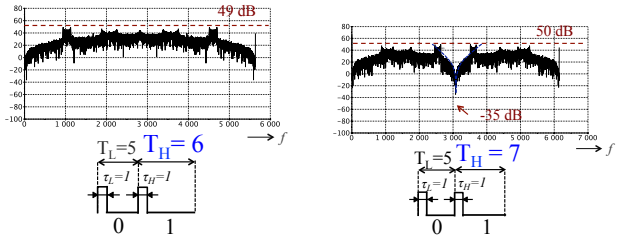
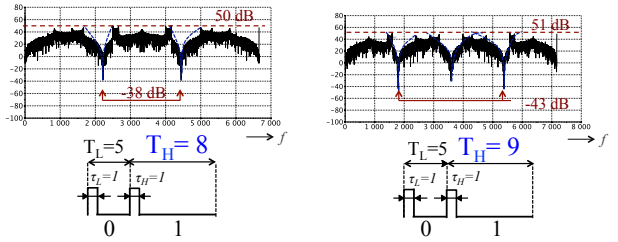


Figure 15: Base peak power without DTC modulation.

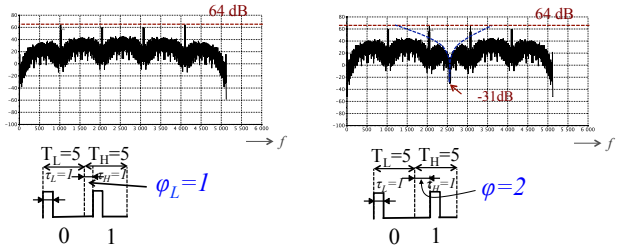


(a) $T_H = 6$ (b) $T_H = 7$

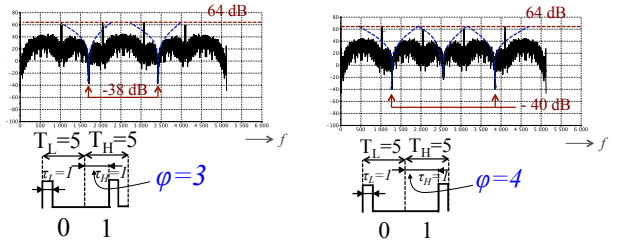


(c) $T_H = 8$ (d) $T_H = 9$

Figure 16: Spreading clock power spectrum by various PCMDTCs.

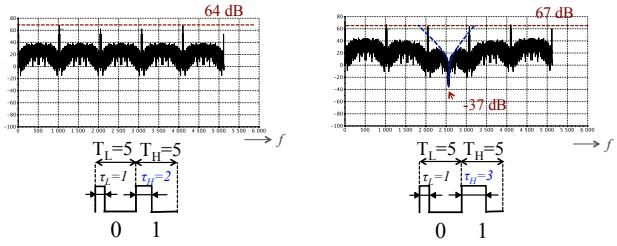


(a) $q_H = 1$ (b) $q_H = 2$

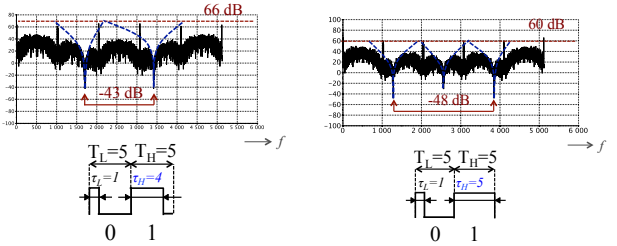


(c) $q_H = 3$ (d) $q_H = 4$

Figure 17: Spreading clock power spectrum by various PPMDTCs.

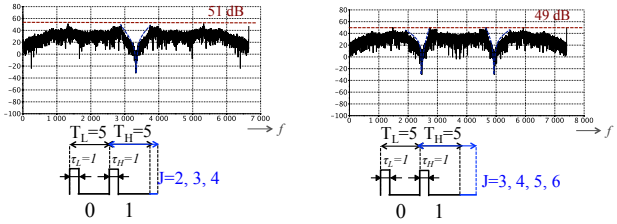


(a) $\tau_H = 2$ (b) $\tau_H = 3$

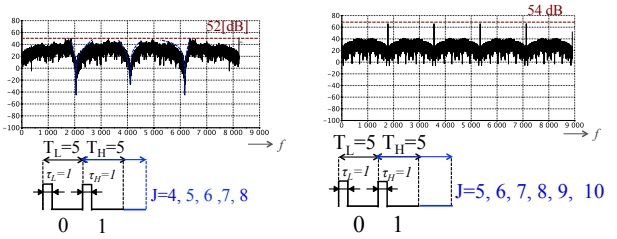


(c) $\tau_H = 4$ (d) $\tau_H = 5$

Figure 18: Spreading clock power spectrum by various PWMDTCs.

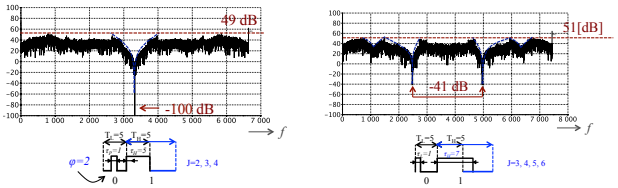


(a) $J = 2, 4$ (b) $J = 3, 6$



(c) $J = 4, 8$ (d) $J = 5, 10$

Figure 19: Spreading clock power spectrum by various PRJDTCs.



(a) $J = 2, 4$ **&** $\tau_H = 5$ (b) $J = 3, 6$ **&** $\tau_H = 7$

Figure 20: Spreading clock power spectrum by PRJWMDTCs.