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A low-offset cascaded time amplifier with reconfigurable inter-stage connection

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Abstract: This study demonstrates the design and testing of a reconfigurable cascaded time amplifier (TA) that enables a reduction in the output offset. By testing the polarity of the output offset time caused by process variations in each stage and then reconfiguring the inter-stage connections, we find that the total output offset time can be reduced dramatically. The results of a SPICE simulation of a 65-nm CMOS match well with the theoretical estimates and show the effectiveness of this proposed testing structure and reconfigurable inter-stage connection technique.

Keywords: time amplifier, jitter measurement, design for testability, BIST

Classification: Integrated circuits

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1 Introduction

As jitter in clock sources, such as all-digital phase-locked loops (ADPLL) is reduced to the order of several hundreds of femtoseconds [1, 2], it becomes critically important to develop methods for high-resolution on-chip jitter measurement [3, 4] in order to evaluate performance. However, no known on-chip jitter measurement strategy meets all necessary requirements, although some improvement in the resolution of on-chip jitter measurement has been reported through the use of time amplifiers (TAs) [5, 6, 7].

As has been reported in recent publications [8], cascaded structures represent one of the more reasonable candidate methods for achieving the gain needed for successful jitter amplification. Unfortunately, the output offset time of cascaded TA is large and, in practical applications, must be compensated for by means of a variable delay line at the output [5], which may increase the implementation cost.

In this paper, we present a low-offset (and thus, low-cost) TA that uses reconfigurable inter-stage connections. Although a limited case of this study was reported in a previous work as a conference proceeding [9], this study demonstrates the circuit implementation and presents the theoretical analysis of general cases for the first time. The reminder of this paper is organized as follows. Section II describes the design of the proposed time amplifier. Section III presents the simulation conditions and results. Section IV concludes the paper.

2 Low-offset cascaded time amplifier with reconfigurable inter-stage connection

The mechanism of offset reduction in the proposed reconfigurable inter-stage connection is explained qualitatively and quantitatively in this section. Fig. 1 shows the motivation and target of this work. From a practical standpoint, the ultimate objective of our research is to reduce the size of the variable delay line that is implemented in order to compensate for the time amplifier offset. By introducing the proposed test and reconfigurable inter-connection, the time offset in the worst case can be reduced.

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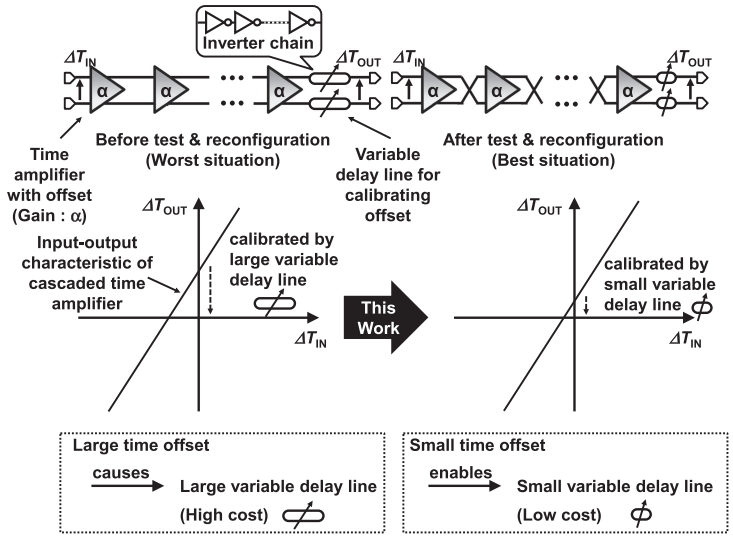

Fig. 1. Motivation and target of this work. Triangle means α-gain time amplifier with time offset. The ellipsoidal symbol with arrow means the variable delay line for calibrating time offset. The offset is calibrated by the variable delay line. The technique presented in this work reduces time offset and hence the size of the variable delay line for calibration can be reduced.

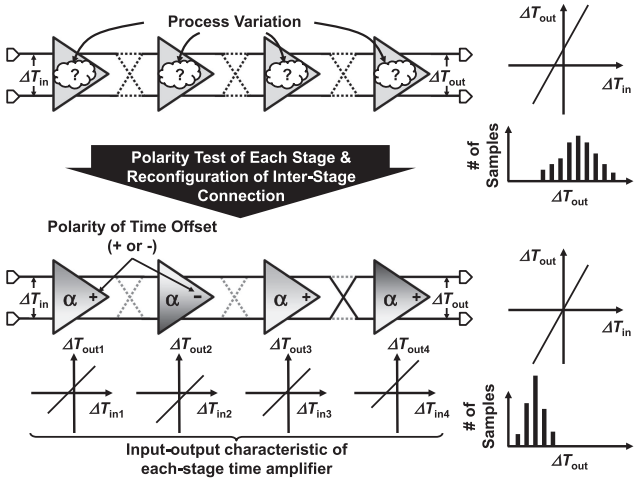

Fig. 2. Concept of the proposed time amplifier with reconfigurable inter-stage connection.

The size of the variable delay line should be determined by consideration of a worst-case scenario caused by performance shortfalls owing to process, voltage and temperature (PVT) variations. Fig. 2 shows the concept of the proposed time amplifier with reconfigurable inter-stage connection. The proposed technique improves performance in the worst-case scenario. In a cascaded structure, the worst case represents a situation in which the polarities of offset in each stage are identical; this condition is interpreted mathematically in the following sub-section. By optimizing the polarities of offset in each stage by reconfiguring the inter-connection switch, the offset can be reduced.

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2.1 Mathematical model of time amplifier

Fig. 3 illustrates the simplified model of the open-loop time amplifier. Open-loop structures are chosen instead of closed-loop structures in cases where a small footprint is needed [10, 11]. In the design procedure, time offset is designed to be zero. However, due to device variations, time offset in output signal, β is inevitable. In the simplified model presented here, the characteristics of the time amplifier are assumed to be linear where ΔT_{IN} is near zero. A variation in process will shift the curve of the output time difference (ΔT_{OUT}) as a function of the input time difference (ΔT_{IN}), resulting in an output time offset.

In order to simplify the model of process variation, the gain and output time offsets of all TAs are assumed to be α and β, respectively, with $\beta > 0$. On the basis of this assumption, the relationship between ΔT_{IN} and ΔT_{OUT} can be expressed using

$$\Delta T_{OUT} = \alpha \Delta T_{IN} + \beta. \tag{1}$$

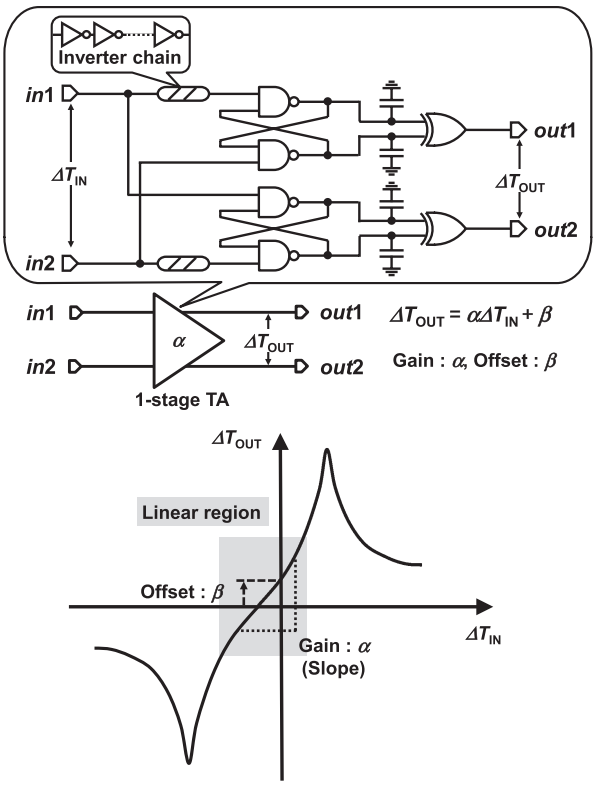

Fig. 3. Simplified model of the open-loop time amplifier. An open-loop time amplifier has linear region at near zero.

2.2 Mathematical background for offset reduction with reconfigurable inter-stage connection

Fig. 4 illustrates the theoretical background of the proposed reconfigurable inter-stage connection when assuming that the gains and offsets of each-stage TA are constant. In the conventional design without the reconfigurable inter-

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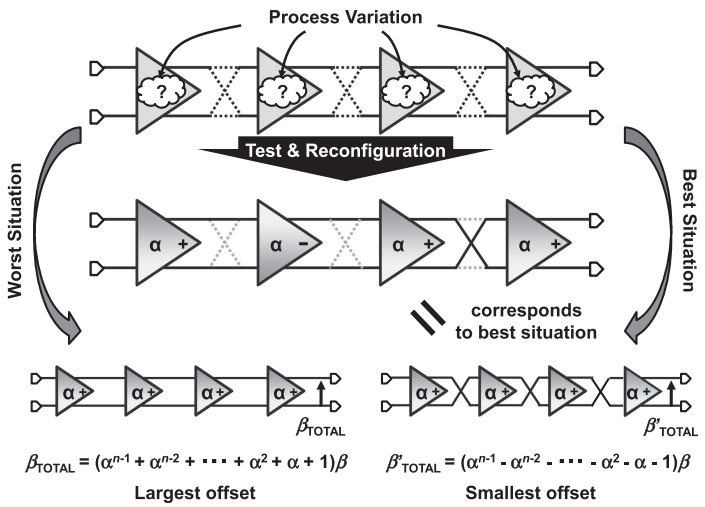

Fig. 4. Theoretical background of the proposed reconfigurable inter-stage connection when assuming that the gains and offsets of each-stage TA are constant.

stage connection, it is possible that worst situation with the largest offset occurs. On the other hand, the proposed technique with test and reconfigurable inter-stage connection provides best situation enabling the smallest offset. This characteristic is explained mathematically as followings.

From (1), the relationship between ΔT_{IN} and ΔT_{OUT} of a two-stage cascaded TA can then be expressed as

$$\begin{aligned}\Delta T_{OUT,2\text{-}stage} &= \alpha_2(\alpha_1 \Delta T_{IN} + \beta_1) + \beta_2 \\ &= \alpha_1\alpha_2 \Delta T_{IN} + \beta_1\alpha_2 + \beta_2 \end{aligned} \tag{2}$$

Thus, the total time offset of a two-stage cascaded TA can be given as

$$\beta_{TOTAL,2\text{-}stage} = \beta_1\alpha_2 + \beta_2 \tag{3}$$

The three-stage time offset can be extrapolated from the two-stage expression as

$$\beta_{TOTAL,3\text{-}stage} = \beta_1\alpha_2\alpha_3 + \beta_2\alpha_3 + \beta_3 \tag{4}$$

From (3) and (4), a generalized expression of the time offset for n-stages can be developed as follows:

$$\begin{aligned}\beta_{TOTAL,n\text{-}stage} = {} & \beta_1\alpha_2\alpha_3 \cdots \alpha_{n-2}\alpha_{n-1}\alpha_n \\ & + \beta_2\alpha_3\alpha_4 \cdots \alpha_{n-2}\alpha_{n-1}\alpha_n + \cdots \\ & + \beta_{n-1}\alpha_n + \beta_n \end{aligned} \tag{5}$$

If the gains and offsets at all the stages are constant, (5) can be simplified to

$$\beta_{TOTAL,n\text{-}stage} = (\alpha^{n-1} + \alpha^{n-2} + \cdots + \alpha^2 + \alpha + 1)\beta \tag{6}$$

This equation indicates that the time offset will increase as an edge propagates through each TA; thus, a non-twisted, cascaded TA will maximize the total time offset (i.e., the worst-case time offset, as shown in the upper part of Fig. 4).

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On the other hand, a twisted-cascaded TA can also reduce the total time offset, β'_{TOTAL}:

$$\begin{aligned}\beta'_{TOTAL,n\text{-}stage} = {} & \beta_1\alpha_2\alpha_3\cdots\alpha_{n-2}\alpha_{n-1}\alpha_n \\ & - \beta_2\alpha_3\alpha_4\cdots\alpha_{n-2}\alpha_{n-1}\alpha_n - \cdots \\ & - \beta_{n-1}\alpha_n - \beta_n \end{aligned} \tag{7}$$

When assuming that the gains and offset of all the stages are constant, (7) can be simplified to the following expression as shown in the lower part of Fig. 4;

$$\beta'_{TOTAL} = (\alpha^{n-1} - \alpha^{n-2} - \cdots - \alpha^2 - \alpha - 1)\beta \tag{8}$$

Following the theoretical analysis above, the proposed reconfiguring of inter-stage connection can be mathematically shown to be effective for reducing the time offset in a cascaded TA.

The theoretical analysis above also indicates that the total output offset of the earlier stages is more important than that of the latter stages, as the output calculation of each stage amplifies the output offset of each of the earlier stages, which can be readily seen from (5) and (7).

2.3 Procedure for testing and connectivity reconfiguration

Fig. 5 shows the procedure for testing and reconfiguring the inter-stage connections in the proposed cascaded TA. The procedure is developed as below.

The proposed cascaded TA initially operates in a test mode in which the two inputs of each TA stage are connected. After this, a test signal in the form of a digital pulse is fed into the shorted inputs; by checking the output of the

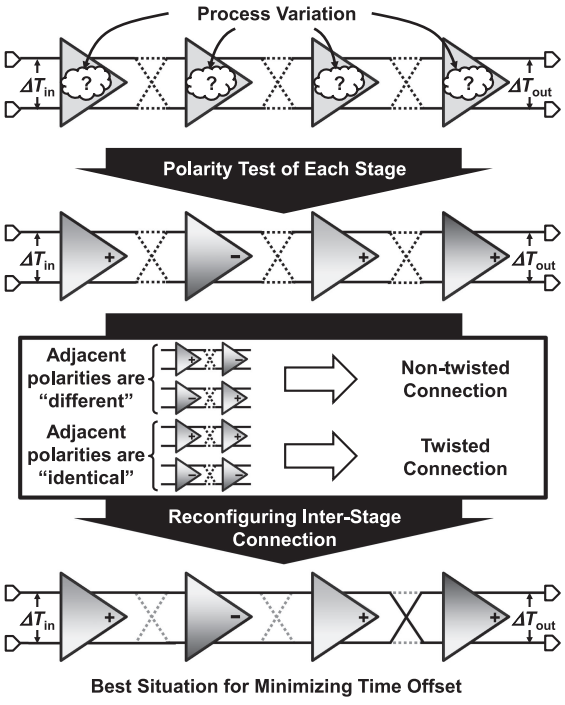

Fig. 5. Procedure of the proposed reconfigurable inter-stage connection.

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flip-flop that serves as a timing comparator, the TA obtains a test result containing the polarity of offset of each TA stage. This information is stored in the memory (e.g., flip-flops).

The next step is the reconfiguration mode, in which the inter-stage connections are reconfigured on the basis of the preceding test results. As stated above, the total offset can be reduced when their polarities are inversely serialized (e.g., $+-+-+-\ldots$). Thus, when adjacent polarities are different, the switches are set to be not-twisted connection. On the other hand, when adjacent polarities are identical, the switches are set to be twisted connection.

As a result of this procedure, the inter-stage connections can be reconfigured.

2.4 Procedure for testing and connectivity reconfiguration

Fig. 6 depicts the circuit implementation of the proposed TA with reconfigurable inter-stage connections. The circuit consists of switches, flip-flops, and EXOR gates, and its simplicity and low additional area overhead make it suitable for on-chip test circuit implementation. The circuit operation procedure is given as follows:

1. Two input ports in each TA stage are electrically shorted.
2. A test stimulus is then fed into each TA stage, and its flip-flop, which serves as a timing comparator, generates test results, the values of which depend on the polarity of the time offset within that particular stage. These results are stored in the flip-flops.
3. The output signals of adjacent flip-flops are fed into the input of an exclusive-or (XOR) logic gate. On the basis of the output of the gate, the inter-stage connections are reconfigured.

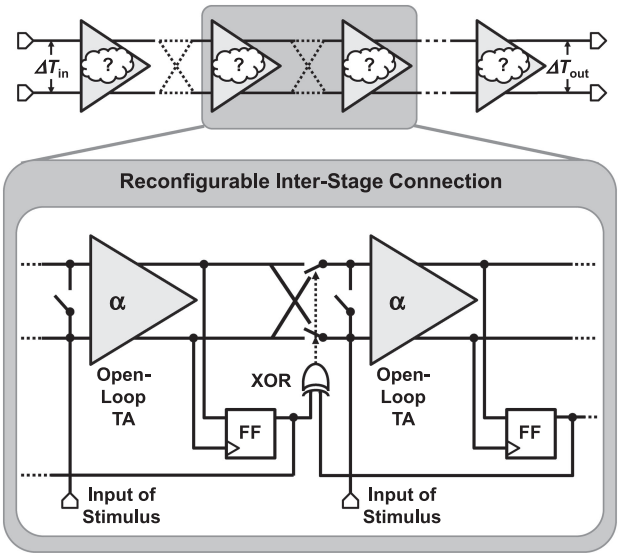

Fig. 6. Circuit implementation of the proposed cascaded time amplifier with reconfigurable inter-stage connection. A test stimulus is fed into each TA stage via the input of stimulus.

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Execution of this procedure reconfigures the inter-stage connections, which, as shown in the previous theoretical analysis, allows the total output offset of the TA to be reduced.

2.5 Minimization of the offset

In usual situation where the time offset of each TA is almost equal, the proposed technique can minimize the total offset effectively. However, when number of stages is more than three and the offset is in unusual condition, the proposed technique cannot minimize (only reduce) the total offset.

In order to explain the cases when the offsets are minimized or not, the condition that number of stages is three is introduced and discussed. There are following four candidates of the offsets.

$$\beta_{TOTAL,3\text{-}stage,++} = \beta_1\alpha_2\alpha_3 + \beta_2\alpha_3 + \beta_3 \tag{9}$$

$$\beta_{TOTAL,3\text{-}stage,+-} = \beta_1\alpha_2\alpha_3 + \beta_2\alpha_3 - \beta_3 \tag{10}$$

$$\beta_{TOTAL,3\text{-}stage,-+} = \beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 + \beta_3 \tag{11}$$

$$\beta_{TOTAL,3\text{-}stage,--} = \beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 - \beta_3 \tag{12}$$

In usual case, $\beta_{\mathrm{TOTAL,3\text{-}stage,--}}$ is the minimum and the proposed technique successfully functions. However, in unusual case, $\beta_{\mathrm{TOTAL,3\text{-}stage,+-}}$ $\beta_{\mathrm{TOTAL,3\text{-}stage,-+}}$ has possibility to be the minimum. Mathematically, the following analysis can be obtained.

$$\begin{aligned}
|\beta_{TOTAL,3\text{-}stage,+-}| &< |\beta_{TOTAL,3\text{-}stage,--}| \\
&\Leftrightarrow |\beta_1\alpha_2\alpha_3 + \beta_2\alpha_3 - \beta_3| < |\beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 - \beta_3| \\
&\Leftrightarrow \beta_1\alpha_2\alpha_3 + \beta_2\alpha_3 - \beta_3 < -(\beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 - \beta_3) \\
&\Leftrightarrow \beta_1\alpha_2\alpha_3 - \beta_3 < 0
\end{aligned} \tag{13}$$

$$\begin{aligned}
|\beta_{TOTAL,3\text{-}stage,-+}| &< |\beta_{TOTAL,3\text{-}stage,--}| \\
&\Leftrightarrow |\beta_1\alpha_2\alpha_3 + \beta_2\alpha_3 - \beta_3| < |\beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 - \beta_3| \\
&\Leftrightarrow \beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 + \beta_3 < -(\beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 - \beta_3) \\
&\Leftrightarrow \beta_1\alpha_2\alpha_3 - \beta_2\alpha_3 < 0
\end{aligned} \tag{14}$$

Under above conditions, $\beta_{\mathrm{TOTAL,3\text{-}stage,--}}$ does not have minimum offset. For instance, when $\alpha_2 = \alpha_3 = 3$, $\beta_1 = 1$, $\beta_2 = 10$ and $\beta_3 = 100$, total offsets are $139(\beta_{\mathrm{TOTAL,3\text{-}stage,++}})$, $-61(\beta_{\mathrm{TOTAL,3\text{-}stage,+-}})$, $71(\beta_{\mathrm{TOTAL,3\text{-}stage,-+}})$ and $-121(\beta_{\mathrm{TOTAL,3\text{-}stage,--}})$. The minimum offset is $\beta_{\mathrm{TOTAL,3\text{-}stage,+-}}$.

3 Verification with SPICE simulation

3.1 Simulation conditions

In order to verify the effectiveness of the proposed technique, we performed a SPICE simulation of a 65-nm standard complementary metal-oxide-semiconductor (CMOS) technology node using Spectre RF software supplied by Cadence Design Systems Inc. A statistical analysis was obtained by running the model at a nominal power supply voltage of 1.2 V through a Monte Carlo simulation based on process variations.

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The model specifications were developed on the basis of their likely applicability to a device used for on-chip timing of jitter measurements [5]. The simulated TA had four stages and a gain of approximately 100; the gain at each TA stage was a constant value of approximately 3.2 (the gains were relatively small in order to achieve a small footprint while enabling high-speed operation [12]). The TA stage design was based on the specifications developed in previous studies [13].

3.2 Simulation results

Fig. 7 shows the results obtained from the simulation. The results indicate that the proposed time amplifier with reconfigurable inter-stage connection is effective for offset reduction. The TA stage offsets are +1.11 ps, −1.34 ps, −0.44 ps, and +6.38 ps. The worst inter-stage connection is the sixth one from the top in the figure, while the best is the third from the top; as hypothesized, the best-case results come from reconfiguring the TA using the proposed technique. In doing so, the total offset is reduced from 327 to 180 ps, corresponding to 45% offset reduction.

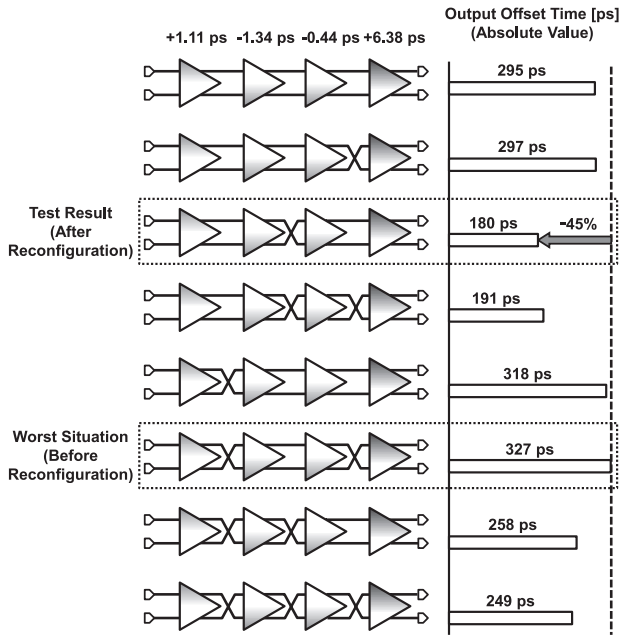

Fig. 7. Simulated effectiveness of the proposed time amplifier with reconfigurable inter-stage connection.

The results of the Monte Carlo analysis are shown in Fig. 8. Monte Carlo analysis was performed 30 times with changing transistors' widths and lengths. The worst-case time offset shows a reduction from 745 to 353 ps, corresponding to a 52.6% offset reduction. The center of the probability distribution function (PDF) also shows a reduction from 290 to 191 ps, or a reduction by 34.0%. The results of this simulation verify that, as suggested in Fig. 2, the offset reduction is effective even when statistical process variations are taken into account; this suggests that the proposed technique would be effective in reducing the size of a variable delay line used for compensation.

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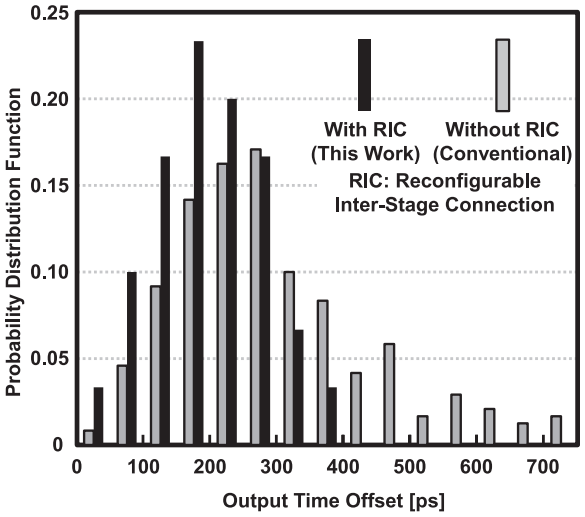

Fig. 8. Simulated effectiveness of the proposed time amplifier with reconfigurable inter-stage connection.

3.3 Area overhead

In this subsection, we discuss some disadvantages of the proposed technique, one of which is the need for additional area overhead. As described above, the target application for this technique is on-chip jitter measurement and, to do this, the area overhead must be minimized. However, additional circuitry is required to reconfigure the inter-stage connections. In order to evaluate the impact of the additional area overhead to the total area occupation, physical implantation into a 65-nm CMOS technology node was carried out.

The appropriate parameters for evaluating the area overhead are predicated on the design of the time amplifier. To simulate a typical situation, we assumed a TA gain of 100 and an input dynamic range of 10 ps, as these values are typical in the context of high-resolution jitter measurement [5]. Under these conditions, the net additional area overhead requirement is approximately 6.5%, which is small enough for practical applications. This relatively modest overhead increase is due to an offset to the additional area overhead by a corresponding reduction in the size of the variable delay line for compensating for the output time.

3.4 Potential of reconfigurable inter-stage connection

This subsection introduces the potential of the proposed reconfigurable inter-stage connection architecture. In previous sections, a simple, low-area overhead circuit design for evaluating the offset of TA was proposed.

Fig. 9 shows an example of an implementation of the proposed reconfigurable inter-stage connection circuit. In this architecture, the cascaded TA has a time-to-digital converter (TDC) for evaluating the total output offset. The circuit functions as follows:

1. The TDC measures the time offset of all possible connection patterns.
2. The embedded digital macro then compares the obtained offsets.
3. Finally, the inter-stage connection is reconfigured on the basis of the comparison results.

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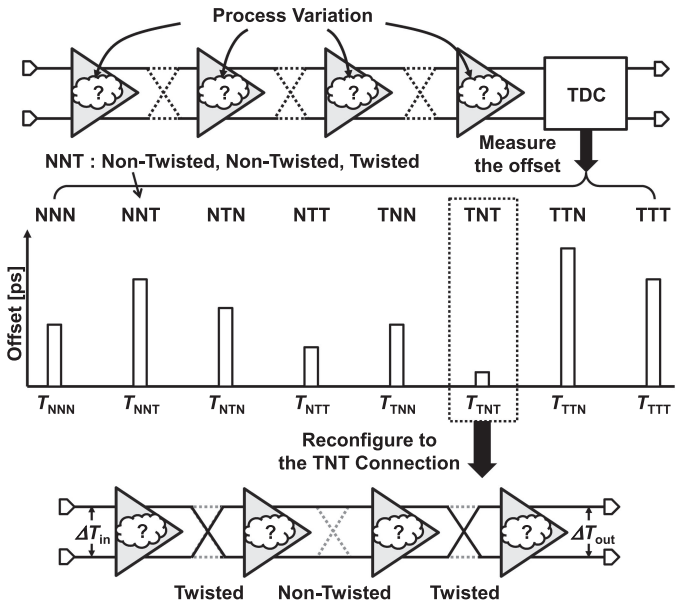

Fig. 9. Example of the circuit implementation for the proposed reconfigurable inter-stage connection.

This proposed inter-stage reconfiguration can be applied in various implementations in addition to the example shown in Fig. 9. The number of reconfigurable inter-stage connections can be optimized; if, for instance, the area requirements of a four-stage cascaded TA are severe, the number of connections can be reduced from three to one. This scalability can provide particular merit in cost-sensitive, on-chip, built-in-self-test (BIST) applications.

Moreover, the positions of the reconfigurable connections can also be optimized. The mathematical analysis in (5) and (7), which shows the importance of reducing the offset in the earlier stages, demonstrates the utility of reconfiguring the earlier inter-stage connections instead of the latter ones.

3.5 Robustness of reconfigurable inter-stage connection against dynamic voltage and temperature changes

The proposed reconfigurable inter-stage connection can improve the robustness against static PVT variations. If the inter-stage connection is frequently reconfigured, dynamic voltage and temperature changes can be compensated. However, under usual condition where the reconfiguration is performed only at start up, it does not have robustness against dynamic voltage and temperature changes. It is our future work to address this issue.

4 Summary

In this paper, we reported on a low-offset time amplifier based on a reconfigurable inter-stage connectivity architecture. By testing process variations and reconfiguring the inter-stage connections based on the test results, the offset time could be reduced significantly with a small additional area overhead. A statistical SPICE simulation in a 65-nm CMOS technology node was per-

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formed in order to confirm the effectiveness of the proposed technique; the simulation results showed that the proposed TA achieved a 45% offset reduction, which matches well with the theoretical estimates.

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