Experimental Verification of Timing Measurement Circuit With Self-Calibration

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***Abstract*—This paper describes the architecture, implementation and measurement results for a Time-to-Digital Converter (TDC), with histogram-method self-calibration, for high-speed I/O interface circuit test applications. We have implemented the proposed TDC using a Programmable System-on-Chip (PSoC), and measurement results show that TDC linearity is improved by the self-calibration. All TDC circuits, as well as the self-calibration circuits can be implemented as digital circuits, even by using FPGA instead of full custom ICs, so this is ideal for fine CMOS implementation with short design time.**

Keywords—Time-to-Digital Converter, Time Measurement, Self-Calibration, Histogram Method, FPGA

I. INTRODUCTION

A Time-to-Digital-Converter (TDC) measures the time interval between two edges, and time resolution of several picoseconds can be achieved when the TDC is implemented with an advanced CMOS process. TDC applications include phase comparators of all-digital PLLs, sensor interface circuits, modulation circuits, demodulation circuits, as well as TDC-based ADCs [1-3]. The TDC will play an increasingly important role in the nano-CMOS era, because it is well suited to implementation with fine digital CMOS processes; a TDC consists mostly of digital circuitry, and resolution improves as switching speed increases.

There are various kinds of TDC circuits, and here we focus on the flash-type TDC. It uses a delay line composed of CMOS inverter buffer delays; however their absolute and relative values vary due to process, supply voltage and temperature (PVT) variations, and this degrades the TDC linearity. Hence self-calibration techniques are required [5-8].

In this paper, we describe a simple circuit which measures the time between two edges of timing signals with high linearity: We report the design of the self-calibration flash type TDC and its experimental verification as Built-Out Self-Test (BOST) [8] for digital signal timing measurement.

II. FLASH-TYPE TDC WITH RING OSCILLATOR

〈2・1〉 Flash-type TDC

The TDC can be used to measure digital signal timing. The architecture of a basic flash-type TDC is shown in Fig.1. It consists of a delay-line using delay cells in the signal path and an array of D flip-flops. The input START signal passes along the delay cells, which are connected in series. Then each signal is connected to the D input terminal in the D flip-flop array. The START signal is delayed by an integer multiple of the buffer delay τ. The state of each D flip-flop is latched by the rising edge of the STOP signal. This circuit converts the time delay between the signals to a certain number of steps of buffer delay. That is, the output from the D flip-flop is obtained as a thermometer code (unary code) output showing the time delay between START signal and STOP signal, and this time delay is obtained as a digital output Dout using a thermometer-code-to-binary encoder.

The flash-type TDC has the advantage of being able to measure a single-event input, however its problem is that each buffer delay value can vary and be different from each other, which degrades the overall linearity of the TDC. We use a ring oscillator for the linearity calibration [4, 5]. Also the absolute value of the average buffer delay τ may vary among TDC circuits, which causes TDC gain error. We use a reference clock generator (whose frequency is known a priori) for the gain calibration. We have implemented the flash-type TDC with self-calibration using a Programmable System-on-Chip 5 (PSoC) LP of Cypress Semiconductor Corporation, and performed experiments to validate self-calibration for many delay-variation cases.

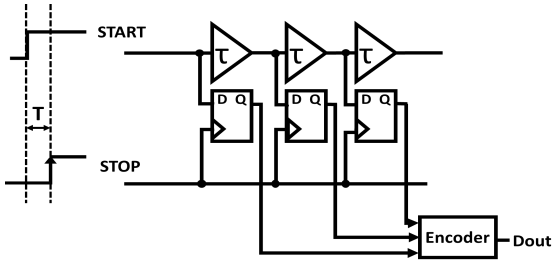

Fig.1. Flash-type TDC.

Fig.2 shows a timing chart for the TDC, where τ is average delay, Δτ is deviation from τ, and D is TDC digital output. In Fig. 2 (a), it is assumed that all delay elements have the same delay τ. If the rising timing difference of START and STOP is between 2τ and 3τ, then D0, D1 are 1 and D3, D4 are 0. On the other hand, Fig.1 (b) shows the case where the second delay element has a delay variation of Δτ, which causes TDC nonlinearity. Fig.2 (b) shows the case Δτ>0, but even in the case Δτ<0 the TDC linearity is degraded.

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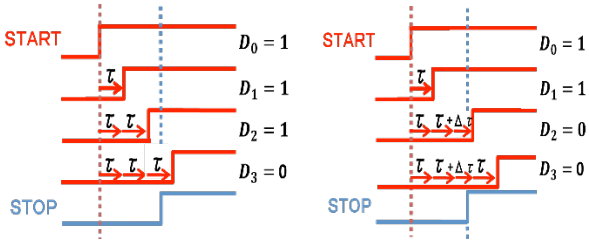

(a) Without delay variation. (b) With delay variation.
Fig.2. Timing diagram of TDC circuit.

〈2・2〉 Flash-type TDC with Self-Calibration

Fig. 3 shows a flash-type TDC with self-calibration. [4][5] The self-calibration circuit consists of a ring oscillator with 24 buffers and one inverter, and histogram engine/digital error correction circuit. We would like to emphasize that the self-calibration circuit is implemented only with digital circuits.

In Fig.3 a ring oscillator is employed on the upper row. By controlling the select signal of the multiplexer, calibration mode or measurement mode is determined. In calibration mode, the ring oscillator is configured and the histogram engine is used, while in measurement mode, the ring oscillator closed-loop is open and the digital error correction circuit works.

Fig.4 shows the flow chart of self-calibration and digital error correction. In calibration mode, the relative variation (ratio) among delay elements are measured with the histogram method. [4,5,6] In measurement mode, the TDC digital output is corrected based on the histogram data to improve the TDC linearity.

Here we have implemented the TDC main circuit, the encoder, and the histogram engine on a PSoC, and calculated the raw TDC nonlinearity and its digital error correction on PC.

(1) Calibration Mode (Histogram Data Acquisition) :

In calibration mode, a ring oscillator is configured by connecting the delay line output and input with the multiplexer select signal control. While this ring oscillator runs freely, a clock is inputted from the STOP signal; the ring oscillator and the clock are set to be asynchronous (without correlation). Then the encoder reads values of the D flip-flop array, and the histogram for each bin (digital output) is computed.

If all the delay values were equal and the number of measurement times were sufficiently large, the histogram for each digital output would be equal. However, in practice, variations among delays exist. When the ring oscillator runs freely, the STOP signal rising edge exists for a digital output with probability proportional to the delay value of the corresponding delay cell. [4,5,6] Thus the each delay (relative) value can be measured by the histogram for the corresponding digital output of the TDC, when the number of the measurement cycles is large enough.

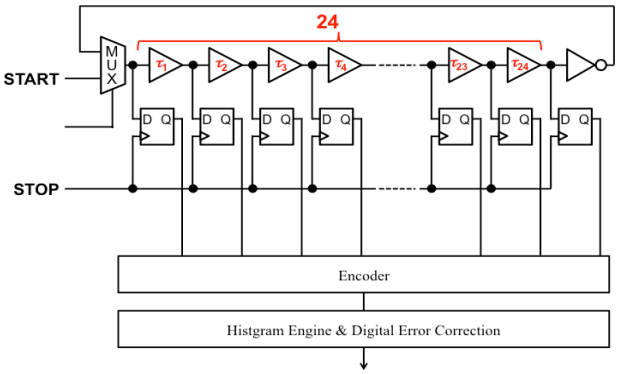

Fig.3. Flash TDC with a ring oscillator.

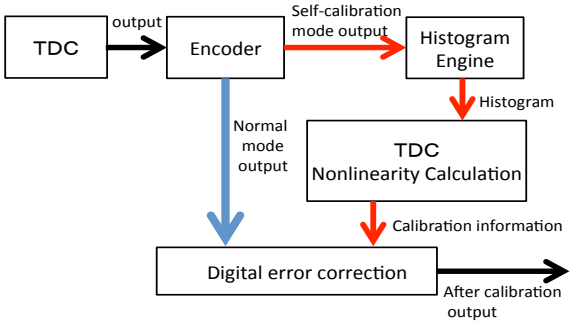

Fig.4. Flow chart of calibration and digital error correction.

(2) Measurement Mode: In measurement mode, START signal and STOP signal are inputted just like a normal flash-type TDC, and the digital value corresponding to their rising edge timing difference is outputted.

(3) Digital error correction operation: Each (relative) delay value in the delay cells is obtained by histogram measurement in calibration mode. In measurement mode, the digital error correction operation is performed based on the obtained delay values, as shown in eq. (1).

$$\mathrm{Dout}(N) = \frac{\sum_{i=1}^{\mathrm{N}} \mathrm{Pin}(i)}{\sum_{i=1}^{\mathrm{FS}} \mathrm{Pin}(i)} \times \mathrm{FS} \qquad (1)$$

N:Raw TDC dgital output to be corrected
Dout(N):Corrected digital output for raw TDC output N
Pin(i):Histogram for raw TDC output i
FS:Maximum TDC digital output value

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III. PSoC Implementation and Experiment

We have implemented the self-calibration TDC circuit in Fig. 2 on PSoC (its photo is shown in Fig. 5), and performed experiments to verify the effectiveness of self-calibration.

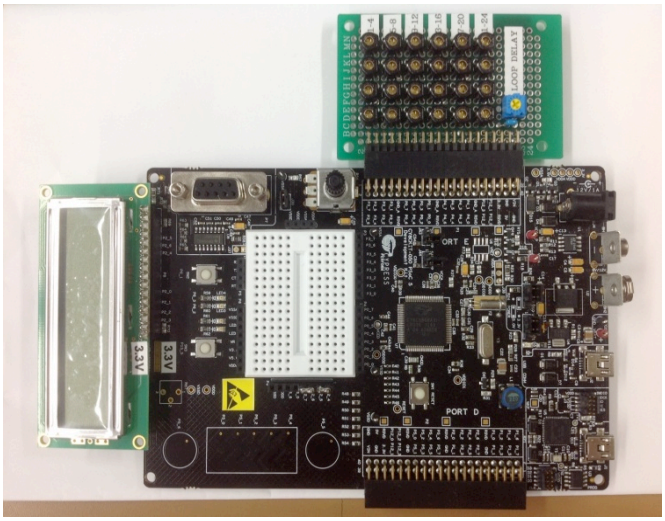


Fig.5. Self-calibration flash-type TDC implemented with PSoC.

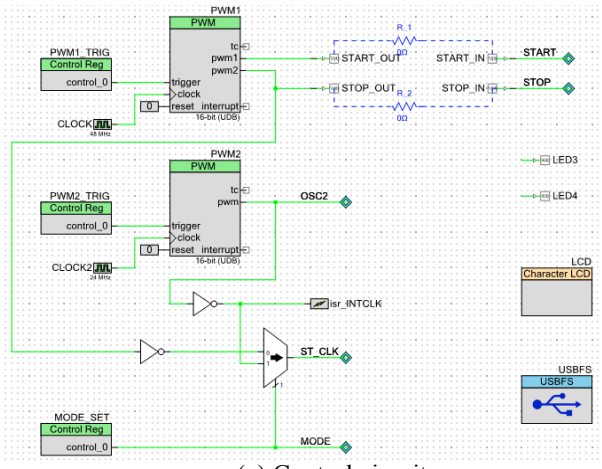
(1) PSoC Circuit Design for TDC with Self-Calibration :

Fig.6 (a) shows control circuit of the whole circuit, where calibration or measurement mode is set by Control Register. **START**, **STOP** and the test mode signal in Fig. 3 are generated by PWM and Control Register in Fig. 6 (a). Fig. 6 (b) shows the TDC main part while Fig.6 (c) shows the encoder.

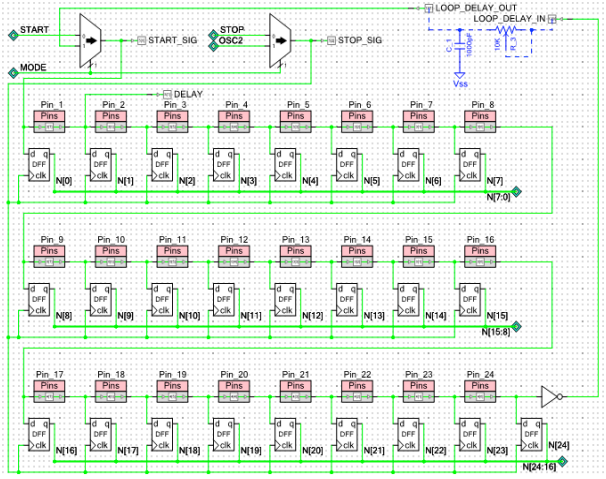
In measurement mode, **CLOCK** source on PSoC is used for **PWM1** in Fig.6 (a) to generate **START** and **STOP** signals. **START** signal is generated and after a given number of cycles **CLOCK** (its frequency is 48MHz, and hence the time resolution is 20.83ns), **STOP** signal is issued.

A signal is issued from MODE_SET Control Register to change the operation mode. Fig. 6 (b) shows the TDC with a ring oscillator. In measurement mode, **START** and **STOP** signals are issued through the multiplexer, and it operates as a normal flash-type TDC. Each delay is realized with RC delay of an embedded resistor (5.6kΩ) in I/O pin and an external variable capacitor (10pF-120pF); each delay value can be setup by adjusting the variable capacitor value individually. (Delay variation can be set with a certain amount of flexibility.)

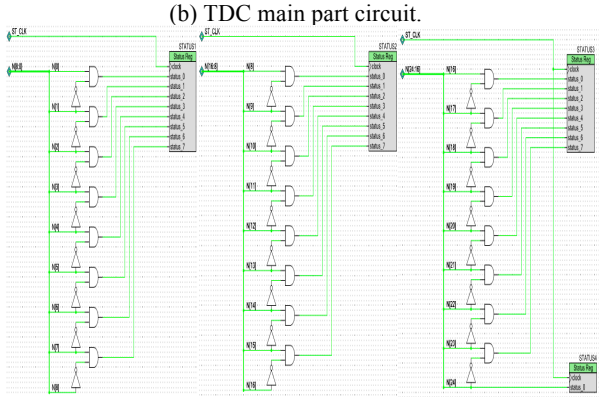
Fig. 6 (c) is the encoder circuit to which each flip-flop output is fed, and Fig.7 shows an example of encoding. In this measurement, we pay attention only to the rising edges of **START** and **STOP**, but not to the falling edges.



(a) Control circuit



(b) TDC main part circuit.



(c) Encoder circuit

Fig.6. Circuit Schematics of the self-calibration TDC implemented with PSoC. (a) Control circuit. (b) Main TDC circuit. (c) Encoder.

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Table 1. Measured histogram in calibration mode.

Pin1	Pin2	Pin3	Pin4	Pin5	Pin6	Pin7	pin8	Pin9	Pin10	Pin11	Pin12
1,565	743	1,860	1,927	546	1,771	1,782	1,909	1,862	1,937	2,069	2,181
Pin13	Pin14	Pin15	Pin16	Pin17	Pin18	Pin19	Pin20	Pin21	Pin22	Pin23	Pin24
1,873	783	1,898	944	1,765	1,913	1,768	2,019	1,786	2,077	1,750	2,206

Table 2. Measurement results in normal measurement mode.

Transiton point(ns)	0	541	812	1,437	2,104	2,291	2,895	3,500	4,166	4,770	5,395	6,083	6,791
TDC outputs	0	1	2	3	4	5	6	7	8	9	10	11	12
Transiton point(ns)	7,416	7,645	8,270	8,583	9,145	9,770	10,354	11,000	11,583	12,250	12,812	13,541	
TDC outputs	13	14	15	16	17	18	19	20	21	22	23	24	

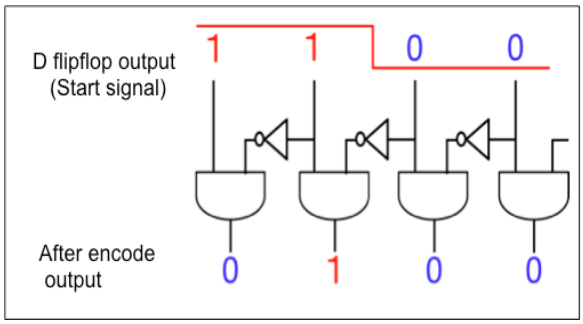

Fig.7. Example of encoding.

The inverted STOP signal by the control circuit is fed to Status Register as a trigger. Pin1 output is read to STATUS1 register as status1, Pin23 output is STATUS3 as status23, and Pin24 output is STATUS24 as status0 and then the TDC measurement is performed.

In calibration mode, **PWM2** to **OSC2** are fed for **STOP** signal repeatedly in Fig.6 (a). **STOP** signal is inputted into **OSC2** from **PWM2**. Inverted **STOP** signal of multiplexer **PWM2** as well as the self-calibration mode signal are given as outputs.

In Fig. 6 (b), one input of the left-hand side multiplexer is connected to the inverter output, and the ring oscillator circuit can be configured. Aside from the individual delay element, an RC delay circuit with a large time constant by a variable resistor of 0-10 kΩ and a capacitor of 1000 pF is put to make the frequency of the whole ring oscillator lower. The right side multiplexer makes **PWM2** output signal to be **STOP** signal.

The encoder in Fig.6 (c) operates similar to in measurement mode. Pin1 output is read to STATUS1 register as status0, Pin24 output is STATUS23 as status7, and then the TDC calibration is performed.

(2) PSoC Implementation of TDC with Self-Calibration :

A PC is connected with PSoC terminals for writing, and the mounting to PSoC is performed by giving information for the circuit configuration, including modules, output pins, and wirings arranged in PSoC on a circuit diagram. Moreover, the embedded program which controls clock rising timing and reading timing of the output value of each bit is written with C language, and is loaded to the PSoC main part. Furthermore, PSoC measurement software is developed in C# language on the PC.

(3) PSoC operation : In calibration mode, the ring oscillator in PSoC runs freely and the **STOP** signal is inputted. Then each D Flip-Flop output is fed to the encoder. In this measurement, 100,000 times of STOP signal were inputted and total 40,934 suitable outputs (where both **START** and **STOP** rise) were obtained; then the histogram data was obtained, and Table 1 shows the measured histogram result for each bin.

In measurement mode, **START** and **STOP** signals are fed to the TDC where their rising edge timing difference is controlled by the reference clock (**CLOCK**) frequency division and hence its value is known a priori (hence TDC gain characteristics can be calibrated) and the raw TDC characteristics measurement results are shown in Table 2.

IV. Experiment of Self-Calibration

Measured histogram data for each bin of the PSoC TDC with the self-calibration is normalized with dividing by (total number of measurements) / (total delay amount), and its correlation with each delay amount are shown in Fig. 8 and Table 3. We see that there is strong correlation between the histogram and the corresponding delay amount; its discrepancy is within 13%.

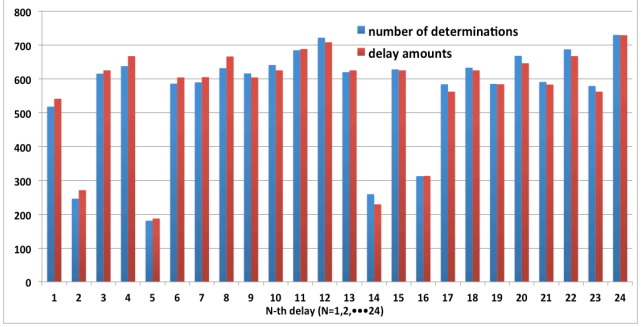

Fig.8. Correlation between of histogram and corresponding delay value (measurement results of sample #1).

Table 3. Measurement results of error between the delay value and the corresponding histogram (sample #1) (%)

Pin1	Pin2	Pin3	Pin4	Pin5	Pin6	Pin7	pin8	Pin9	Pin10	Pin11	Pin12
-4.31	-9.30	-1.55	-4.43	-3.41	-3.01	-2.56	-5.18	1.979	2.52	-0.52	1.90
Pin13	Pin14	Pin15	Pin16	Pin17	Pin18	Pin19	Pin20	Pin21	Pin22	Pin23	Pin24
-0.87	13.11	0.46	-0.23	3.89	1.25	0.15	3.39	1.34	3.01	3.01	0.10

Table 4. TDC outputs after calibration (sample #1).

Transition point(ns)	0	541	812	1,437	2,104	2,291	2,895	3,500	4,166	4,770	5,395	6,083	6,791
Corrected outputs	0	0.917	1.353	2.443	3.573	3.893	4.932	5.976	7.096	8.187	9.324	10.536	11.815
Transition point(ns)	7,416	7,645	8,270	8,583	9,145	9,770	10,354	11,000	11,583	12,250	12,812	13,541	
Corrected outputs	12.913	13.372	14.485	15.038	16.073	17.195	18.231	19.415	20.462	21.680	22.706	24	

The linearity is calibrated based on the correlation between the histogram and the delay amount as described in Section 2 using the algorithm in [9]. The corrected TDC outputs after calibration are shown in Table 4. Also the input and output TDC characteristics before and after calibration are shown in Fig. 9, and we see that the TDC linearity is improved.

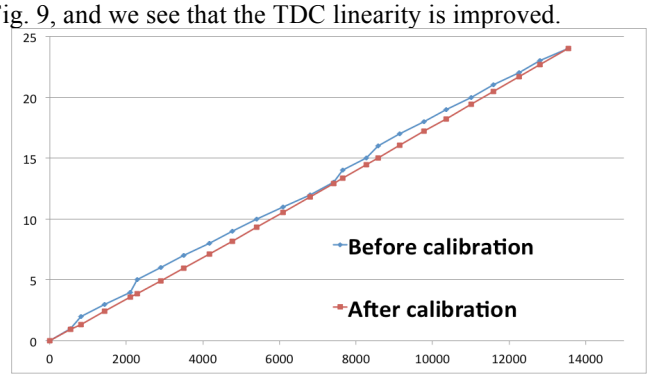

Fig.9. TDC characteristics before and after calibration (sample #1).

V. Evaluation of Measurement Results

We evaluate the measurement results of the proposed self-calibration method quantitatively. We use a straight-line linear approximation using a least-mean-square (LMS) method, and calculate the integral nonlinearity (INL) or the deviation from the straight line. INL is an index of the cumulative error between the measurement result and the linear approximation straight line; it is desirable that it is close to 0. The gain of the linear approximation straight line and offset can be denoted by the following formulas.

$$\text{gain} = \frac{N \cdot K_4 - K_1 \cdot K_2}{N \cdot K_3 - K_1^2} \quad (2)$$

$$\text{offset} = \frac{K_2}{N} - \text{gain} \cdot \frac{K_1}{N} \quad (3)$$

Here N= 24 and K1 to K4 are defined as follows:

$$K_1 = \sum_{i=0}^{N-1} i \quad (4)$$

$$K_2 = \sum_{i=0}^{N-1} S(i) \quad (5)$$

$$K_3 = \sum_{i=0}^{N-1} i^2 \quad (6)$$

$$K_4 = \sum_{i=0}^{N-1} i \cdot S(i) \quad (7)$$

Here *i* indicates a normalized input time difference given by the reference clock division and S(i) is the corresponding TDC output histogram. It follows from eqs. (2) - (7) that INL is calculated by

$$\text{INL(i)} = \frac{S(i) - (gain \cdot i + offset)}{gain} \quad (8)$$

INL calculated from this formula and measured data is shown in Fig. 10, and we see that INL is reduced by (more than) 2/3 with the calibration.

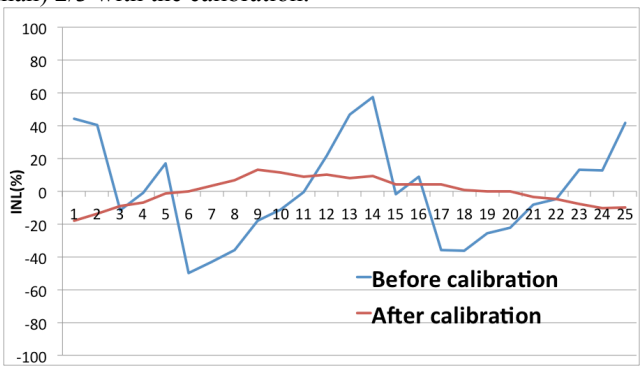

Fig.10. Measured INL before and after calibration (sample #1).

In this PSoC implementation of the TDC with self-calibration, each delay can be changed by adjusting the corresponding variable capacitor, and we have measured INL before and after calibration for several delay-amount cases as shown in Figs. 11-15. We see that in all cases the INL is reduced after the calibration.

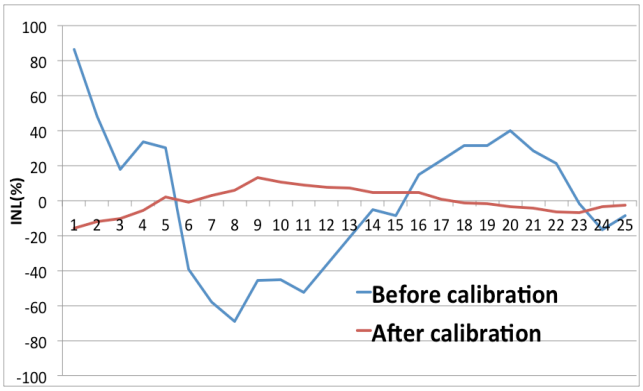

Fig.11. Measured INL before and after calibration (sample #2).

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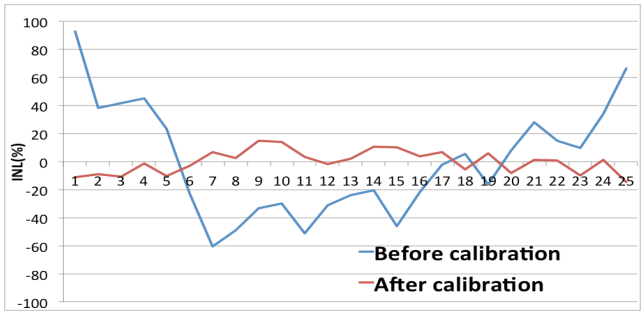

Fig.12. Measured INL before and after calibration (sample #3).

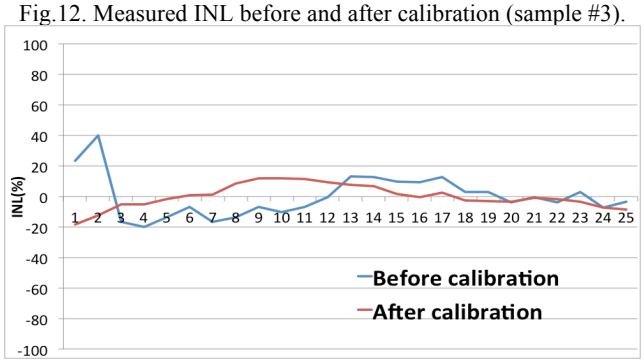

Fig.13. Measured INL before and after calibration (sample #4).

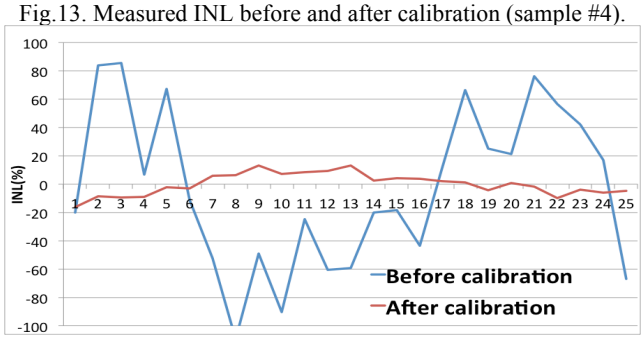

Fig.14. Measured INL before and after calibration (sample #5).

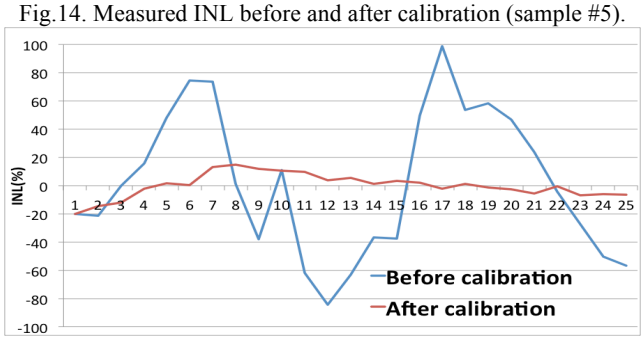

Fig.15. Measured INL before and after calibration (sample #6).

VI. Conclusion

In this paper, we have shown implementation and experimental results for a TDC with self-calibration using an analog FPGA or PSoC of Cypress Semiconductor Corporation. Two digital timing input signals are generated on the PSoC and fed to the TDC where a given time difference is known a priori, and the TDC characteristics is measured. Our measured results show that the histogram and the delay values have strong correlation. We have proposed self-calibration for the TDC linearity, and measurement results show that linearity is improved by the proposed method. We emphasize that the self-calibration circuit is full digital.

Our objective here was to verify the basic operation or principle of the histogram calibration method, and we used a rather simple circuit; while its time resolution is not fine, the number of measurements for the histogram is not large.

As a next step, we are collecting data for many delay variation cases and analyzing them; each delay can be easily changed because each delay is implemented with an embedded resistor and an external variable capacitor, and each capacitor value can be changed individually. These results will be reported in the workshop.

Finally we close this paper by remarking that this time we use an analog FPGA (or PSoC) to change each delay value individually, for experimental purposes. However we can implement the whole system with only digital circuit, and we actually have implemented it with the Xilinx FPGA which is expected to be used as a BOST for timing signal testing.

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