Phase Noise Measurement Techniques Using Delta-Sigma TDC

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***Abstract* - This paper describes two techniques for measuring phase noise of a clock using a delta-sigma time-to-digital converter (TDC). One technique uses a reference signal (which has only very small phase noise), and the other does not use a reference signal. Both proposed techniques can be implemented with relatively simple circuitry, due to the following: (i) The clock under test (CUT) is a repetitive signal. (ii) The time resolution with CUT and a reference clock can be increased by using longer measurement time with the delta-sigma TDC. (iii) The phase noise power spectrum can be calculated from the delta-sigma TDC output data using FFT. Costly high-performance spectrum analyzers which average several-time phase measurement results over a long measurement time (about 10s order), are not needed for phase noise measurement with the proposed technique. The other technique, which differs in that it uses a self-referenced clock rather than a reference signal, has potential wide applications.**

Keywords : Phase Noise Measurement, Time-to-Digital Converter, Delta-Sigma Modulation, PLL Testing

I. INTRODUCTION

In recent years, thanks to the advancement of semiconductor manufacturing processes, the semiconductor fabrication cost per transistor has decreased, while testing costs may increase if testing-related technologies are not improved; hence much attention is being paid to low-cost, high-quality testing technology [1].

We here consider how to perform low-cost high-quality phase noise testing of phase locked loop (PLL) circuits without using a spectrum analyzer. Phase noise is one of the most important performance metrics of PLL circuits [1-7], and to measure it directly [3] requires a spectrum analyzer with long measurement time (say, 10 seconds). Hence industry is looking for a technology breakthrough to provide low-cost high-quality testing.

Jitter and phase noise on-chip testing circuits have already been proposed in [5, 6]. However, the on-chip jitter measurement circuit [5] can measure the rms value of jitter (phase noise), but not phase noise versus frequency. The technique in [7] uses a normal flash TDC which does not have fine time resolution, so precision phase noise measurement is not possible.

This paper proposes two techniques for measuring phase noise of a clock using a delta-sigma TDC [8]. One technique uses a reference signal (which has only very small phase noise) [9]. The other is a new technique that doesn't use a reference signal, and has potential wide applications.

The delta-sigma TDC is useful for phase noise measurement because the clock under test (CUT) is a repetitive signal, and the time resolution with CUT and a reference clock can be increased by using longer measurement time in the delta-sigma TDC. We can also obtain the frequency characteristics of the phase noise by applying FFT to the TDC outputs.

We show the validity of the proposed methods with theoretical analysis and MATLAB simulations. The proposed techniques can realize low-cost phase noise testing without requiring both an expensive spectrum analyzer and long testing time.

This paper consists of the following: Section 2 explains the delta-sigma TDC, Section 3 describes the proposed phase noise measurement technique with a reference clock, and Section 4 discusses the simulation results. Section 5 describes the proposed phase noise measurement technique without a reference clock and Section 6 provides conclusions.

II. DELTA-SIGMA TDC

Fig.1 shows a delta-sigma TDC architecture [8] consisting of a delay element, three multiplexers, an analog integrator (or charge pump circuit), and a comparator. Its inputs are two clock signals CLK1 and CLK2 with the same frequency, and it measures the time difference ΔT of their clock timing edges. In this design, the TDC output as the time difference is positive when the CLK1 rising edge is earlier than CLK2, and it is negative when the CLK1 edge is later. The number of 1's of the comparator output for a given time is proportional to the time difference between CLK1 and CLK2 when CLK1 is earlier. Similarly the number of 0's is proportional to their time difference when CLK2 is earlier.

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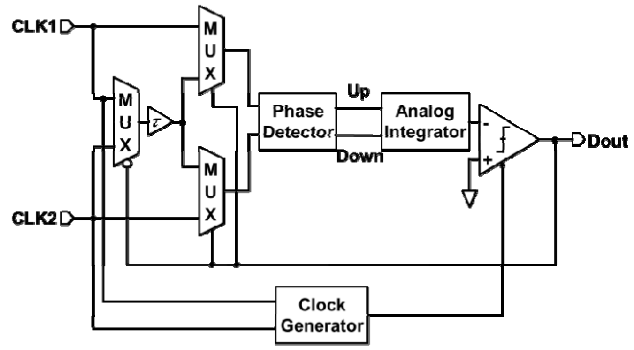
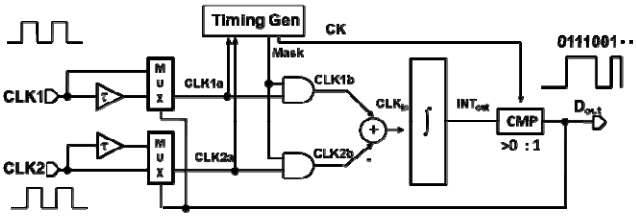


(a) Proposed circuit block diagram.



(b) Matlab simulation model diagram.

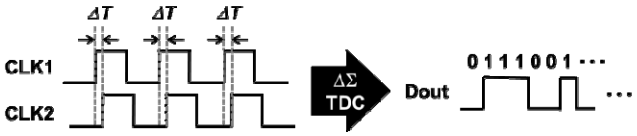


Fig. 1. Block diagram of a delta-sigma TDC.

Its operation is as follows (Fig.2):

(i) When the comparator output is "1", CLK1 is delayed by τ, while CLK2 is not delayed. When the comparator output is "0", CLK1 is not delayed, while CLK2 is delayed by τ.

(ii) The clock signals acquired as a result are defined as CLK1a and CLK2a respectively.

(iii) The mask signal (generated in "Timing Generator") is the same as CLK1a when CLK1a comes earlier than CLK2a; otherwise it is the same as CLK2a.

(iii) CLK1b is the logical AND of the Mask signal and CLK1a, while CLK2b is the logical AND of the Mask signal and CLK2a.

(iv) We generate the signal CLKin representing time delay between CLK1b and CLK2b and convert it to a voltage signal by subtracting CLK1b from CLK2b in the analog domain, and feed it to the integrator whose output is INTout.

(v) The comparator examines (at the rising edge of CLK which is delayed by Td from the falling edge of Mask signal) whether the integrator output INTout is larger than "0" or not. Its output Dout is the delta-sigma TDC signal that is fed-back to the multiplexers.

Fig.3 shows the delta-sigma measurement range of the time difference ΔT of the input clock $-\tau < \Delta T < \tau$. In other words, τ determines the input range, not the time resolution.

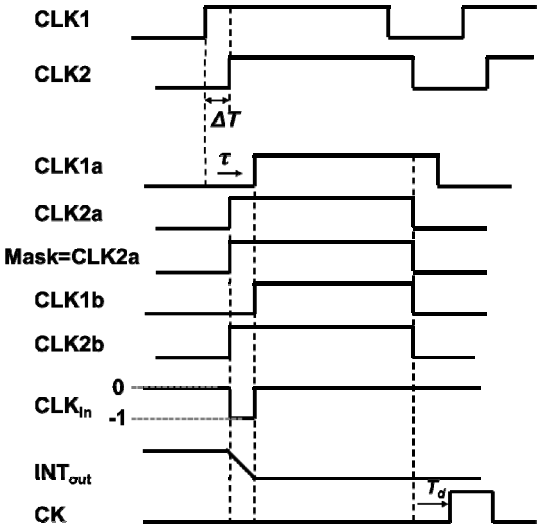


Fig. 2. Timing chart of the delta-sigma TDC in Fig.1 (in case D_{out}=1.)

Notice that the time resolution of the phase noise measurement with the delta-sigma TDC is given by

$$T\_resolution = \frac{2\tau}{N_{DATA}}$$

The time resolution is determined by the delay element τ and the number of obtained TDC output data points N_{DATA}; hence the longer the measurement time, the larger N_{DATA}, and then the finer the time resolution (this is similar to an integrator ADC). This enables to apply the delta-sigma TDC to phase noise measurement.

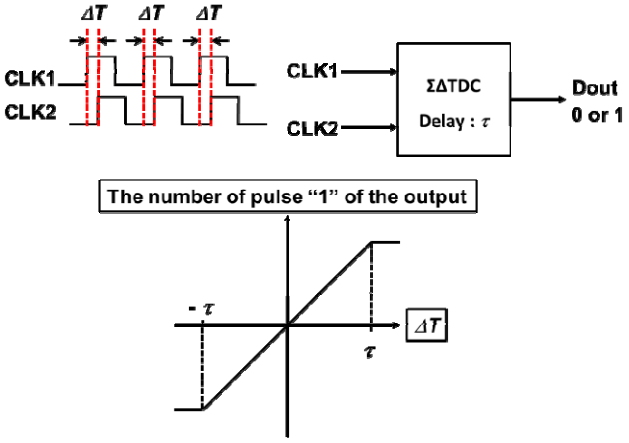


Fig.3. Input-output characteristics of the delta-sigma TDC.

III. PROPOSED PHASE NOISE MEASUREMENT USING DELTA-SIGMA TDC WITH REFERENCE SIGNAL

A. Principle of Phase Noise Measurement

Fig.4 shows the first proposed phase noise measurement principle using the delta-sigma TDC (with a reference clock) [9]. We assume here that

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CLK1 is the clock under test and it may have some phase noise, while CLK2 is a reference clock without phase noise, and also that the frequencies of CLK1 and CLK2 are the same.

Suppose that CLK1 has no phase noise. Then the rising edge timing difference between CLK1 and CLK2 causes only a DC component in the output spectrum of the delta-sigma TDC, because the timing difference is always constant.

On the other hand, when there's finite phase noise in the input clock CLK1, the time difference between CLK1 and CLK2 changes at each clock cycle, and these fluctuation effects appear in the output spectrum of the delta-sigma TDC; based on this, phase noise can be measured.

Note that since noise shaping is applied by delta-sigma modulation, the components of the comparator quantization noise floor rise as their frequencies increase. However, in many cases, the phase noise frequency characteristics close to the carrier frequency are important. The x-axis of Fig.4 below shows the spectrum obtained by FFT of the sigma-delta TDC output. Phase noise is near the carrier (CLK1) frequency; shaped quantization noise is at higher frequencies, and so does not appear to affect the accuracy of phase noise measurement.

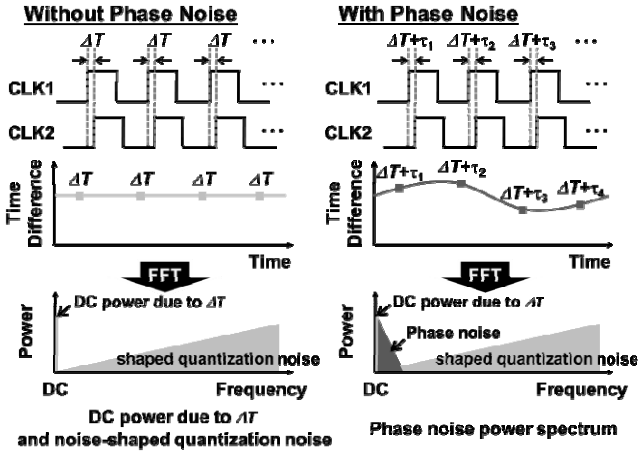

Fig. 4. Principle of the proposed phase noise measurement using a delta-sigma TDC with a reference clock.

B. Analytical Discussion

Fig.5 shows the proposed phase noise measurement system using a delta-sigma TDC. The delta-sigma TDC measures the time difference between CUT (CLK1 with phase noise) and a reference clock REF (CLK2 without phase noise). The phase noise frequency characteristics of CLK1 from the carrier (clock) frequency can be obtained by FFT of the TDC output. Now we derive analytical expressions for the phase noise.

Suppose that CLK1 is approximated by a sinusoidal signal:

$$\mathrm{CUT} \approx \sin\left(2\pi f_{in} t + \phi(t)\right) \quad \ldots\ldots\ldots\ldots \quad (1)$$

Here φ(t) is phase noise expressed in time domain. Let the *m*-th zero-crossing rising edge timing function be *τ(m)*, and we have

$$2\pi f_{in}\left(mT + \tau(m)\right) + \phi(mT) = 2\pi m \quad \ldots\ldots \quad (2)$$

$$\therefore \phi(mT) = -2\pi f_{in}\tau(m) \quad \ldots\ldots \quad (3)$$

Here τ(m) is the m-th zero-crossing timing, and let us consider the case that τ(m) is a sinusoidal input with an angular frequency of ω_1

$$\tau(m) = T \cdot \alpha_1 \cdot \sin(\omega_1 \cdot mT) \quad \ldots\ldots\ldots\ldots \quad (4)$$

Then we have the phase noise in time domain

$$\phi(mT) = -2\pi\alpha_1 \cdot \sin(\omega_1 \cdot mT) \quad \ldots\ldots\ldots \quad (5)$$

Thus its power at ω_1 is given by

$$\Phi(\omega_1) = \frac{1}{2}(2\pi\alpha_1)^2 \quad \ldots\ldots\ldots\ldots \quad (6)$$

Eq. (6) shows that the phase noise power spectrum at ω_j away from the CUT (carrier) frequency.

Next, let us consider the case that phase variation is given by superposition of several sine waves. Let τ(m) be

$$\tau(m) = \sum_{j=1}^{N} T \cdot \alpha_j \cdot \sin\left(\omega_j \cdot mT\right) \quad \ldots\ldots\ldots\ldots \quad (7)$$

Then we have the phase noise in time domain

$$\phi(mT) = -2\pi \sum_{j=1}^{N} \alpha_j \cdot \sin\left(\omega_j \cdot mT\right) \quad \ldots\ldots\ldots \quad (8)$$

Thus its power at ω_j is given by

$$\Phi\left(\omega_j\right) = \frac{1}{2}\left(2\pi\alpha_j\right)^2 \quad \ldots\ldots\ldots\ldots \quad (9)$$

We see that the phase noise power spectrum is obtained by FFT of the delta-sigma TDC outputs.

C. Phase Noise Measurement Simulation

We have confirmed the effectiveness of the proposed method with a reference clock by MATLAB simulation. Fig.5 shows the circuit configuration for the simulation, where the frequency of the input clocks REF and CUT is set to 1MHz. In MATLAB simulation, exact phase variation of the input clock CUT (CLK1) is applied using VTD (Variable Time Delay, which is one of MATLAB functions), while CLK2 has no phase noise. Delay τ in the delta-sigma TDC is set to 200ns, and the number of the delta-sigma TDC data we use is 4,096. Table I shows simulation conditions. We have conducted simulations for phase variation both for single sine wave and several superposed sine waves.

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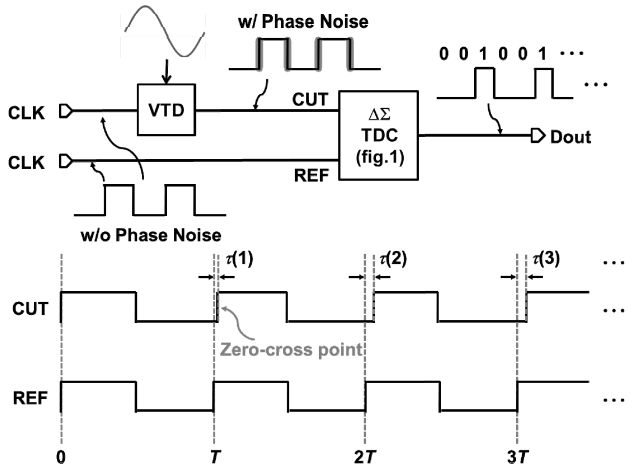

Fig. 5. Phase noise measurement system using the delta-sigma TDC and zero-cross variation function $\tau(m)$.

1) In Case of Single Sine Wave Phase Fluctuation

We have conducted MATLAB simulations with phase variation of single sine waves of 10kHz and 50kHz.

a) Phase variation of 10kHz

Fig.6 shows the FFT analysis results of the delta-sigma TDC output data without and with phase noise of 10kHz (in eq.(4), $\omega_1/(2\pi)$=10kHz). We see in Fig.6 that the spurious component appears at 10kHz.

b) Phase variation of 50kHz

Fig.7 shows the FFT analysis results of the delta-sigma TDC output data with phase noise of 50kHz (in eq.(4), $\omega_1/(2\pi)$=50kHz). We see in Fig.7 that the spurious component appears at 50kHz.

2) In Case of Superposition of Two Sine Waves of Phase Fluctuation

We have also performed MATLAB simulation of the phase fluctuation of CUT when two sine waves are superimposed (in eq.(8), N=2, $\omega_1/(2\pi)$=10kHz, $\omega_2/(2\pi)$=50kHz). Fig.8 shows simulation results, and we see that the spurious components appear at the frequencies of 10kHz and 50kHz. Consequently, even if the CUT contains multiple phase fluctuation components, the proposed method can measure their frequency components.

We have compared the simulation results in this section and analytical results in Section 3-2, and found that both agree well.

IV. Proposed phase noise measurement using delta-sigma TDC without reference signal

A. Principle of Phase Noise Measurement

Fig.9 shows the second proposed phase noise measurement principle using the delta-sigma TDC (without a reference clock). CLK is the clock under

TABLE I .SIMULATION CONDITIONS

Simulation condition of phase variation	
1. Single sinusoidal wave	2. Sinusoidal Synthesis
$\tau(m) = T \cdot \alpha_j \cdot \sin(\omega_j \cdot mT)$ ... (4)	$\tau(m) = \sum_{j=1}^{z} T \cdot \alpha_j \cdot sin(\omega_j \cdot mT)$ ... (7)
$T \cdot \alpha_j = 100\ [ns]$	$T \cdot \alpha_1 = T \cdot \alpha_2 = 50\ [ns]$
$f_j = \frac{\omega_j}{2\pi} = 10$ [kHz]	$f_1 = \frac{\omega_1}{2\pi} = 10$ [kHz]
	$f_2 = \frac{\omega_2}{2\pi} = 50$ [kHz]

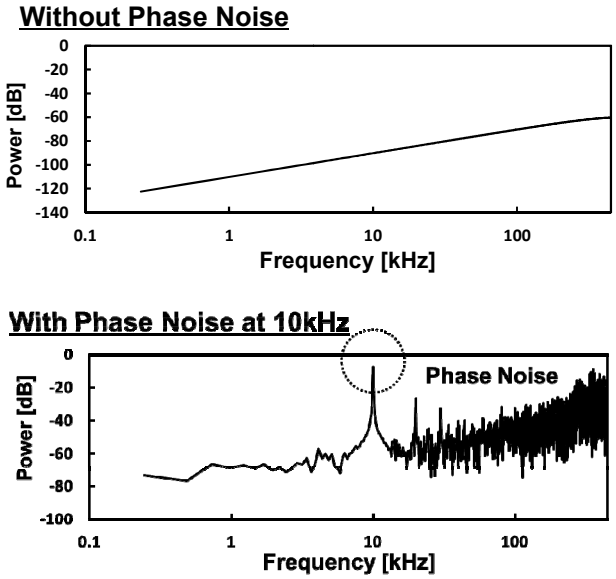

Fig. 6. Power spectrum of the delta-sigma TDC output (MATLAB simulation)

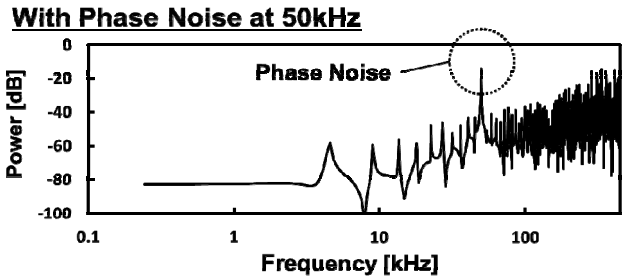

Fig. 7. Power spectrum of the delta-sigma TDC output (MATLAB simulation).

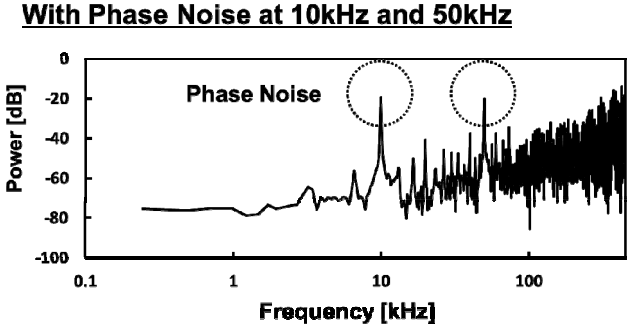

Fig. 8. Power spectrum of the delta-sigma TDC output. (MATLAB simulation).

test, which may have some phase noise, and it is delayed by βT. Here T is the clock period, and β is required to be approximately one (exactly one or an integer is not necessary) and hence it is relatively easy to implement.

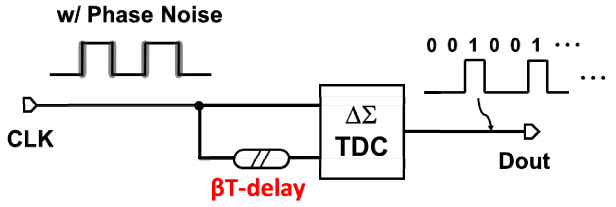

Fig.9 Proposed phase noise measurement using delta-sigma TDC without reference clock.

The proposed system can measure period jitter of CLK (Fig.10). We can obtain the phase noise power spectrum by multiplying the power spectrum of the period jitter obtained by FFT of the delta-sigma TDC output by $1/\omega^2$ (see Fig.10 [1] and Fig. 11).

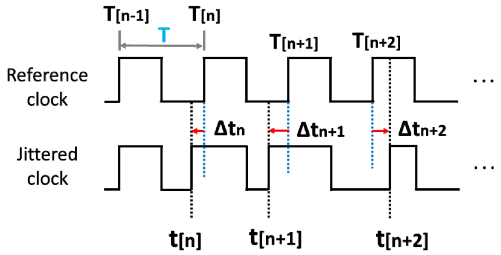

Fig. 10 Explanation of period jitter [1].

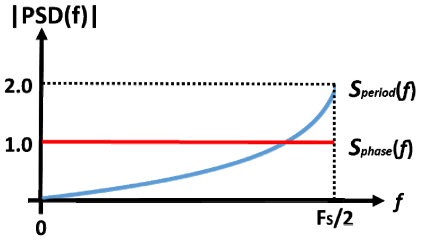

Fig.11 Power spectrum of period jitter and phase noise [1].

B. Analytical Discussion

We derive analytical expressions for the phase noise in Fig.9. Suppose that CLK is approximated by a sinusoidal signal.

$$\text{CUT} \approx \sin\left(2\pi f_{in} t + \phi(t)\right) \quad \ldots\ldots\ldots\ldots \quad (10)$$

Here φ(t) is phase noise expressed in time domain. Let the *m*-th zero-crossing rising edge timing function be *τ(m)*, and we have

$$2\pi f_{in}\left(mT + \tau(m)\right) + \phi(mT) = 2\pi m \quad \ldots\ldots \quad (11)$$

$$\therefore \phi(mT) = -2\pi f_{in}\tau(m). \quad \ldots\ldots \quad (12)$$

Here τ(m) is the m-th zero-crossing timing, and let us consider the case that τ(m) is a sinusoidal input with an angular frequency of ω_1.

$$\tau(m) = T \cdot \alpha_1 \cdot \sin(\omega_1 \cdot mT) \quad \ldots\ldots\ldots\ldots \quad (13)$$

The delta-sigma TDC in Fig.9 measures the time

$$\tau(m+1) - \tau(m) + (\beta - 1)\text{T}$$

$$= T \cdot \alpha_1[\sin(\omega_1 (m+1)T) - \sin(\omega_1 \cdot mT)] + (\beta - 1)\text{T}$$

$$= 2T \cdot \alpha_1 \sin(\omega_1 T/2)\cos(\omega_1 (m+1/2)T) + (\beta - 1)\text{T} \quad \ldots..(14)$$

Here $(\beta - 1)$T is DC component.

$2\sin(\omega_1 T/2)\cos(\omega_1(\text{m}+1/2)\text{T})$ is the frequency component at ω_1 and its corresponding power of $\phi(mT)$ at ω_1 is

$$\Phi'(\omega_1) = \frac{1}{2}(2\pi\alpha_1)^2 [2\sin(\omega_1 T/2)]^2 \quad \ldots\ldots\ldots \quad (16)$$

Then we have the phase noise power atω_1 as follows:

$$\Phi(\omega_1) = \frac{\Phi'(\omega_1)}{[2\sin(\omega_1 T/2)]^2} \quad \ldots\ldots\ldots\ldots \quad (17)$$

Assumption: ω_1 is much lower than$2\pi f_{in}$. This is reasonable in many applications, such as wireless communications, because the oscillator frequency is very high, but attention must be paid only to the phase noise characteristics close to the oscillator frequency. When the above assumption is valid, we have $\omega_1 T/2$ <<1.Then we have $2\sin\left(\frac{\omega_1 T}{2}\right) \cong \omega_1 T$ and the phase noise power is

$$\Phi(\omega_1) \cong \frac{\Phi'(\omega_1)}{{\omega_1}^2 T^2} \quad \ldots\ldots\ldots\ldots \quad (18)$$

We have similar equations when the phase noise results from superposition of several sinusoidal signals.

Remark:

(i)The requirement for β is to be approximately one; It is easy to implement, and noise addition in βT is small. Other self-reference clock jitter/phase noise measurement methods such as in [5,6] require exactness or an integer greater than one for β, which is difficult to implement, and the noise addition in βT is relatively large.

(ii) The deviation of β from one only appears as a DC component in the frequency domain after FFT of the delta-sigma TDC output.

(iii) Note that since noise shaping is applied by delta-sigma modulation, the components of the comparator quantization noise floor rise as their frequencies increase. However in this case we obtain the phase noise power spectrum by multiplying the power spectrum of the period jitter obtained by FFT of the delta-sigma TDC output by $1/\omega^2$; hence noise-shaped quantization noise at high-frequencies is also suppressed.

C. Phase Noise Measurement Simulation

We have confirmed the effectiveness of the second

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proposed method (without a reference clock) by MATLAB simulation in Fig.9, where the input clock frequency is set to 1MHz. Figs.12 (a), (b), (c) show the simulation results with the same amount of phase variation at 1kHz, 10kHz and 100kHz respectively; we see that as the frequency of the phase noise increases, the corresponding TDC output power spectrum increases. Fig. 13 shows simulation results and theoretical analysis in eq.(17) for the phase variation versus corresponding TDC output power, and we see that both agree well.

V. Conclusion

We have proposed two techniques—with and without a reference clock—for measuring phase noise of a clock using a delta-sigma TDC, and we have verified their effectiveness by MATLAB simulations. We have also derived analytical formula for phase noise measurement with the proposed method, which agree the simulation results well. The proposed techniques enable low-cost high-quality phase noise measurement without requiring high-performance spectrum analyzers. Some concluding remarks:

(i) Measurement of oscillator phase noise due to 1/f noise is difficult with a spectrum analyzer because the 1/f noise effect appears at the frequency close to the oscillation frequency. However the proposed methods here can measure it accurately

(ii) A multi-bit sigma-delta TDC with linearization techniques can further reduce the phase noise measurement time [8].

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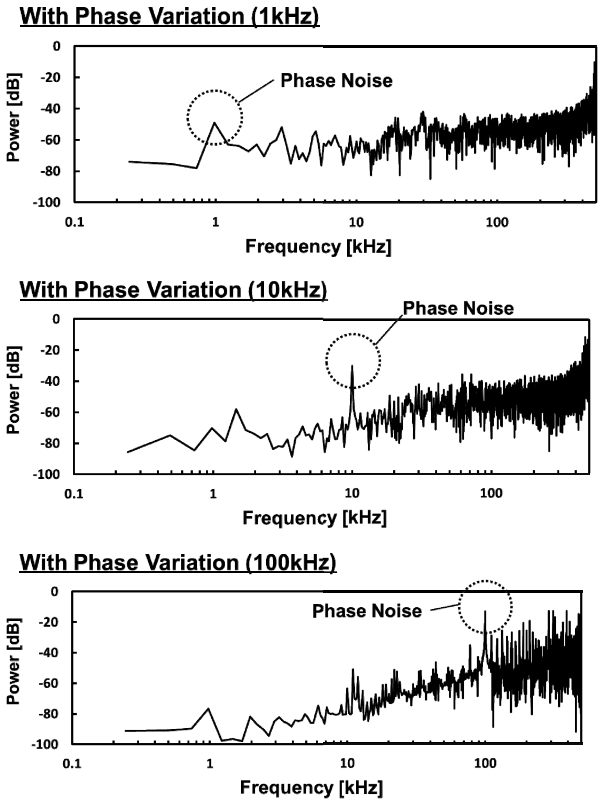

Fig.12 MATLAB simulation results of phase noise measurement without a reference clock (delta-sigma TDC output power spectrum).

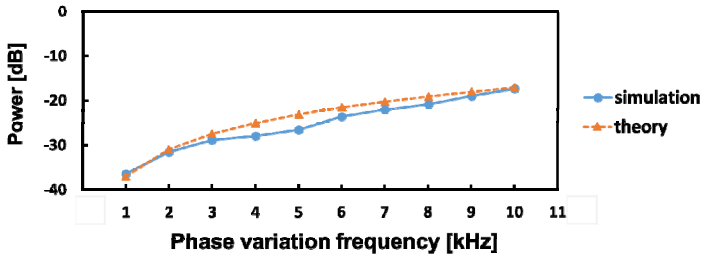

Fig.13 MATLAB simulation results and theoretical analysis of TDC output power versus phase variation frequency with the proposed phase noise measurement technique without a reference clock.

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