

Study of High Precision IGBT Macro-Model Considering Temperature Dependency

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Abstract—In this study, a novel SPICE model of an Insulated-Gate-Bipolar-Transistor (IGBT), which is often used to handle high power signals in automotive electrical circuits, has been developed. The model consists of basic SPICE elements. Thus, it can be used in any SPICE-compatible simulators without any source code modifications. This paper reports the results of drain current characteristics considering the temperature dependence by using the proposed IGBT macro-model for SPICE.

Keywords— Insulated Gate Bipolar Transistor, IGBT, SPICE, Macro Model)

I. INTRODUCTION

Insulated Gate Bipolar Transistor (IGBT) is suitable for high-voltage and large current applications. Because IGBT is voltage-controlled device with the insulated gate, it is mainly applied for high voltage semiconductor elements for car electronic systems. IGBT models for circuit simulations have been implemented in any standard SPICE libraries [1]. However, existing SPICE models are not so accurate to simulate IGBT device behavior comparing with actual measurements. Therefore, model improvements are necessary to apply them for practical circuit design.

Our study is to develop the SPICE IGBT macro-model by high voltage semiconductor elements for car electronic systems. An IGBT model for circuit simulations has been developed as a SPICE sub-circuit. The model consists of basic SPICE elements to improve accuracies without any source code modifications. Hence, it can be used in any SPICE-compatible simulators.

This paper reports the results of drain current static characteristic considering the temperature dependence by using the proposed IGBT macro-model for SPICE simulators.

II. BASIC PRINCIPLES OF IGBT

A. Typical structure of IGBT

IGBT is the structure of power MOSFET (DMOS transistor) by appending the high diffusion rate p-layer. Fig. 1 [2] shows the device structure of IGBT. When enough voltage is applied to the gate under forward bias between anode and cathode terminals condition, an inversion layer is formed in p-layer to the vicinity of the gate electrode. Current flows the n- layer through the inversion layer, and holes are injected toward the n⁻ layer from the p-layer. This hole moves the n⁻ layer which is

basically the drift layer by diffusion, and the part of them are recombined with electrons which passing through the drift layer. Remained holes flow into the p-layer through the junction. In other words, conduction has been made between the anode and the cathode. It can be seen that this is an on-state pnp bipolar transistor, whose p⁺ layer is the emitter of the hall, p-layer is the collector (cathode), and n-layer is the base (gate).

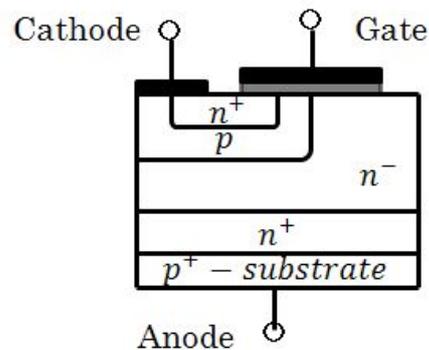


Fig. 1. Simplified structure of IGBT

B. The static characteristics of the IGBT

Fig.2 shows static DC output characteristics of IGBT [2].

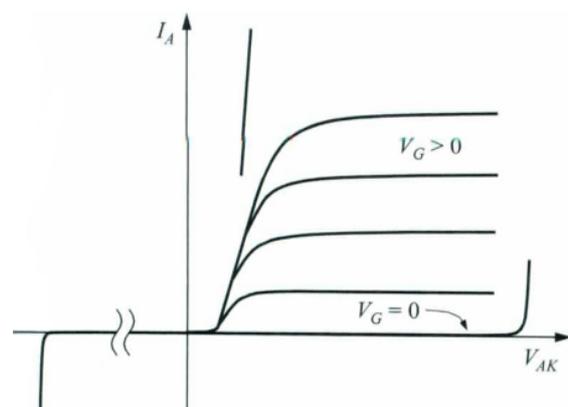


Fig. 2. Static DC output characteristics of IGBT [2]

When V_{AK} is smaller than 0.7V, equivalent circuit is the DMOS transistor in the series with p-i-n diode as shown in Fig. 3 (a). When a small voltage is applied to the DMOS transistor, conduction current of p-i-n diode flows under the forward bias by recombination of excess electrons and holes.

When V_{AK} is greater than 0.7V, it cannot be completely absorbed excess hole injection from the anode terminal. They spill out from the p-area, and contribute to the current of the bipolar transistor. The equivalent circuit at the moment is shown in Fig. 4 (b). Drain current of DMOS (I_{MOS}) becomes base current, then, anode current becomes emitter current. The equation of the current is shown in the following table [1];

$$I_A \approx (1 + \beta_{pnp})I_{MOS} \quad (1)$$

$$\beta = \frac{\alpha}{1 - \alpha} \quad (2)$$

$$\alpha \approx \alpha_T \approx \frac{1}{\text{csch}(x_{nn}/L_n)} \quad (3)$$

Here, α_T is transport factor of base and x_{nn} is neutral base.

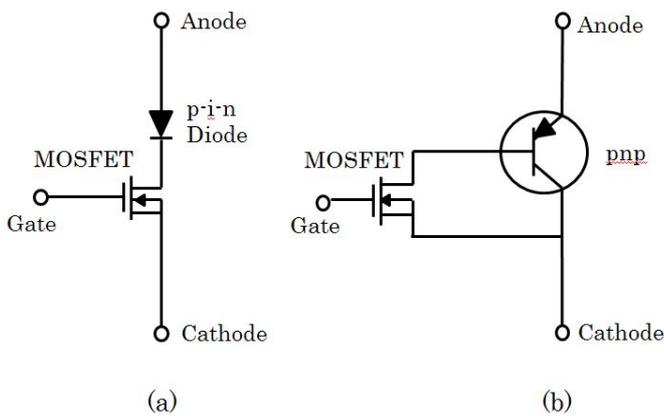


Fig. 3. Equivalent circuits of an IGBT
(a) $V_{AK} < 0.7$ V, (b) $V_{AK} > 0.7$ V.

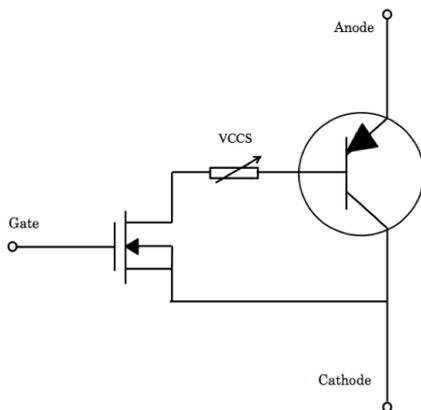


Fig. 4. Conventional IGBT macro-model

C. Conventional IGBT Macro-model

The important feature to use macro-models is the ability to create a new device models without source code modifications of SPICE. Another advantage is their high versatility because they can be used in many SPICE simulators. Fig. 4 shows a conventional IGBT macro-model. This model uses UCB MOSFET level 3 model as MOSFET's and SPICE Gummel-Poon model as pnp bipolar transistor's. Then, a Voltage Controlled Current Source (VCCS) represents the variable resistance, which is caused by the n-epi-layer of drain of MOSFET. This macro-model has the following disadvantages,

- 1) It is not possible to model the drift current through the n-layer.
- 2) The DMOS output resistance becomes constant.
- 3) It cannot simulate the characteristics of free-wheel diodes.

Simulation results of the conventional macro-model [3] are shown in Fig. 5.

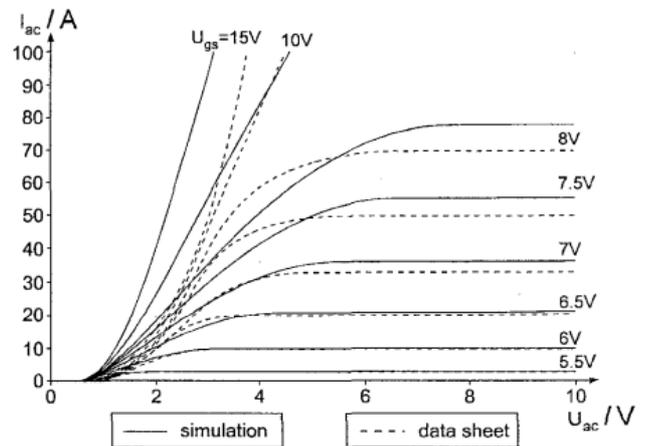


Fig. 5. Anode DC current comparison of the conventional IGBT model [3]

The result shows that the simulation accuracy of the static DC output characteristics is not enough to use it for any circuit designs. We would like to propose a macro-model of IGBT (named as A-IGBT model) to improve the accuracy of static simulations, which includes IGBT itself, and free-wheel diodes.

III. MACRO-MODEL DEVELOPMENT

A-IGBT model is shown in Fig. 6 [4]. Two pn diodes are connected in parallel, in addition to the equivalent circuit of conventional IGBT. These pn diodes are applied to control the backward breakdown voltage of the n⁻ layer and to simulate the forward current characteristic of the free-wheel diode. Other role is to represent turn-off transient simulations operated by junction capacitances of pn diodes. By connecting two different pn junction diode models in parallel, the parameters of each diode can be set, independently. Thus, they increase the flexibility of the slope

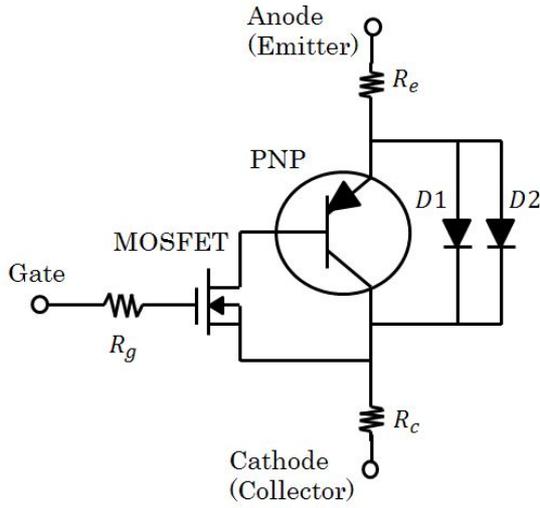


Fig. 6. Proposed IGBT macro model (A-IGBT)

at current-voltage characteristic curve. In addition, we use the BSIM4 model to simulate the DMOS characteristics. To represent the carrier mobility behavior, UCBMOS level 3 supports linear mobility reduction with an analytical equation whose number of parameters is only one. BSIM4 supports four kind of mobility equation options to represent vertical and horizontal fields effects. Thus, it is possible to more accurately represent the current drift model for the model. Moreover, saturation region model of BSIM4 can be classified into three regions of the channel length modulation effect, DIBL (Drain Induced Barrier Lowering) effect and the hot electron effect the output resistance. Therefore, the output resistance can be accurately represented by BSIM4. Although A-IGBT model has a very simple equivalent circuit, it is suitable for the device operation mechanisms.

To explain the model equation of the Carrier mobility and the output resistance in BSIM4 [5], model parameter is shown in table I .

TABLE I. BSIM4 MODEL PARAMETERS RELATED TO CARREIER MOBILITY AND OUTPUT RESISTANCE

Parameter Name	Description
TOX	Gate oxide thickness
$U0$	Carrier mobility
UA	First order factor of mobility degradation
UB	Second order factor of mobility degradation
UC	Substrate effect factor of mobility degradation
UD	Coulomb scattering mobility degradation factor
$TOXE$	Electrical gate oxide thickness
V_t	Thermal voltage

V_{gsteff}	Smoothing function to the gate bias
P_{CLM}	Channel length modulation parameter
P_{DIBLCB}	Body bias coefficient of DIBL effect on Rout
A_{bulk}	Substrate charge effect
P_{VAG}	Gate depending parameter of early voltage
L_{eff}	Effective channel length
D_{ROUT}	Channel-length dependence of DIBL effect on Rout
P_{SCBE1}	First substrate current induced body-effect parameter
P_{SCBE2}	Second substrate current induced body-effect parameter
NF	Number of gate fingers

Carrier mobility in BSIM4 is modeled based on the electric field in the vertical direction. Carriers affected by the effective electric field (E_{eff}) in the inversion layer are shown in the following equations ;

$$E_{eff} = \frac{Q_B + \frac{Q_{inv}}{2}}{\epsilon_{si}} \quad (4)$$

Here, Q_B is substrate charge, Q_{inv} is inversion charge and ϵ_{sv} is silicon permittivity. This equation can be written by the model parameters and the voltage as

$$E_{eff} \cong \frac{V_{gs} + V_{th}}{6TOX} \quad (5)$$

Where, V_{gs} is gate source voltage, and V_{th} is threshold voltage. The effective carrier mobility (μ_{eff}) and effective electric field are associated as follows;

$$\mu_{eff} = \frac{\mu_0}{1 + \left(\frac{E_{eff}}{E_0}\right)^v} \quad (6)$$

Where, v is a coefficient of the electric field ratio. This equation derives as a quadratic equation by series expansion as

$$\mu_{eff} = \frac{\mu_0}{1 + A\left(\frac{E_{eff}}{E_0}\right) + B\left(\frac{E_{eff}}{E_0}\right)^2} \quad (7)$$

Where, A and B are the constants that occur in the series expansion. The following equation is obtained by substituting (7) to (5) as

$$\mu_{eff} = \frac{\mu_0}{1 + A\left(\frac{V_{gs} + V_{th}}{6TOX \cdot E_0}\right) + B\left(\frac{V_{gs} + V_{th}}{6TOX \cdot E_0}\right)^2} \quad (8)$$

Considering of the bias and channel length dependences, it can be expressed by following equation;

$$\mu_{eff} = \frac{U_0 \cdot f(L_{eff})}{1 + [UA\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right) + UB\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)^2] \dots} \dots \frac{1}{(1 + UC \cdot V_{bseff}) + UD\left(\frac{V_{th} \cdot TOXE}{V_{gsteff} + 2V_{th}}\right)^2} \quad (9)$$

Here, V_{bseff} is effective substrate voltage. As the output resistance (R_{ds}) is coupled to the drain current in three areas, the model of drain current includes the output resistance characteristics. Drain current equation is shown as

$$I_{ds} = I_{dsat} + \frac{\partial I_{ds}}{\partial V_{ds}}(V_{ds} - V_{dsat}) \quad (10)$$

$$\begin{aligned} I_{ds} &= I_{dsat} + \left[\left(\frac{I_{dsat}}{V_A}\right)(V_{ds} - V_{dsat})\right] \\ &= I_{dsat} \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right) \end{aligned} \quad (11)$$

In order to ensure continuity, the model equation of the gate bias (V_{dsx}) is written as

$$I_{ds} = I_{dsat} \left(1 + \frac{V_{ds} - V_{dsx}}{V_A}\right) \quad (12)$$

Also, it shows the early voltage in three regions. The equation of the early voltage in channel length modulation region (V_{ACLM}) is shown as

$$V_{ACLM} = C_{cml} \cdot (V_{ds} - V_{dsat}) \quad (13)$$

The early voltage in DIBL region (V_{ADIBL}) is shown as

$$\begin{aligned} V_{ADIBL} &= \frac{V_{gsteff} + 2v_t}{\theta_{rout}(1 + PDIBLCB \cdot V_{bseff})} \\ &\left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t}\right) \left(1 + \frac{PVAG \cdot V_{gsteff}}{E_{sat} L_{eff}}\right) \end{aligned} \quad (14)$$

The early voltage in substrate current induced body bias effect (SCBE) region (V_{SCBE}) is shown as

$$V_{ASCBE} = \frac{L_{eff}}{PSCBE2} \exp\left(\frac{PSCBE1 \cdot l_{itl}}{V_{ds} - V_{dsat}}\right) \quad (15)$$

As a result, The drain current including the output resistance model (I_{ds}) is shown in the following equations ;

$$\begin{aligned} I_{ds} &= \frac{I_{dso} \cdot NF}{1 + \frac{R_{ds} \cdot I_{ds0}}{V_{dseff}}} \left[1 + \frac{1}{C_{clm} \log e \left(\frac{V_A}{V_{Asat}}\right)}\right] \\ &\left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADIBL}}\right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ADITS}}\right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right) \end{aligned} \quad (16)$$

Where, early voltages and V_{Asat} are shown in the following equations;

$$V_A = V_{Asat} + V_{ACLM} \quad (17)$$

$$\begin{aligned} V_{Asat} &= \frac{E_{sat} L_{eff} + V_{dsat}}{R_{ds} v_{sat} C_{oxe} W_{eff} A_{bulk}^{-1} + \frac{2}{\lambda}} \dots \\ &\dots \frac{1}{+ 2R_{ds} v_{sat} C_{oxe} W_{eff} V_{gsteff} \left[1 - \frac{A_{bulk} V_{dsat}}{2(V_{gsteff} + 2v_t)}\right]} \end{aligned} \quad (18)$$

Here, v_{sat} is the saturation velocity.

IV. MODEL PARAMETER EXTRACTIONS AND SIMULATIONS

In this study, we digitized DC current-voltage characteristics of IGBT from datasheets of IGBT module, MBN1200E33E, made by HITACHI. Circuit diagram of MBN1200E33E is shown fig. 7. Where, collector-to-emitter voltage (V_{CES}) is 3300V, gate-to-emitter voltage (G_{GES}) is $\pm 20V$, collector current (I_C) is 1200A, and forward current (I_F) is 1200A.

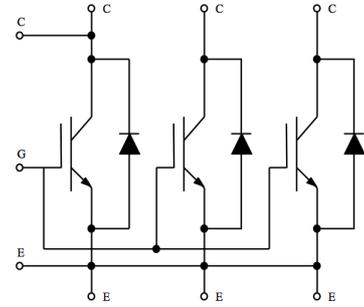


Fig. 7. Circuit diagram of IGBT MODULE

Proposed IGBT macro-model is implemented in SPICE. Most parameters of BSIM4 model, Gummel-Poon model, and PN diode models have been extracted and optimized by using a general optimization program. Physical model parameters are calculated with measured data. Fitting parameters used to express secondary effects are left as initial values.

Temperature dependencies of the BSIM4 model are discussed as follows. To derive drain current equations dependent on ambient temperature in BSIM4 model, mobility and saturation velocity include temperature terms. They are shown in eq. (19) and (20) [6],

$$UX(T) = UX(TNOM) + UX1 \cdot (T/TNOM - 1) \quad (19)$$

$$VSAT(T) = VSAT(TNOM) - AT \cdot (T/TNOM - 1) \quad (20)$$

Here, $TNOM$ is the temperature that the measurement for parameter extraction was performed. UX is the temperature coefficient of the parameter and AT is the temperature coefficient of the carrier velocity saturation.

We have changed the static characteristics of the IGBT to follow even at high temperatures by tuning the parameters of temperature effects in BSIM4. The X in UX and $UX1$ should be replaced by A , B , and C to read them for mobility parameters that are listed in table 1. $UX1$ is the temperature

coefficient of the parameter UX . These temperature parameters have been extracted and optimized with drain current measurements dependent on drain and gate voltages in linear and saturation regions at 25 and 125 Celsius. Parameters related to mobility and saturation velocity are shown in table I and II.

TABLE II. BSIM4 MODEL PARAMETERS RELATED TO TEMPERATURE DEPENDENCE ON MOBILITY

Parameter Name	Value
$U0$	400 [m/V]
UA	2.29×10^{-9} [m/V]
UB	5.87×10^{-19} [m ² /V ²]
UC	0 [m/V ²]
UAI	10.0×10^{-9} [m/V]
UBI	-2.61×10^{-18} [m ² /V ²]
UCI	-40.0×10^{-12} [m ² /V ²]

TABLE III. BSIM4 MODEL PARAMETERS RELATED TO TEMPERATURE DEPENDENCE OF SATURATION VELOCITY

Parameter Name	Value
$VSAT$	8.00×10^4 [m/s]
AT	2.30×10^4 [m/s]

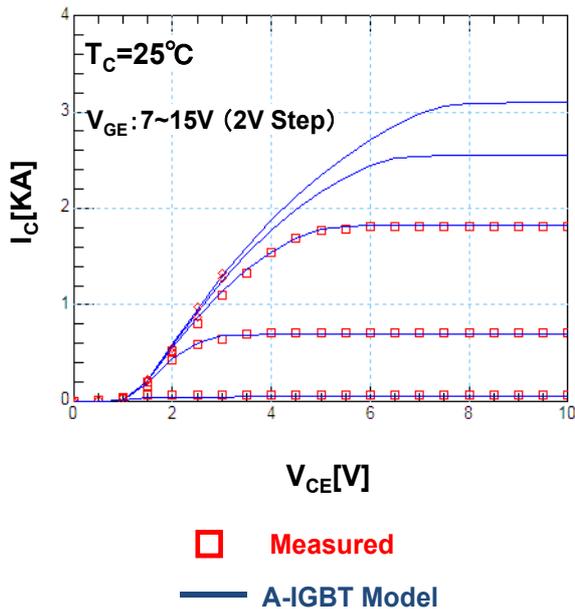


Fig. 8. Comparison between measured from Datasheet and simulated collector-emitter currents of an IGBT ($T_c=25^\circ\text{C}$)

Fig. 8. is the V_{CE} - I_C characteristics to compare A-IGBT model with measured data at $T_c=25^\circ\text{C}$. Although measured data from the datasheets showed up to 2KA, we simulated up to 3KA to verify the plausibility of the A-IGBT model. Thus, we

guarantee the linearity of the simulation. It can be seen that A-IGBT model represent the collector current characteristic accurately from Fig. 8. In comparison with Fig.5, it is possible to obtain accurate simulations in the saturation and the linear region. Especially, gate resistance dependency of V_{CE} , which appeared to be the gain compression between curves whereas the conventional model could not be represented, is accurately simulated.

Fig. 9 is the I_C - V_{CE} characterization compared A-IGBT model with measured data at $T_c=125^\circ\text{C}$. As shown in fig. 9, A-IGBT model successfully reproduces collector current even in higher temperature. It is evidence that the model can be satisfactory applied for static current simulations.

Fig. 10 shows measurement and simulation results of forward current characteristic of free-wheel diode. Free-wheel diode is important elements of IGBT. There is a role to eject the electromotive force of the coil load to be used in high current circuits. As shown in Fig. 10, the forward current is accurately simulated with the A-IGBT model. Resistance of the diode is larger than that of PN diodes with small geometry, which is appeared to be the gentle curve from medium to high injection region. Since our model uses two different grading coefficients, NF, for optimizations, the excellent agreement with measurement has been obtained.

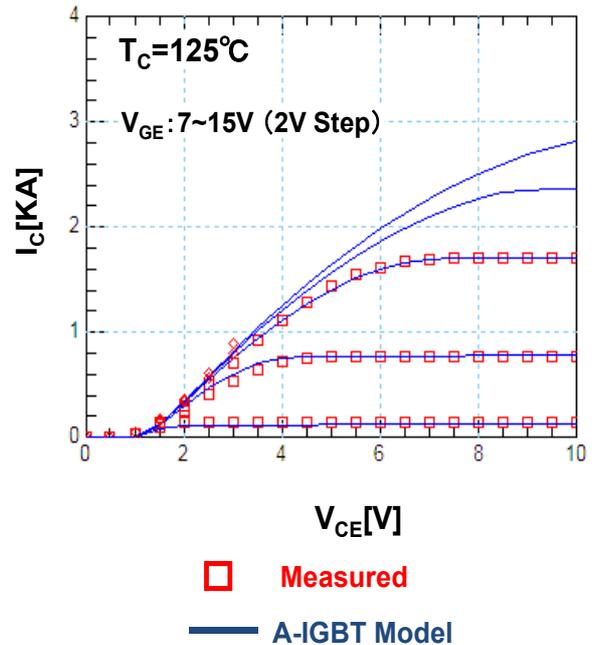
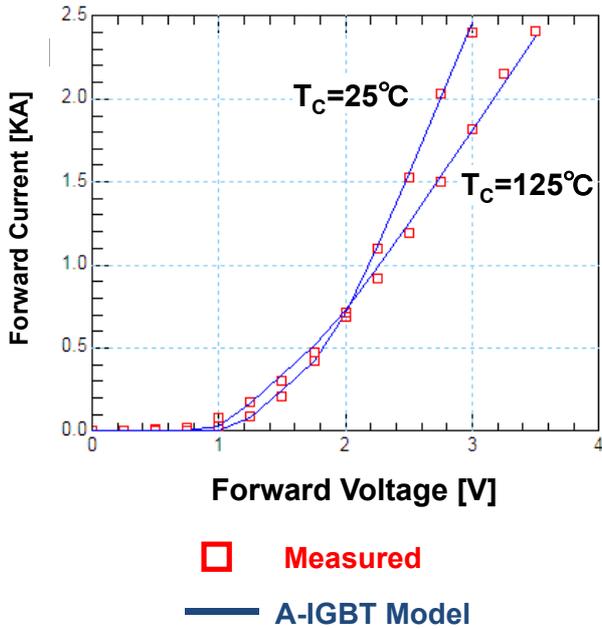


Fig. 9. Comparison between measured from Datasheet and simulated collector-emitter currents of an IGBT ($T_c=125^\circ\text{C}$)



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Fig. 10. Measurement from Datasheet and simulation results of forward current of free-wheel diode

V. CONCLUSION

This paper proposed a new IGBT macro-model for SPICE simulators and extractions of the high precision model parameters by using the DC I-V measurements. BSIM4 model is applied for the core DMOS structure to represent the drift current and output resistance models, accurately. Simulation results with the proposed macro-model represent the static characteristics, accurately. In addition, this simulation can be accurately represented static characteristics of the IGBT at high temperature by extracting model parameters of temperature effects related to mobility and saturation velocity. We are going to continue to develop the capacitance model of IGBT, then, complete our A-IGBT model by verifying the switching characteristics.

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