BSIM4 Modeling of 90nm n-MOSFET Characteristics Degradation Due to Hot Electron Injection

Takuya Totsuka*, Hitoshi Aoki, Fumitaka Abe, Khatami Ramin, Yukiko Arai,
Shunichiro Todoroki, Masaki Kazumi, Wang Taifeng, Haruo Kobayashi, (Gunma University)

Abstract- The final purpose of this study is to model the drain current and 1/f noise degradation characteristics of n-channel MOSFETs. In this report, we present the implementation of hot carrier degradation into drain current equations of BSIM4 model. Then, we show simulation results of the DC drain current degradation, and also 1/f noise voltage density simulation results affected by the drain current degradation. We have extracted BSIM4 model parameters extensively with the measured data including I-V and 1/f noise measurement of our TEGs.

Keywords— MOSFET, Modeling, Hot Electron, 1/f noise, degradation, BSIM4

1. Introduction

The ultimate goal of this study is to develop a “reliability model of 1/f noise and thermal noise for n-channel MOSFETs” used for circuit simulations. 1/f noise is mainly generated in the active elements including MOSFETs, bipolar transistors, and diodes. In particular, 1/f noise is dominant at lower frequencies. It has been known that 1/f noise is induced by the interface state density. Since interfacial trap occurs in the weak to medium inversion region in MOSFETs, it does not affect DC current parameters at high currents in saturation region.

In order to develop the time and temperature degradations of 1/f noise model, DC bias dependencies on these degradations should be analyzed and modeled in advance. It is also evident from the fact that drain current terms are included in any 1/f noise models [2], [3]. There are two major effects in the time and temperature degradations of n-channel MOSFETs. One is the Positive Bias Temperature Instability (PBTI), which arises from positive voltage stress for a long time. The other is the Hot Carrier Injection (HCI), which arises from high drain currents in saturation region. We focus on HCI phenomenon for our characterizations because it is more dominant than PBTI especially in analog circuit design.

In this study, our goal is to implement HCI phenomenon into the n-channel MOSFET model in our SPICE (MDW-SPICE) circuit simulator for circuit designers to simulate DC and 1/f noise characteristics with and without the effect of degradations.The MOSFET model that we adopted for implementing the degradation equations is BSIM4 model [4].

The HCI effect model [5] was first introduced by Professor Hu at University California, Berkeley (UCB). Later on, advanced HCI model [6] which is based on the same theory as [5] was announced. However, it is intended to consider the different analytical methods and to support advanced CMOS technology. This HCI model is developed by calculating the Interface Trap Number and also have done by derivation of carrier mobilities.

We will use the advanced HCI model [6] equations in this research. Time and temperature dependent degradations in DC are implemented in BSIM4 model parameters to simulate HCI phenomenon on SPICE. We will demonstrate to predict the degradations in DC characteristics with and without our implementations. Also, an 1/f noise simulation, which is affected by time and temperature degradations in DC, is presented.

2. HCI induced degradation analysis

HCI is one of deterioration phenomena which is gradually changed characteristic of the transistor. Carriers with energy are accelerated by the high electric field in the MOSFET is trapped into the gate insulating film. Carriers will be the hot carrier that having large energy. It crosses the potential barrier that exists between the Si substrate and gate oxide film. This hot carrier forms space charge which is injected or trapped in the gate oxide film. Then, it will degrade over time characteristics such as transconductance and threshold voltage of the MOSFET. They degrade the characteristics of semiconductor devices. At this time, carriers injected was not trapped which will be the gate current. Carriers flowing into the substrate are observed as a substrate current. Currently, the mechanism of 1/f noise generation has not yet been clarified. It is described as a fluctuation of carrier concentration and fluctuation of mobility in the surface channel region. The smaller the gate channel length of the device becomes large 1 / f noise. The shorter channel length makes the unnecessary electrons more than longer channel. If the device is miniaturized without low voltage power supply voltages, the electric field strength of the internal elements is increased, thus electric field strength near the drain is increased. It leads to HCI. As a result, the carrier is easily trapped in the interface of gate surface. This phenomenon is similar with 1/f noise generation mechanism. It is thought that the 1/f noise is affected by HCI. Therefore, HCI induced 1/f noise model should be considered.

Equations of time and temperature degradations in DC [6] are based on CMOS 0.25μm CMOS process. This model is called the Reaction Diffusion (RD) model that is developed by Alam and Kufluoglu 2004 [7].The RD model can be modeled the hot carrier effect generated near the drain of the transistor before restoration. RD model represents the generation of hydrogen diffusion of particles near the junction of the gate and channel/oxide interface. Using the RD model, hydrogen reaction equation in the interface trap number and the channel/oxide interface can be represented as follows.

$$N_{H(0)}N_{it} \approx \frac{k_F}{k_R}N_0 \quad (1)$$

$N_{H(0)}$ is the initial value of the hydrogen concentration on the interface. N_{it} is the number of interface trap. k_F is the oxide-field-dependent forward dissociation rate constant. k_R is the annealing rate constant. N_0 is the initial number of unbroken Si-H bonds.

$$N_{H_x} = k_H {N_H}^{n_x} \quad (2)$$

N_H is the concentration of hydrogen particles per volume. k_H is a reaction constant. n_x is the number of hydrogen atoms per hydrogen particles. The number of interface traps can be calculated by integrating the number of broken Si-H bonds. The hydrogen particles spread from the drain which created into the gate oxide. So we can be expressed it that H atoms are calculated as the average number of interface trap number.

$$N_{it} = \frac{\pi W}{2A_{tot}} n_x \int_0^{\sqrt{D_{H_x t}}} \left(N_{H_x(0)} \left[r - \frac{r^2}{\sqrt{D_{H_x t}}} \right] \right) dr$$

$$= N_{H_x(0)} \frac{\pi n_x}{12L} D_{H_x t} \quad (3)$$

$D_{H_x t}$ is the density of N_H. A_{tot} is the total area under the transistor gate. L is the channel length of the transistor. W is the channel width of the transistor.

N_{it} is written as follows by combining (1), (2), with (3).

$$N_{it} = \left(\frac{k_F N_0}{k_R}\right)^{\frac{n_x}{1+n_x}} \left(\frac{n_x \pi k_H}{12L} D_H\right)^{\frac{1}{1+n_x}} * t^{\frac{1}{1+n_x}} \quad (4)$$

Using the capacitance analysis, voltage dependence of the charge caused by interface traps is expressed as a shift of the sub-threshold characteristic curve which is close to the threshold voltage.

$$\Delta V_{th_{DEGRADATION}} =$$

$$C_{HCI} \left(\frac{k_F N_0}{k_R}\right)^{\frac{n_x}{1+n_x}} \left(\frac{n_x \pi k_H}{12L} D_H\right)^{\frac{1}{1+n_x}} * t^{\frac{1}{1+n_x}} \quad (5)$$

D_H is density of hydrogen atoms. *t* is time . C_{HCI} is technology-dependent parameter.

The mobility degradation is modeled, only if the threshold voltage of equation (5) can be implemented in the mobility model.

There are three types of mobility model equations in BSIM4 model. Either one can be selected by a switch parameter, MOBMOD.

MOBMOD=1

$$\mu_{eff} = \frac{U0}{1 + (UA + UC * V_{bseff})\left(\frac{V_{gsteff} + 2V_{th}}{TOXE}\right)} \frac{*f(L_{eff})}{+UB\left(\frac{V_{gsteff}+2V_{th}}{TOXE}\right)^2 + UD\left(\frac{V_{th}*TOXE}{V_{gsteff}+2V_{th}}\right)^2} \quad (6)$$

MOBMOD=2

$$\mu_{eff} = \frac{U0}{1 + (UA + UC * V_{bseff})} \frac{*1}{\left[\frac{V_{gsteff}+C_0(\boxed{VTH0}-VFB-\emptyset_S)}{TOXE}\right]^{EU}} \quad (7)$$

MOBMOD=3

$$\mu_{eff} = \frac{U0}{1 + UD\left(\frac{V_{th} * TOXE}{V_{gsteff} + 2V_{th}}\right)^2 + (1 + UC * V_{bseff})} \frac{*f(L_{eff})}{\left[UA\left(\frac{V_{gsteff}+2V_{th}}{TOXE}\right)+UB\left(\frac{V_{gsteff}+2V_{th}}{TOXE}\right)^2\right]} \quad (8)$$

$f(L_{eff})$ is expressed by the following equation.

$$f(L_{eff}) = 1 - \mathrm{UP} * \exp\left(-\frac{L_{eff}}{LP}\right) \quad (9)$$

U0 is the zero voltage carrier mobility. *UA* is the primary factor of mobility degradation. *UB* is the secondary coefficient of mobility degradation. *UC* is the substrate effect factor of mobility degradation. *UD* is the coulomb scattering coefficient of mobility degradation. UP is the channel length coefficient of mobility. LP is the channel length index of mobility. TOXE is the electrical gate oxide thickness. VTH0 is the threshold voltage at zero drain voltage. V_{th} is the threshold voltage. VFB is the flat-band voltage. V_{gsteff} is the effective value of V_{gs}-V_{th}. L_{eff} is the effective channel length. V_{bseff} is the effective substrate voltage of source. $\emptyset_s$ is the surface potential. C_0 is the constant value. When transistor is nMOS, C_0 becomes 2.0. When transistor pMOS, C_0 becomes 2.5.

Since only eq. (7) includes *VTH0* among these tree mobility models, the degradation of the mobility can be used directly by selecting MOBMOD = 2 after extracted and optimize other model parameters.

As the next step, equations of threshold voltage degradation are implemented in the model. $\Delta V_{th_DEGRADATION}$ in eq. (5) is added to the threshold voltage equation of the BSIM4 model as shown in eq. (10).

$$V_{th} = VTH0 + \Delta V_{th,\ body_effect} - \Delta V_{th,\ charge_{sharing}} - \Delta V_{th,\ DIBL} + \Delta V_{th,\ reverse_short_cannel} + \Delta V_{th,\ narrow_{width}} + \Delta V_{th,\ small_size} - \Delta V_{th,\ pocket_implant} + \Delta V_{th_DEGRADATION} \quad (10)$$

3. Degradation characteristics of the 1/f noise and DC current simulation

Using our modified BSIM4 model, DC model parameters are extracted and optimized to simulate the HCI degradations with MDW-SPICE.

In this experiment, we have simulated the degraded DC characteristics, which is dependent on channel length. We used a 90 nm process n-channel MOSFET whose channel width and length are 10.0 μm, which is called as Large (TEG). The other TEG which is celled as Short (TEG), has 10.0 μm channel width and 0.1 μm channel length. Degradation model parameters that we adopted for implementing into equation (5), which is described in the literature [7], are for 65 nm process. We obtained the threshold voltage degradation using *VTH0* after 1,000 hours at 300.15 K room temperature. Because of our resource limitations, measured data to calculate HCI degradations is different from the measured data used for other model parameter extractions. Therefore, the value of degradation parameters might be slightly aggressive for simulations with 90nm process devices. Compared to figure 1, 2, 3 and 4, short channel effect appears in the threshold and the amount of current. Similarly, compared to figure 5, 6, 7 and 8, we observe almost 3.3E-03 [A] change by the short channel effect. Excellent agreements between simulation and measurement data before degradations are obtained. After degradation, simulation data has been changed drastically by comparing with fresh measurements and simulations. The amount of drain current degradation with Short device is greater than the one with Large device. Average displacement of id-vg of Large dvice is 2.87E-06[A], id-vg of Short device is 1.65E-04[A], id-vd of Large device is 3.60E-05[A] and id-vd of Short device is 1.16E-03[A]. Although we changed only threshold voltage, the slope of id-vg characteristic in figure 1, 2, 3, and 4 are also changed. Because *VTH0* is used in mobility equations, the mobility degradation has been occurred. Figure 5, 6, 7, and 8 show decrease in the amount of current after the degradation. Electrons in the active channel become hot electrons under the high electric field at the drain end. Then, electrons reaching at the drain channel are reduced by injection into the gate oxide film and ionization at the substrate. Therefore, it is consistent with the theory [2].

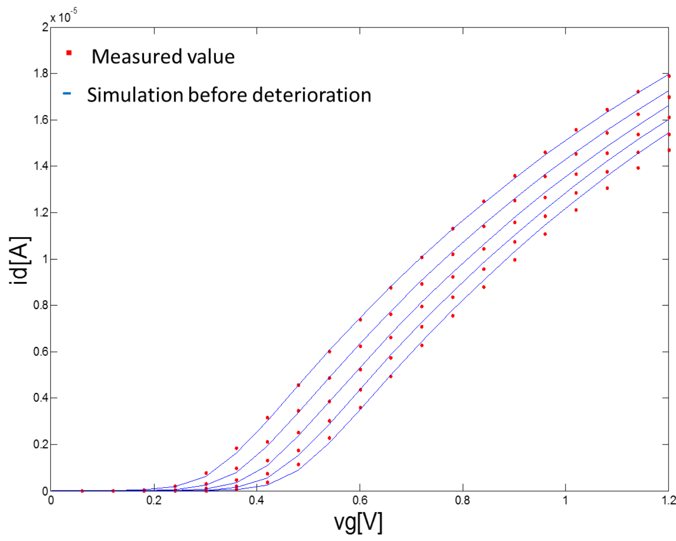

Fig. 1. I_{DS} vs. V_{DS} characterizations of fresh n-MOSFET of Large (V_{DS} = 0.01 V)

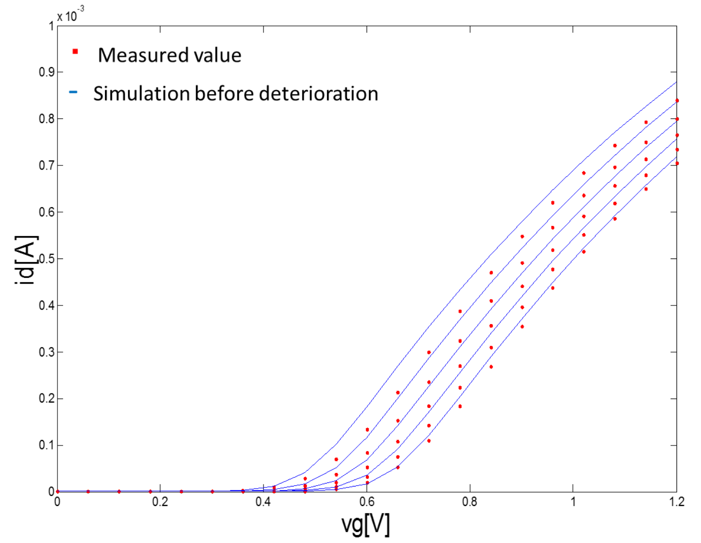

Fig. 3 .I_{DS} vs. V_{DS} characterizations of fresh n-MOSFET of Short (V_{BS} = 0.01 V)

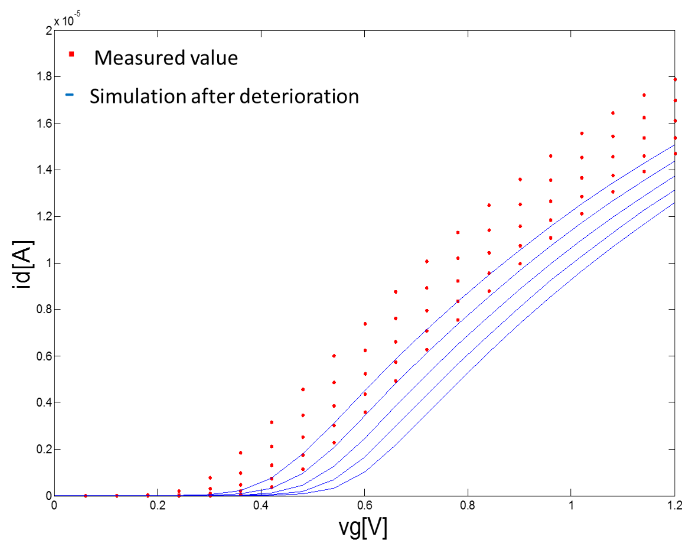

Fig. 2. I_{DS} vs. V_{DS} characterizations of degraded n-MOSFET of Large (V_{DS} = 0.01 V)

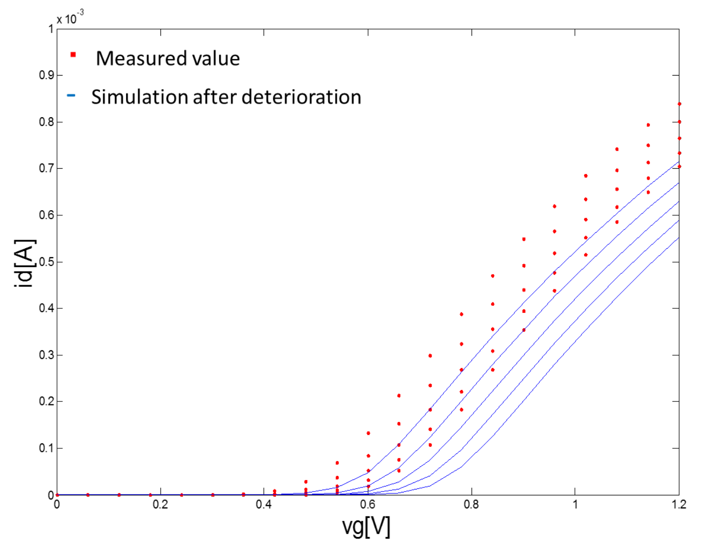

Fig. 4 .I_{DS} vs. V_{DS} characterizations of degraded n-MOSFET of Short (V_{BS} = 0.01 V)

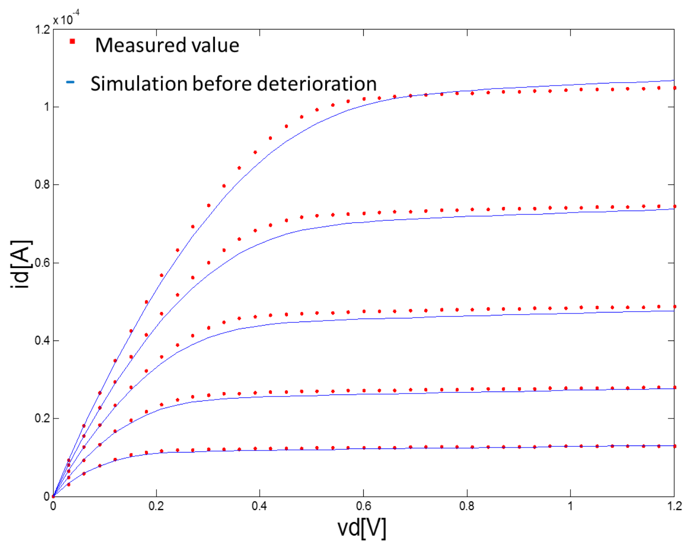

Fig.5. I_{DS} vs. V_{DS} characterizations of fresh n-MOSFET of Large (V_{BS} = 0.0 V)

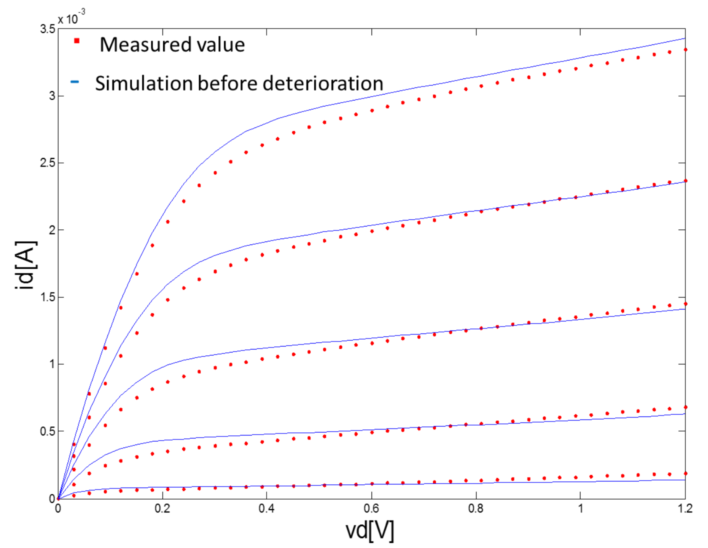

Fig.7. I_{DS} vs. V_{DS} characterizations of fresh n-MOSFET of Short (V_{BS} = 0.0 V)

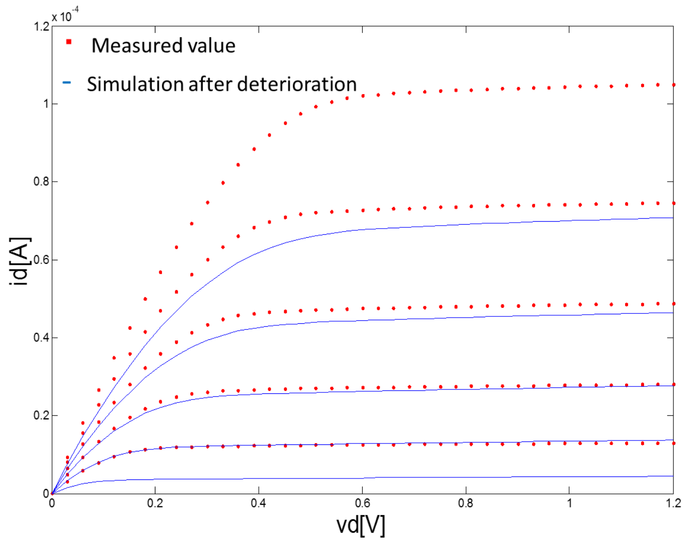

Fig.6. I_{DS} vs. V_{DS} characterizations of degraded n-MOSFET of Large (V_{BS} = 0.0 V)

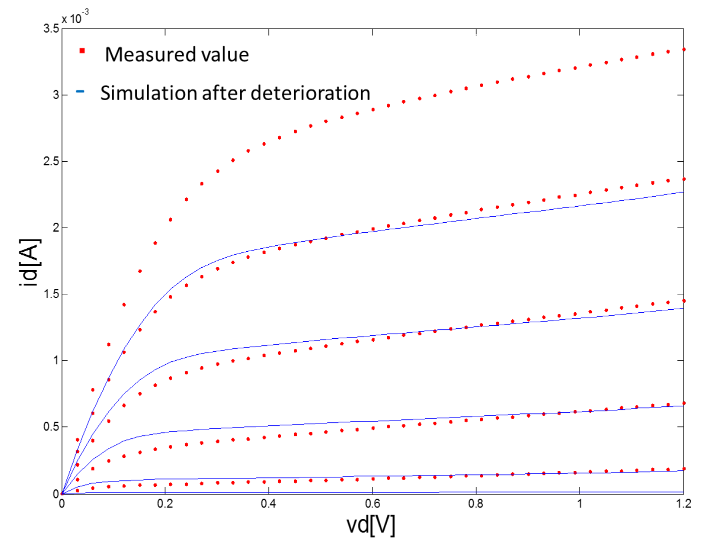

Fig.8. I_{DS} vs. V_{DS} characterizations of degraded n-MOSFET of Short (V_{BS} = 0.0 V)

We have measured 1/f noise of the TEG [8]. Figure 9 shows 1/f noise characteristics. Same degradation condition is used as static DC characteristics'. Degradation model parameters that we adopted for implementing into equation (5), which is described in the literature [7], are for 65 nm process. We obtained the threshold voltage degradation using *VTH0* after 1,000 hours at 300.15 K room temperature. By comparing before and after the degradations, noise is increased in 0.53 [dB]. The reason why the difference between two simulations before and after the stress is so small is as follows: By applying biasing stresses, the threshold voltage of the device is increased. Then, the drain current is decreased. Because drain output 1/f noise voltage density is proportional to the drain current, the noise level is reduced. On the other hand, when the mobility is increased, the drain output 1/f noise density increases caused by mobility fluctuations [8]. As a result, two effects negate degraded drain output 1/f noise density level. To observe the 1/f noise degradations, input referred noise should be calculated. We will analyze it in later study.

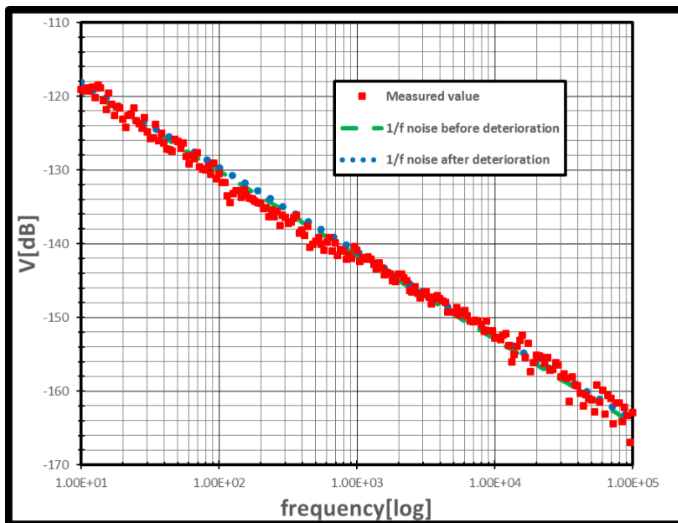

Fig.9 1/f noise characterizations of fresh and degraded n-MOSFET

4. Summary

In this study, we implemented the HCI phenomenon of n-channel MOSFET into a circuit simulator, MDW-SPICE. We have developed a method for predicting the DC voltage-current characteristics of fresh and degraded MOSFETs. The device model is based on BSIM4 model with equations for HCI degradations. We have extracted model parameters with 90nm process device when it is fresh state and showed deterioration DC characteristics of the channel length dependence in the simulation. Then, 1/f noise simulation is performed in order to verify the effects caused by time and temperature degradation in DC.

The 1/f noise characteristics of time and temperature degradations due to HCI phenomenon only affected by DC model are also simulated in this paper. We will complete to develop the temperature and time degradation model by analyzing 1/f noise dedicated degradation mechanisms.

Reference

[1] S. Todoroki, H. Aoki, F. Abe, K. Ramin, Y. Arai, M. Kazumi, T. Totsuka, H. Kobayashi, "1/f Noise Variance Modeling of Gate Voltage Dependence with n-channel MOSFETs," Institute of Electrical Engineers Japan (IEEJ). ECT-14-010 Kanazawa (Jan, 2014).

[2] H. Aoki, M. Shimasue, Y. Kawahara, *CMOS Modeling Technology*, Maruzen Publishing, (2006).

[3]H. Aoki, "Bias and Geometry Dependent Flicker Noise Characterization for n-MOSFETs," IEICE Trans. Electronics, vol. E85-C, no.2 pp.408-414(2002).

[4] Information on http://www-device.eecs . berkeley.edu/bsim/

[5] C. Hu, et al, "Hot-electron induced MOSFET degradation model, monitor, and improvement," Trans. Electron Devices, 32(2), 375-385, 1985.

[6] E. Maricau and G. Gielen, *Analog IC Reliability in Nanometer CMOS*, Springer Science Business Media New York, 2013.

[7] H. Kufluoglu and M. A. Alam, "A unified modeling of NBTI and hot carrier injection for MOSFET reliability," 10th International Workshop on Computational Electronics, pp. 28-29, Oct. 2004.

[8] H. Aoki and M. Shimasue, "Noise Characterization of MOSFETs for RF Oscillator Design," Proc. 1999 IEEE MTT-S International Microwave Symposium, Anaheim CA, (Jun. 1999).