

# *Efficiency Improvement for Switching Power Supply at Light Load Using DSP Control*

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*Gunma University*

*Sanken Electric Co., Ltd.*

# Outline

- Research Background
- Two Parts of Server Power Supply
- Loss Mechanisms of PFC AC/DC Converter and DC/DC Converter
- Experimental Environment
- Experiment Results A:  
*Link Voltage Optimization of BLPFC AC/DC at a Half-Load*
- Experiment Results B:  
*Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%*
- Experiment Results C:  
*Optimization of PWM Frequency of PSFB DC/DC at a Load Rate of 5% to 20%*
- Conclusion

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# Research Background

- The **energy efficiency** of server power supply is gaining attention.
- **Low energy efficiency at light load of 20%~30%** . 😞
- 80 PLUS Certified Power Supplies and Manufacturers



Server Power Supply



% of Rated Load	10%	20%	50%	100%
BRONZE	N/A	80%	85%	81%
SILVER	N/A	85%	89%	85%
GOLD	N/A	88%	92%	88%
PLANTINUM	N/A	90%	94%	91%
TITANIUM	90%	94%	96%	91%

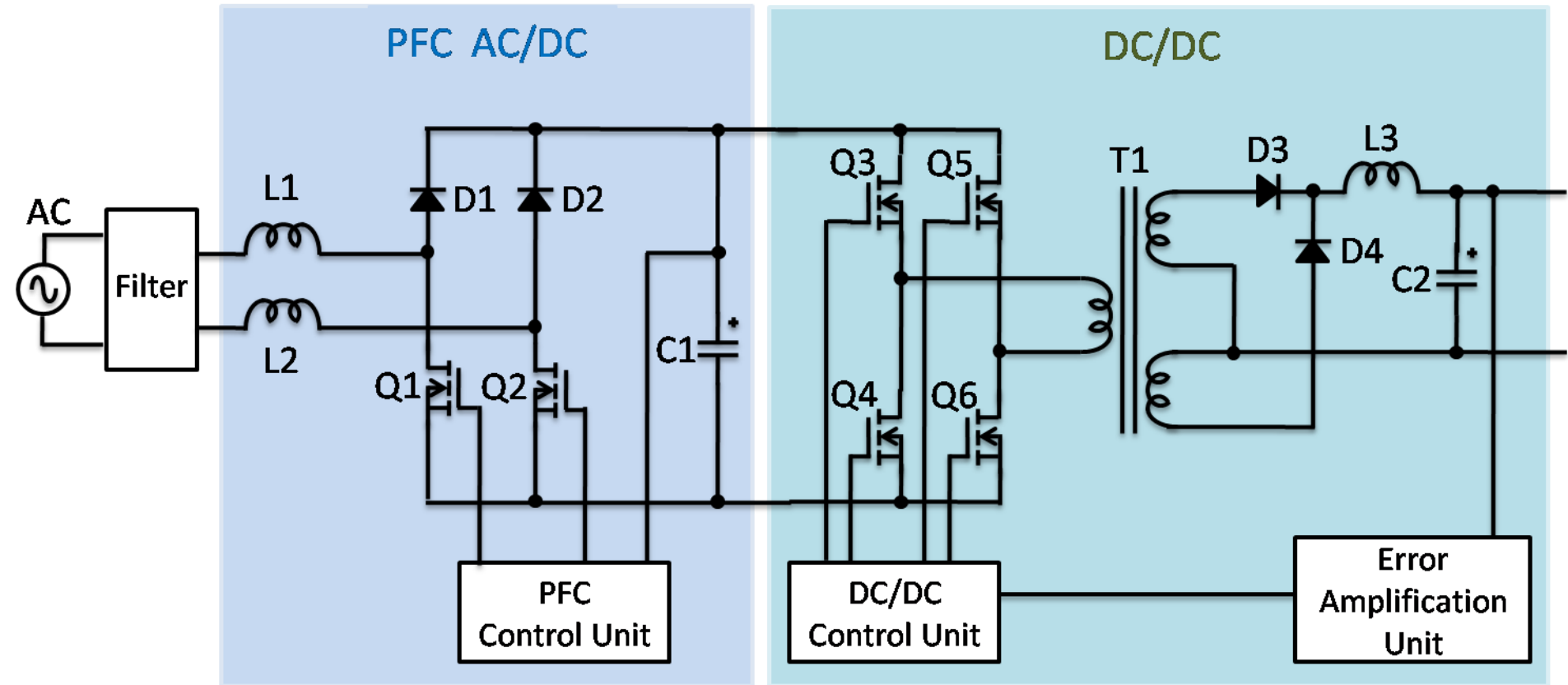
# Outline

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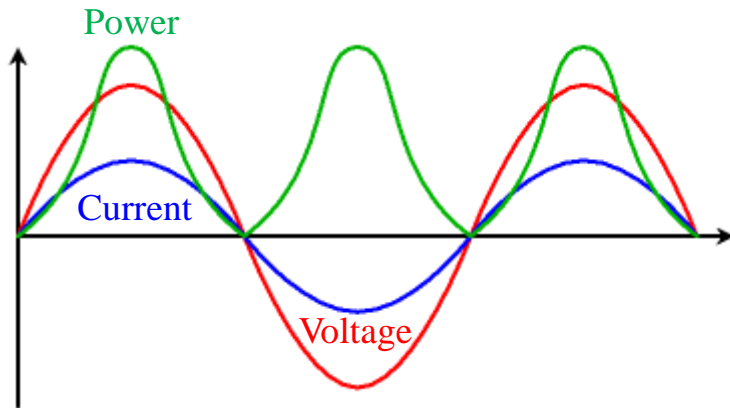
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# Two parts of Server Power Supply

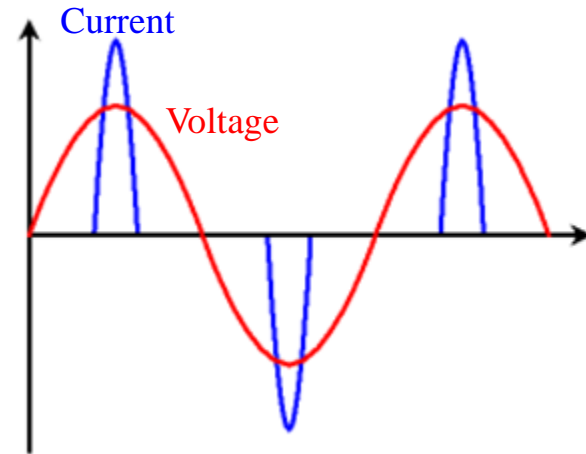
AC/DC part + DC/DC part



# Power Factor Correction (PFC) Circuit



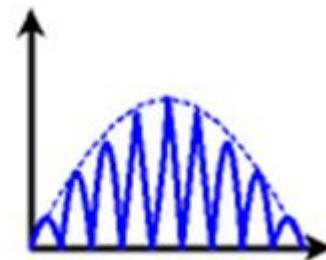
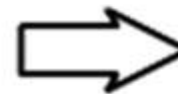
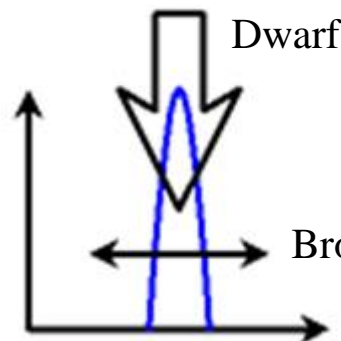
Ideal Input Voltage and Current



Actual Input Voltage and Current

Risk of damage to power transmission and distribution appliances

What PFC does



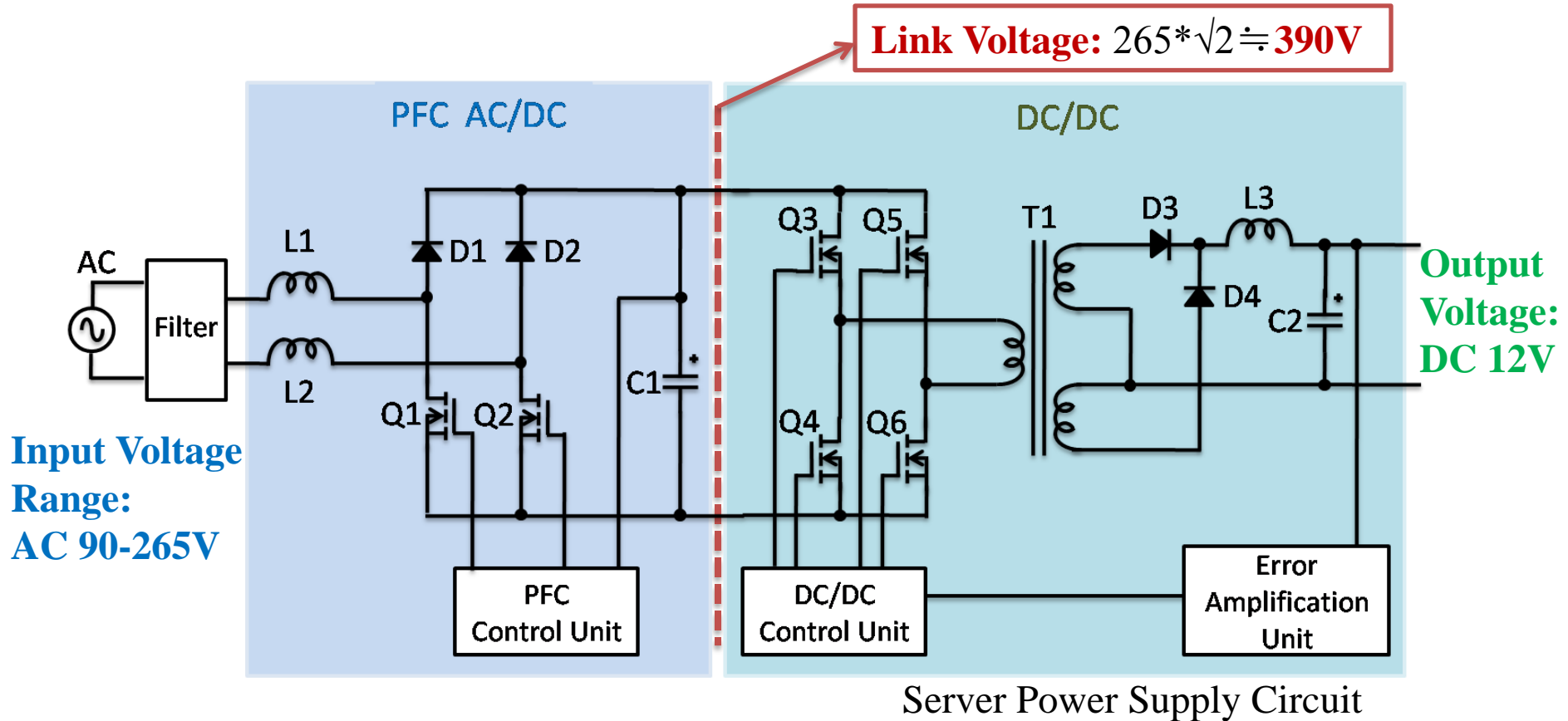
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# Loss Mechanisms of Server Power Supply ①

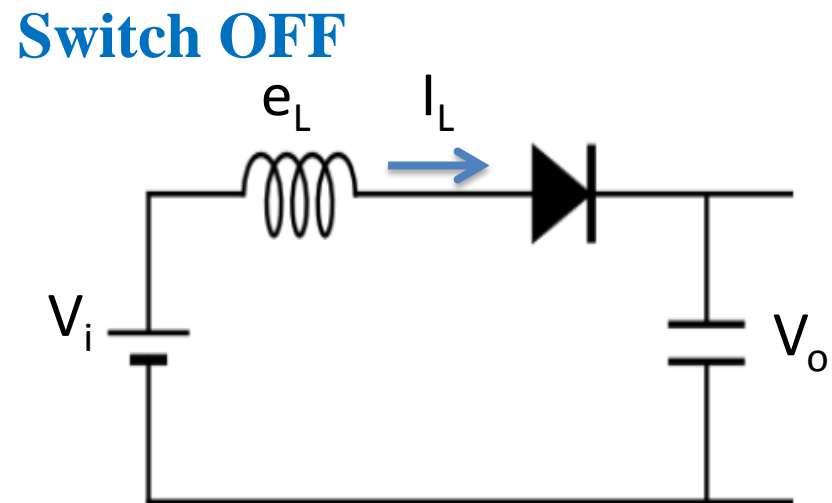
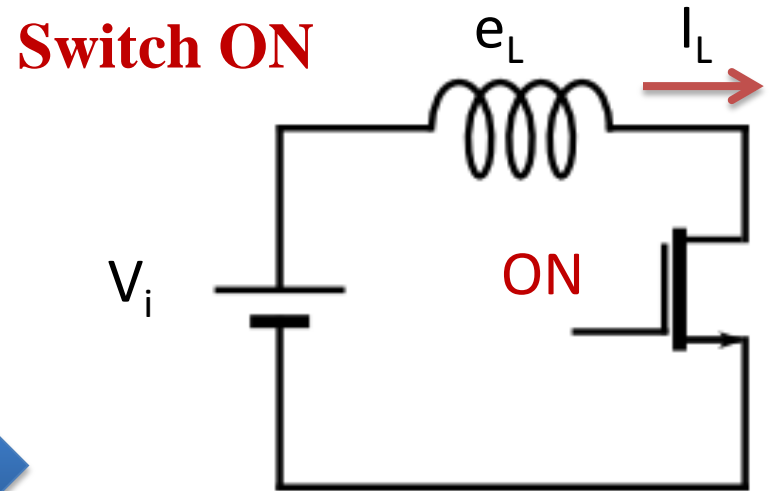
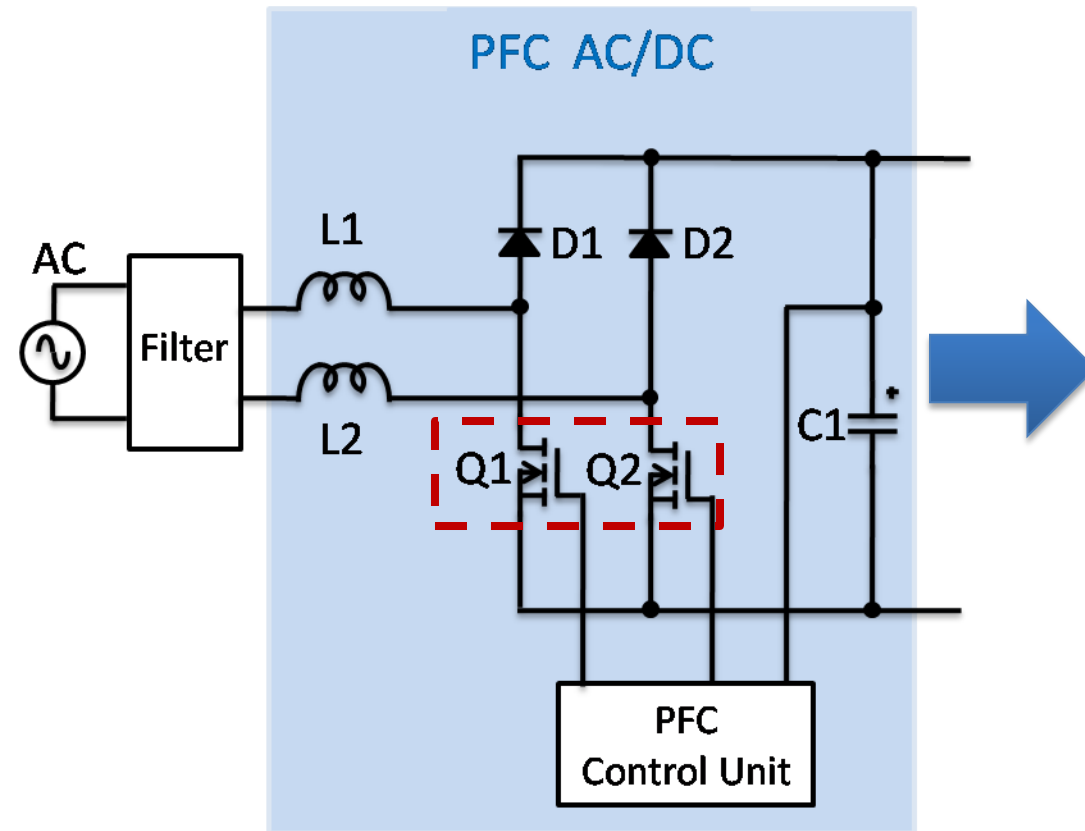


High Link Voltage

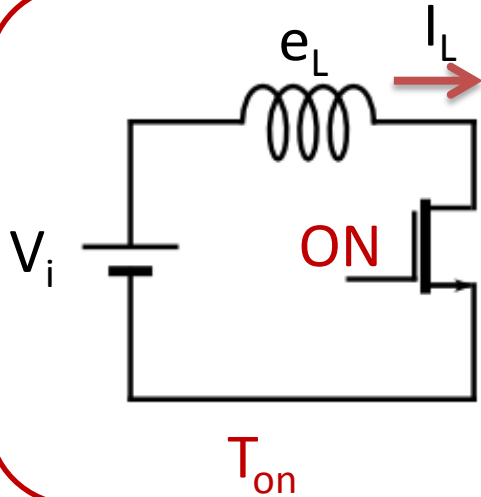


Lower energy efficiency

# Principle of PFC AC/DC ②: Boost



## Energy Charging



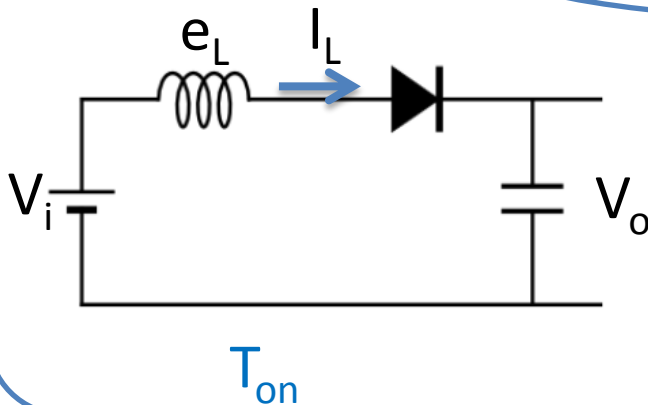
Current through L:

$$i_u = \frac{1}{L} \int_0^{T_1} e_L dt$$

Steady state:  $e_L = V_i$

$$i_u = \frac{V_i}{L} \cdot T_{on}$$

## Energy Releasing



$$e_L = V_o - V_i$$

$V_i$  ,  $V_o$  remain the same  $\rightarrow$   $e_L$  remains the same

$$\text{Current through L: } i_d = \frac{V_o - V_i}{L} \cdot T_{off}$$

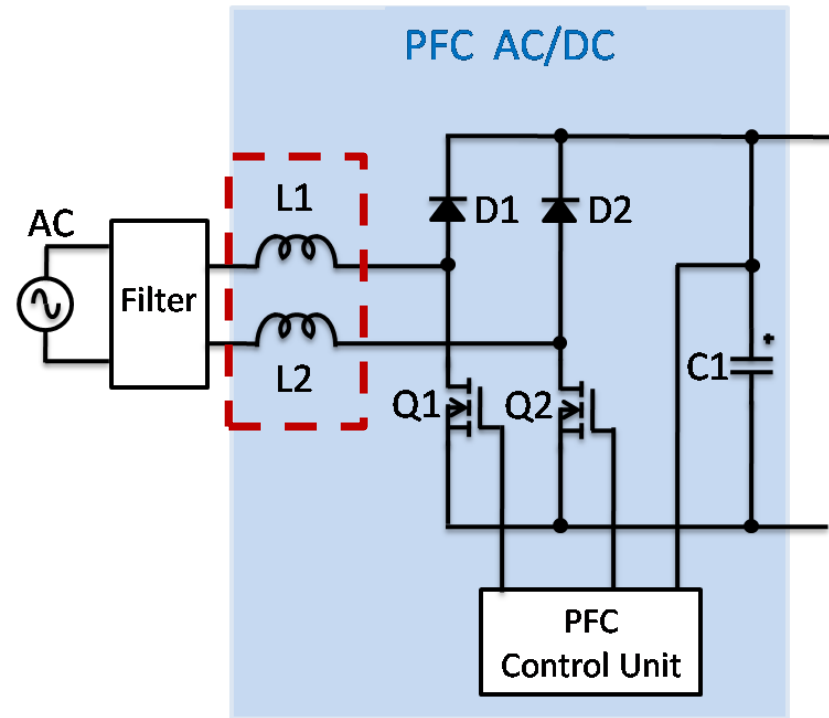
Steady State

$$i_d = i_u$$



$$V_o = \left(1 + \frac{T_{on}}{T_{off}}\right) \cdot V_i$$

# Loss derived from High Link Voltage



● **Reactor Loss / Iron Loss**  $P_i = P_h + P_e = K(B_m^{2.77} f^{1.55})$

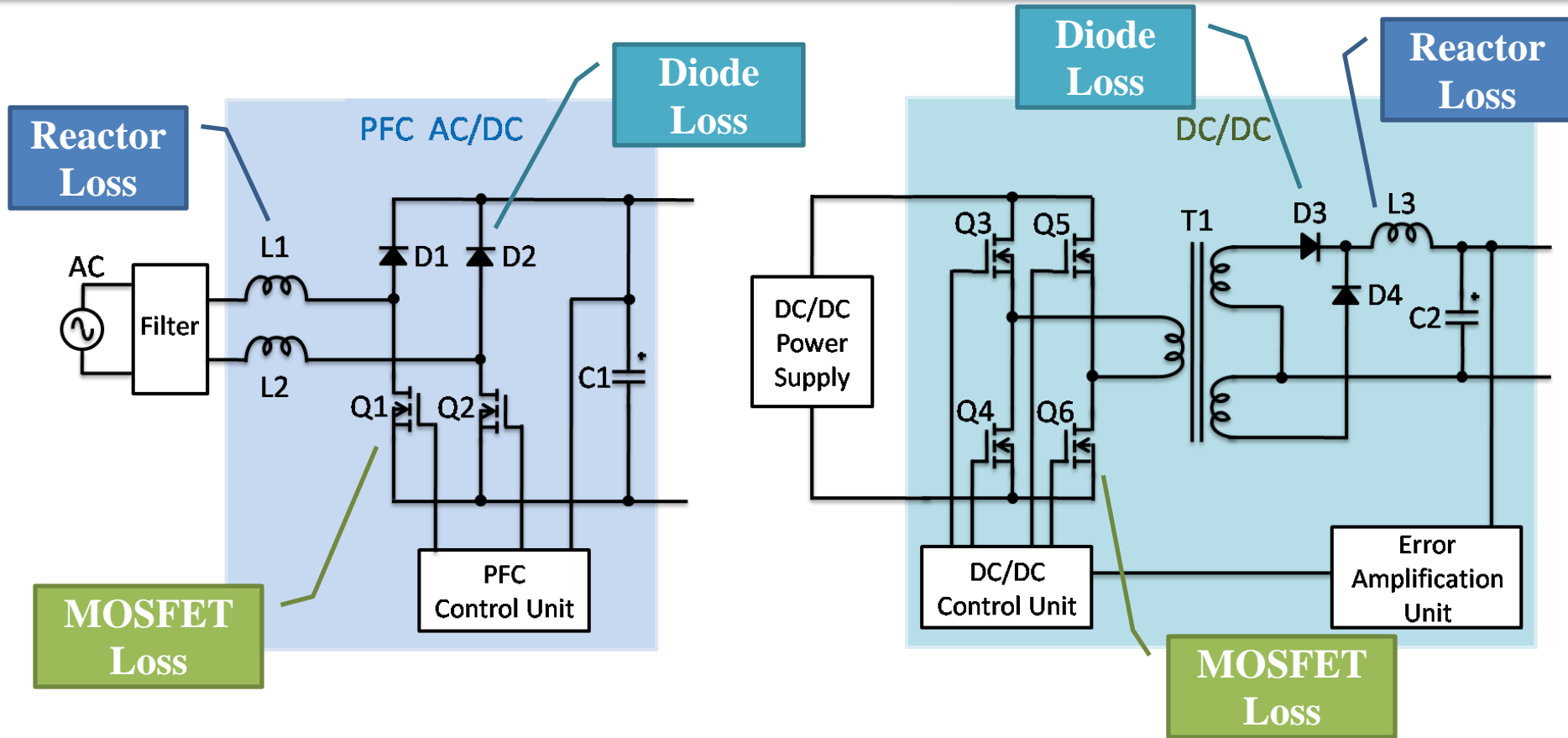
● **Hysteresis Loss**  $P_h = k_h \frac{e_L^{1.6}}{f^{0.6}}$

● **Eddy Current Loss**  $P_e = k_e \frac{(te_L)^2}{f^{0.6}}$

$$e_L = V_o - V_i$$

**Link Voltage**

# Loss Mechanisms of Server Power Supply ②



Diode Loss



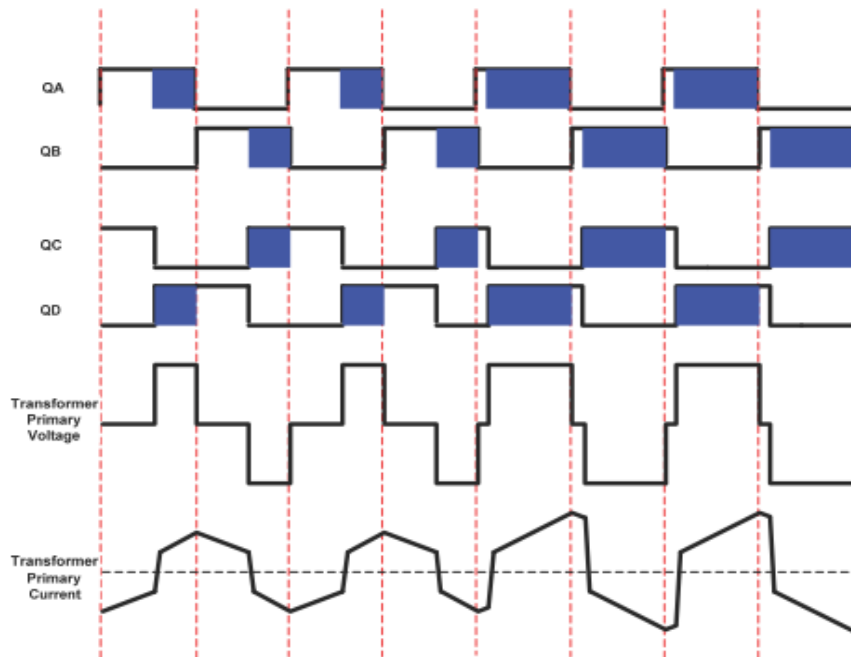
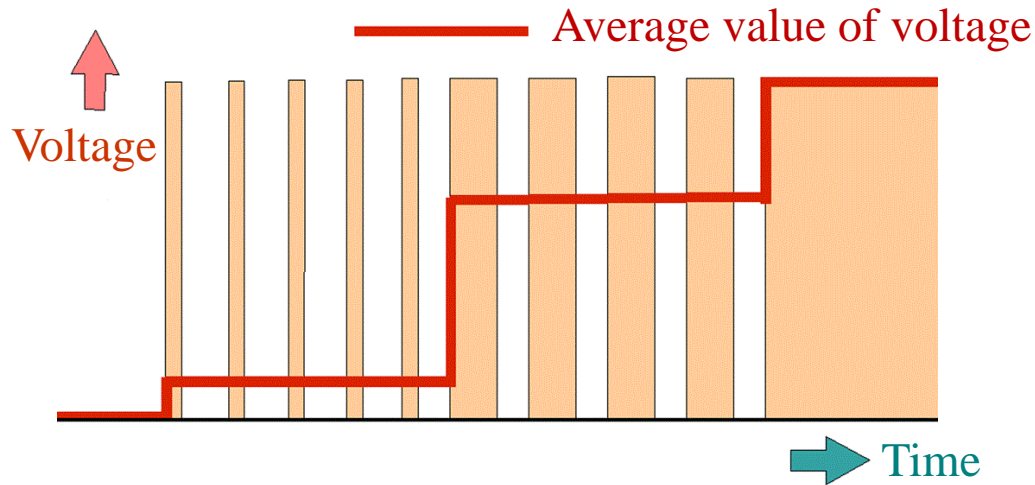
$$P_{SW(DIODE)} = 0.5 \times V_{REVERSE} \times I_{RR(PEAK)} \times t_{RR} \times f_s$$

MOSFET Loss



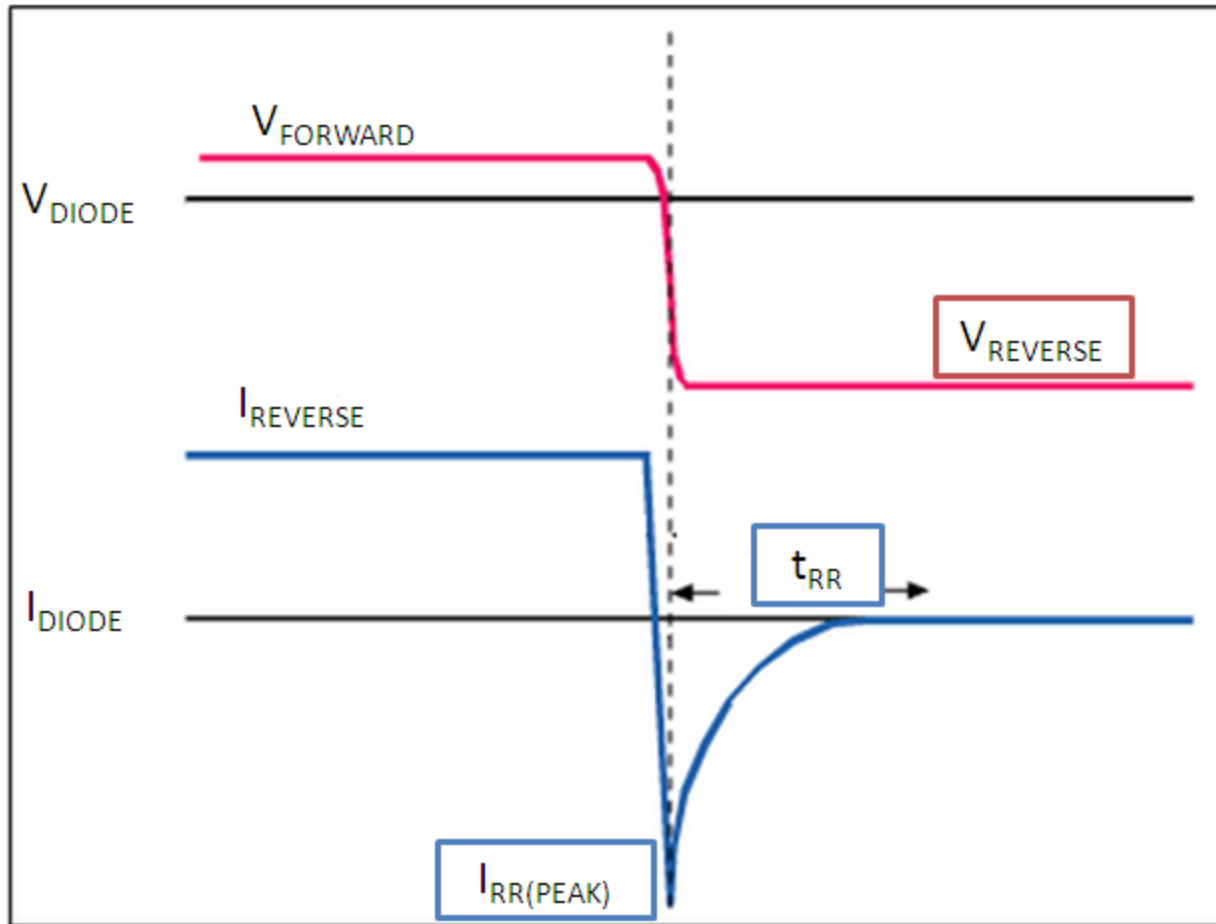
$$P_{SW(MOSFET)} = 0.5 \times V_D \times I_D \times (t_{SW(ON)} + t_{SW(OFF)}) \times f_s$$

# PWM(Pulse-width Modulation) Control



PSFB (Phase Shifted Full Bridge)  
PWM waveform

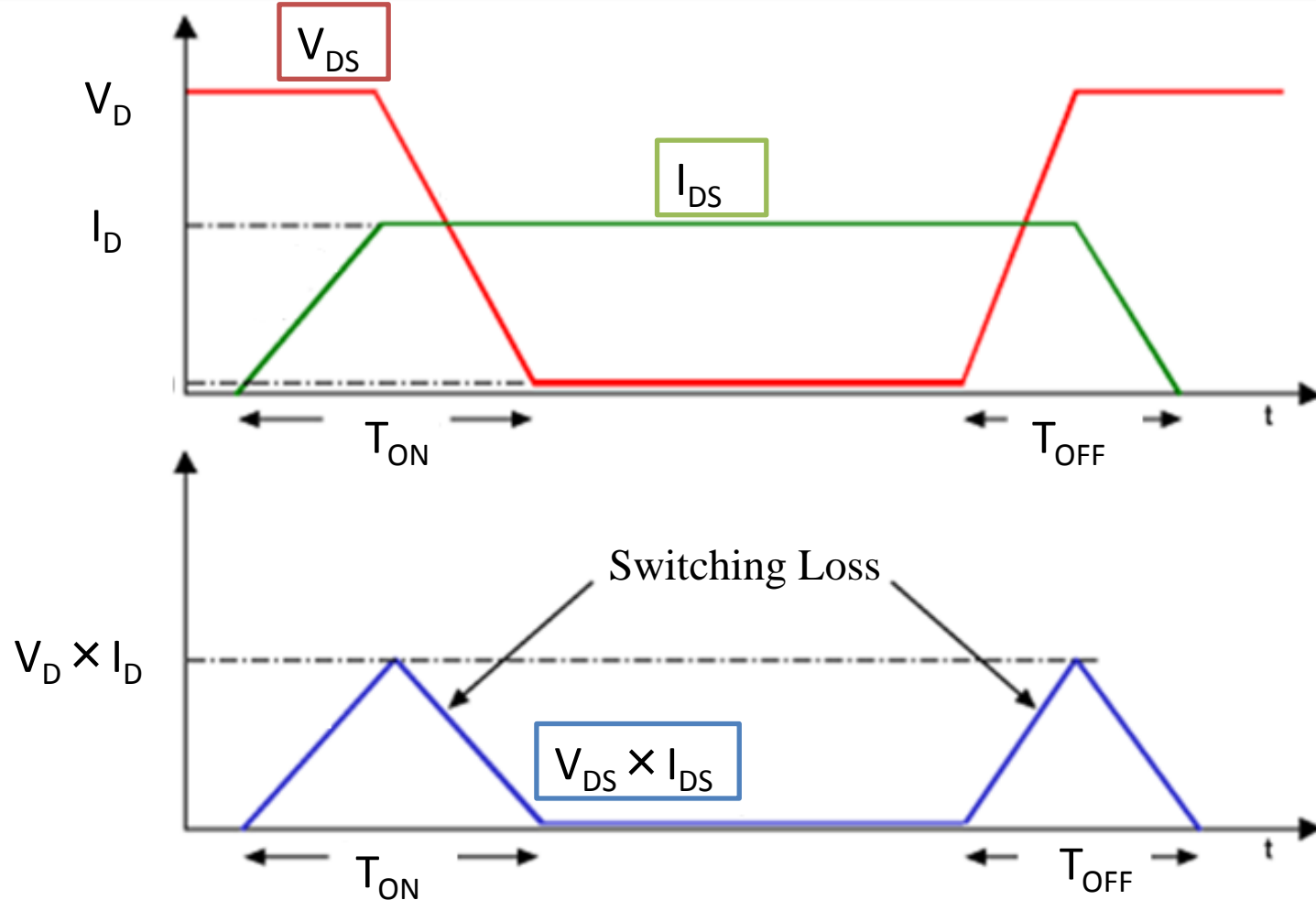
# Diode Loss



Power Loss = **Reverse Voltage** × **Spike Current** × **Time Span** × **Frequency**

$$P_{SW(DIODE)} = 0.5 \times V_{REVERSE} \times I_{RR(PEAK)} \times t_{RR} \times f_S$$

# MOSFET Loss

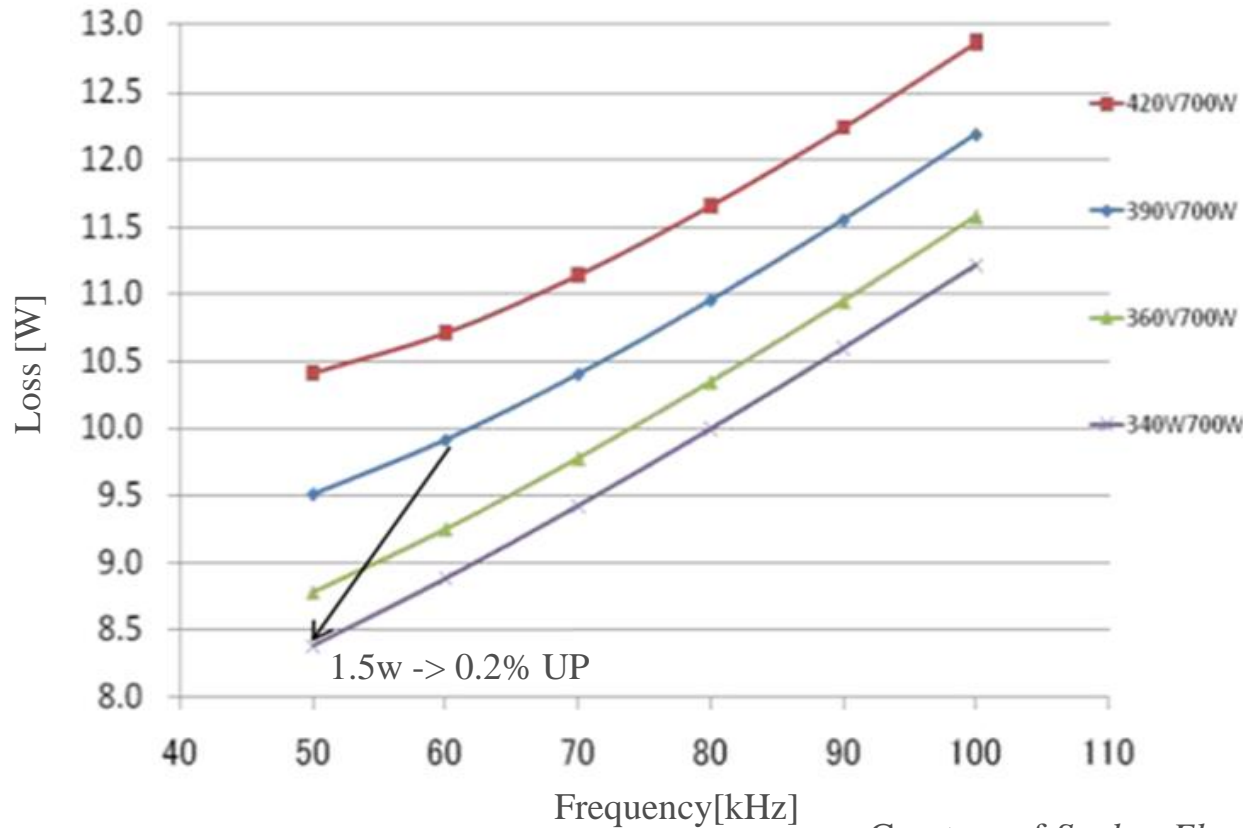


**Power Loss = Drain-Source Voltage  $\times$  Channel Current  $\times$  Time Span  $\times$  Frequency**

$$P_{SW(MOSFET)} = 0.5 \times V_{DS} \times I_D \times (t_{SW(ON)} + t_{SW(OFF)}) \times f_S$$



# Total Effect of Loss Mechanism ①+②



Courtesy of Sanken Electric Co., Ltd.

Energy efficiency downgrade of the PFC  
on the account of these **two** main loss mechanism  
(**Reactor Loss + Diode Loss + MOSFET Loss**).

# Proposed Method

This paper discussed how to improve the efficiency of power supplies at **half-load** and **light load under 20%** using digital control.

## Conventional Method

[PFC]

- **Fixed** link voltage
- PWM(**fixed** frequency)

[DC/DC]

- PWM(**fixed** frequency)



Efficiency  
degradation



## Proposed Method

[PFC]

- **Variable** link voltage
- PWM(**variable** frequency)

[DC/DC]

- PWM(**variable** frequency)



Circuit topology  
**Hardware**



DSP digital control  
**Software**



# Research Approach

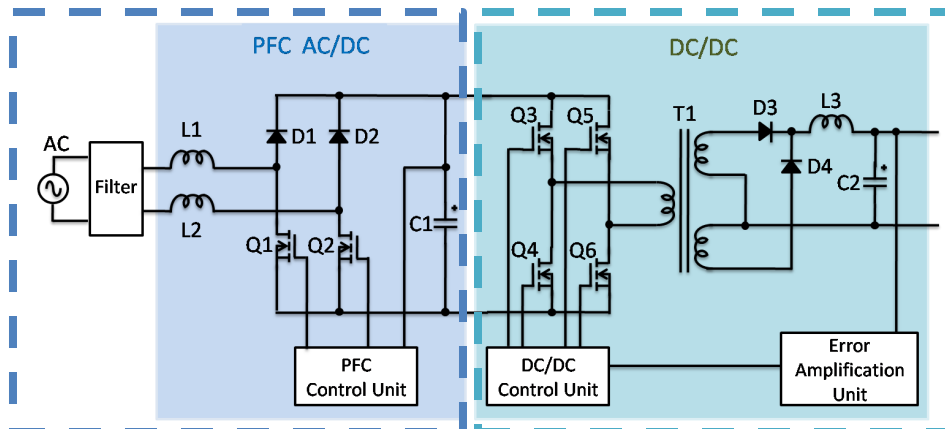
The experiment is conducted by a mean of **two parts** and **three steps**.

## BLPFC AC/DC part (Bridgeless Power Factor Correction AC/DC)

- **Step A:** Load rate 50% → Deal with **Link Voltage**
- **Step B:** Load rate 10%~20% → Deal with **PWM Frequency**

## PSFB DC/DC part (Phase Shift Full Bridge DC/DC)

- **Step C:** Load rate 10%~20% → Deal with **PWM Frequency**



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# Experimental Environment

## Specifications of experiment boards controlled by **C2000 Series DSP**

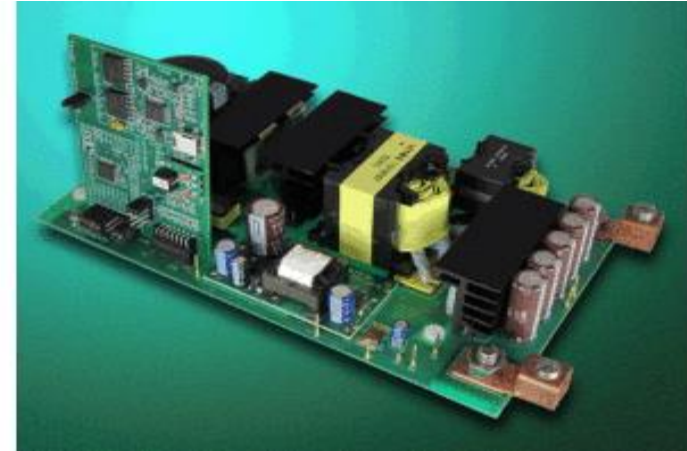
(Texas Instruments Inc.)



- Input Voltage (AC line): 85V(Min) to 265V(Max), 47~63Hz
- **400Vdc Output**
- 300 Watts Output Power
- Full Load efficiency greater than 93%
- Power factor at 50% or greater load – 0.98(Min)
- **PWM frequency 200kHz.**

### BL PFC (Bridgeless PFC) AC/DC Kit

- **400Vdc Output**
- **PWM frequency 200kHz**



- 400V DC input (370Vdc to 410Vdc operation)
- 12V DC output
- Peak efficiency greater than 95%
- 50A (600Watt) rated output.
- Phase Shifted Full Bridge Circuit topology
- **100kHz switching frequency.**

### PSFB (Phase shifted Full Bridge) DC/DC Kit

- **400V dc Input (370Vdc to 410Vdc)**
- **100kHz switching frequency**

**Link voltage**

# Experimental Environment



**Code Composer Studio (CCStudio or CCS)** is an integrated development environment (IDE) to develop applications for Texas Instruments (TI) embedded processors.

The screenshot shows the Code Composer Studio IDE with a C program open. The program defines a structure for PWM registers and implements a function to configure and start PWM channels. The code includes comments for duty cycle and switching frequency settings.

```
#include "PeripheralHeaderIncludes.h"
#include "DSP2802x_EPWM_defines.h" // useful defines specific to EPWM
11 extern volatile struct EPWM_REGS *EPWM[];
12
13
14 void PWMDRV_PSFB_PWM_CHANGE(int16 n, int m, int16 IoutR, int16 SR_Enable)
15 {
16     switch(m)
17     {
18         case 0:
19         {
20             (*EPWM[n]).TBPRD = 858; //70kHz
21             (*EPWM[n]).CMPA.half.CMPA = 858/2; // Fix duty at 50%
22             (*EPWM[n+1]).TBPRD = (858-1); // Fix duty
23             (*EPWM[n+1]).CMPA.half.CMPA = 858/2; // Fix duty
24             if (SR_Enable == 1)
25             {
26                 (*EPWM[n+3]).TBPRD=858/2-1;
27             }
28             break;
29         case 1:
30         {
31             (*EPWM[n]).TBPRD = 750; //80kHz
32             (*EPWM[n]).CMPA.half.CMPA = 750/2; // Fix
33             (*EPWM[n+1]).TBPRD = (750-1); // Fix
34             (*EPWM[n+1]).CMPA.half.CMPA = 750/2; // Fix
35             if (SR_Enable == 1)
36             {
37                 (*EPWM[n+3]).TBPRD=750/2-1;
38             }
39             }
40         case 2:
41         {
42             (*EPWM[n]).TBPRD = 668; //90kHz
43             (*EPWM[n]).CMPA.half.CMPA = 668/2; // Fix
44             (*EPWM[n+1]).TBPRD = (668-1);
```

## BL PFC (Bridgeless PFC) AC/DC Kit

- Appropriate **Link Voltage**
- Appropriate **PWM Switching Frequency**

## PSFB (Phase shifted Full Bridge) DC/DC Kit

- Appropriate **PWM Switching Frequency**

These characteristics can be achieved by modifying the main program.

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# Analysis of BLPFC AC/DC part ①

## ● Loss Mechanisms of Server Power Supply ①

Input Voltage < Link Voltage  
 (85~265V) (390~400V)

● By monitoring the **effective value of** input voltage and adjust the link voltage in a real-time way.

Monitor the input voltage  $V_{in\_N}$ ,  $V_{in\_L}$



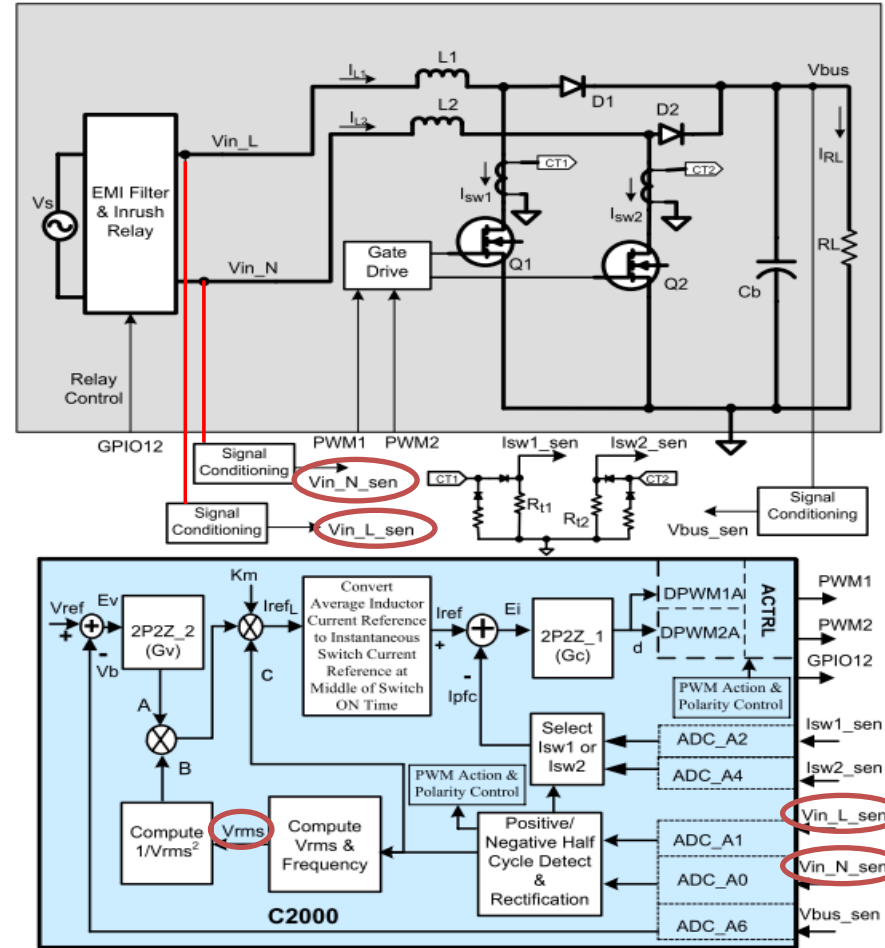
Read into DSP



Evaluation of effective value  $V_{rms}$



**Link voltage:**  $V_{out} = \text{Optimum boost ratio} \times V_{rms}$



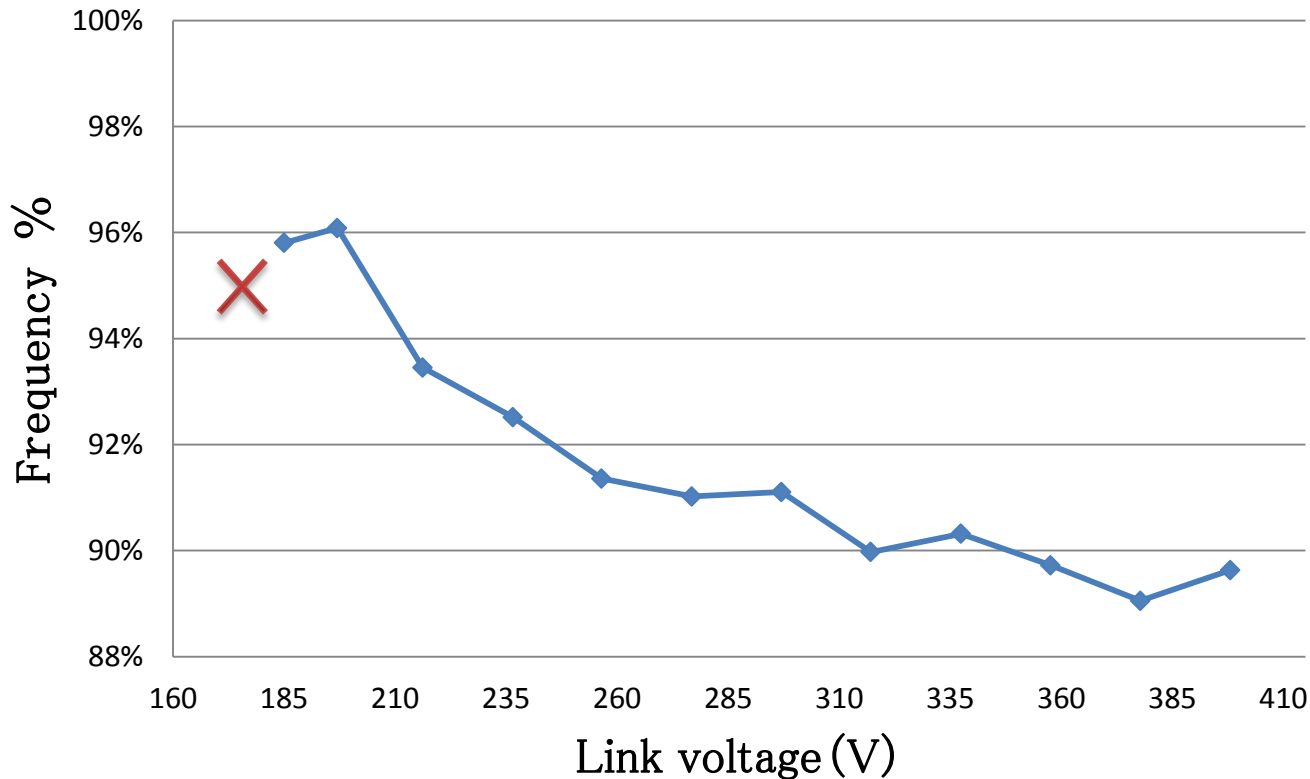


# Experiment Results A:

## Link Voltage Optimization of BLPFC AC/DC *at a Half-Load*

Experiment environment

- AC input voltage  $V_{in}=100V$
- Switching frequency is fixed at 200kHz
- Load rate 50% (150W output)



Unexpected problem occurs when **link voltage is set down below 190V.**



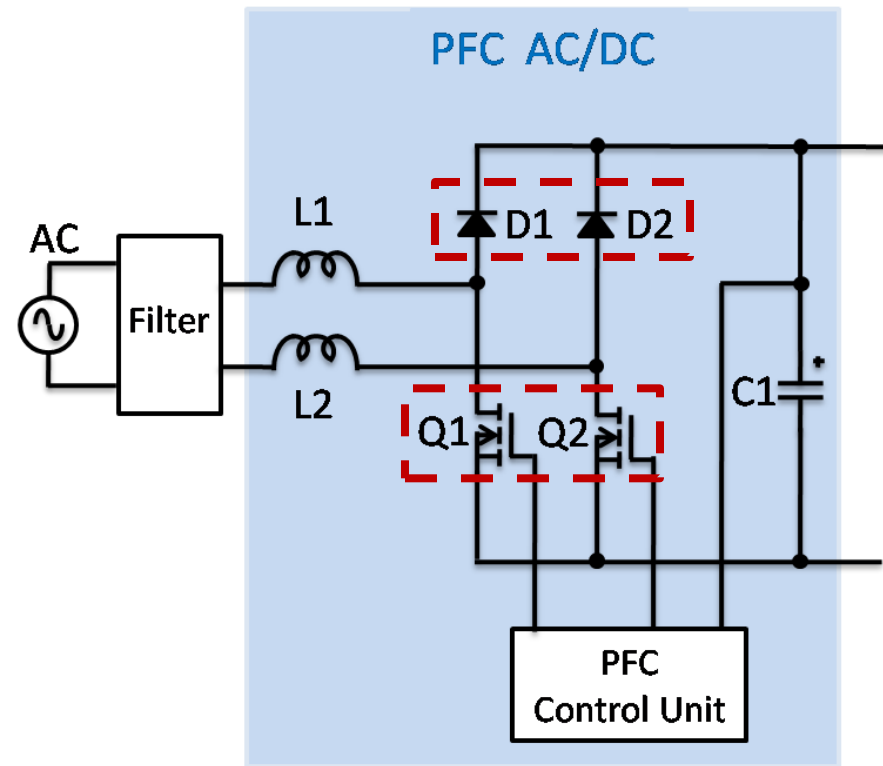
Appropriate link voltage is 200V if possible.

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# Analysis of BLPFC AC/DC part ②



- Loss Mechanisms of Server Power Supply ②  
(Diode loss & MOSFET loss  $\propto f$ )
- Therefore, a **variable PWM switching frequency by digital control** has been tested.

Light load + **Fixed frequency**

Light load + **Variable frequency**

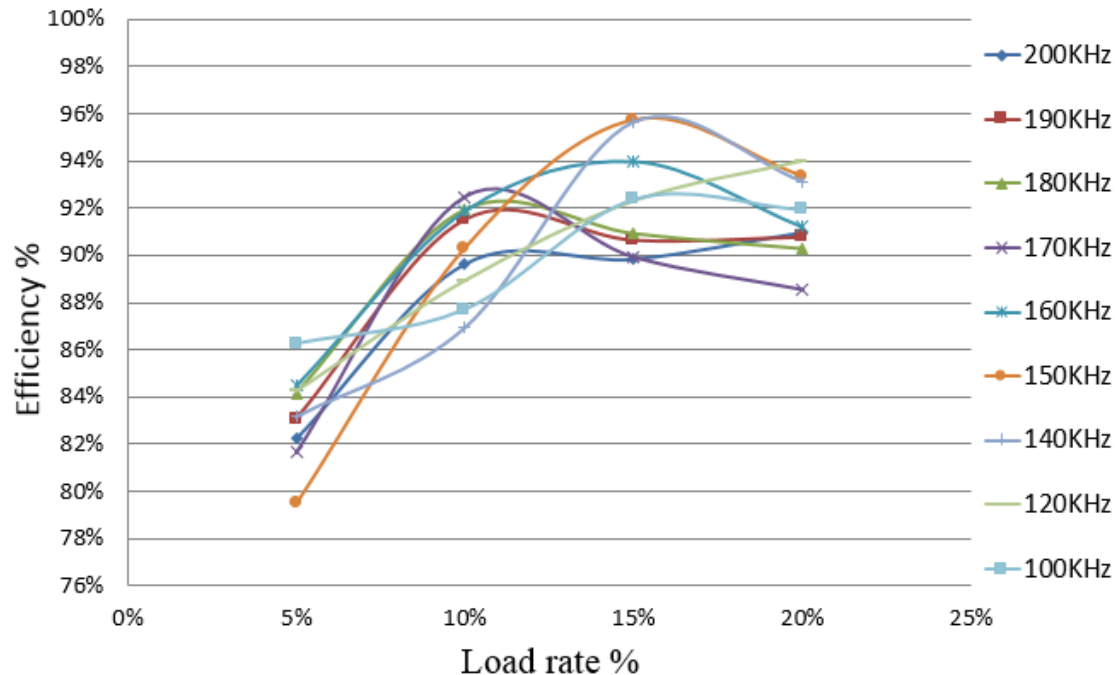
**Proposed**

# Experiment Results B:

## Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%

### Experiment environment

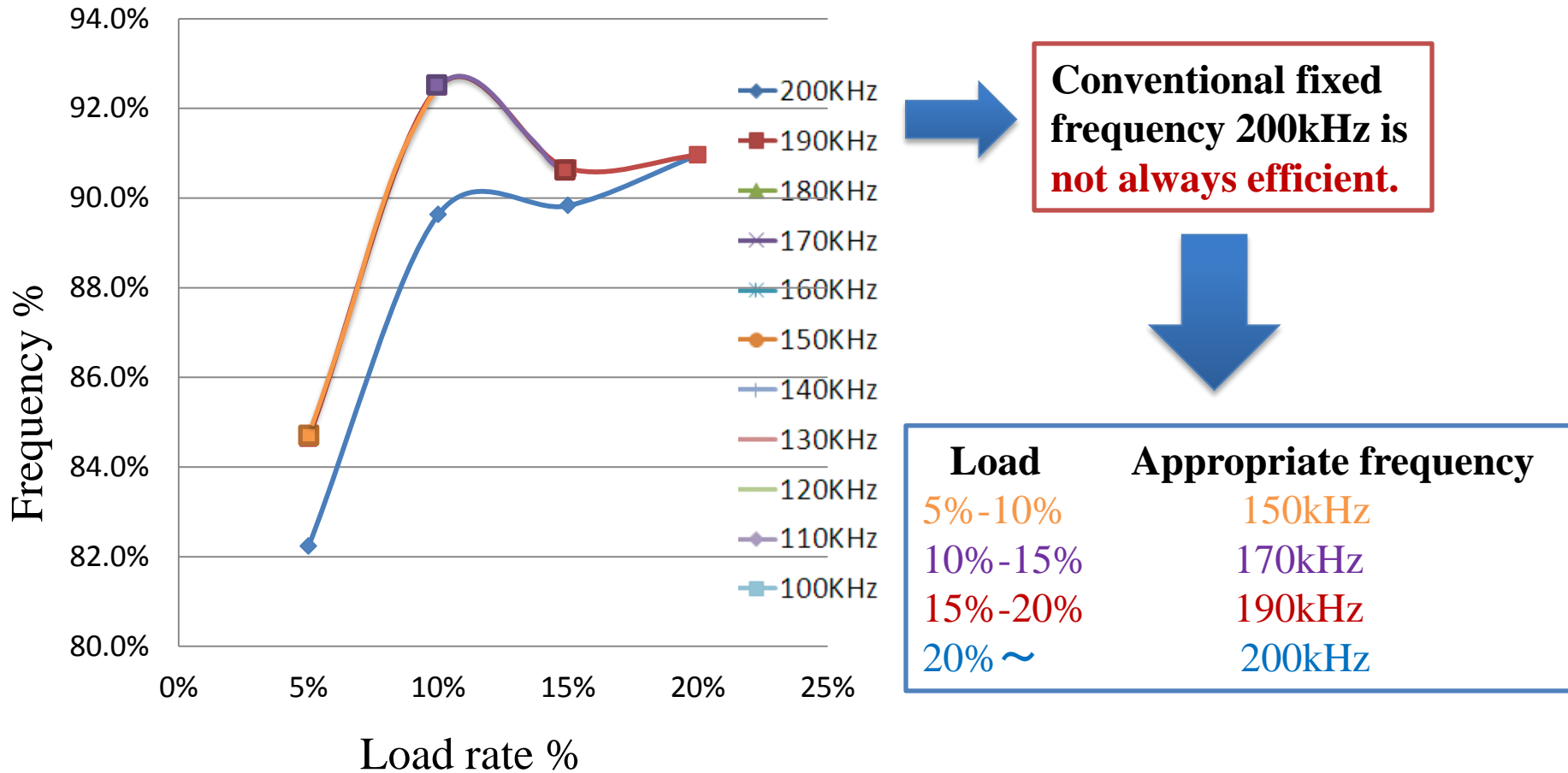
- AC input voltage  $V_{in}=100V$
- Link voltage (PFC output voltage) is fixed at **400V**



(a) Variation of efficiency according to frequency at 400V link voltage.

# Experiment Results B:

## Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%



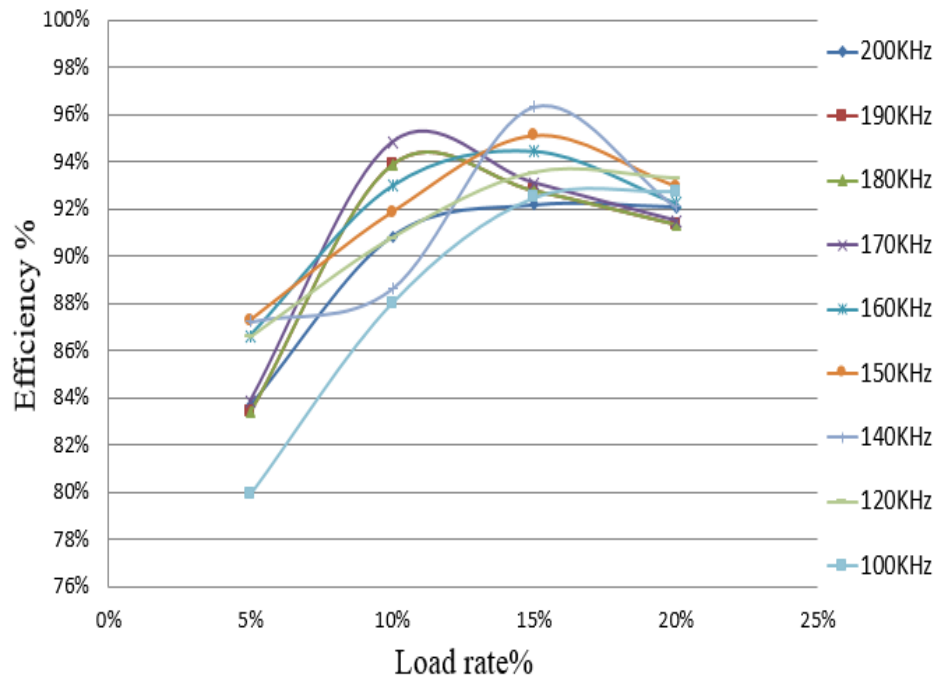
(b) Comparison of efficiency between 200kHz and optimum frequency.

# Experiment Results B:

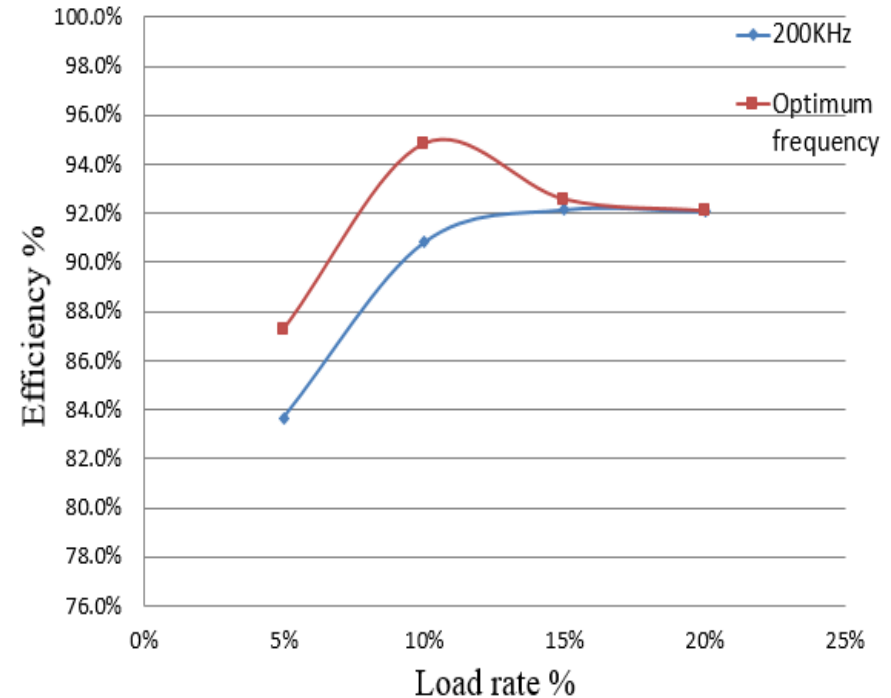
## Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%

### Experiment environment

- AC input voltage  $V_{in}=100V$
- Link voltage (PFC output voltage) is fixed at **350V**



(a) Variation of efficiency according to frequency at 350V link voltage.



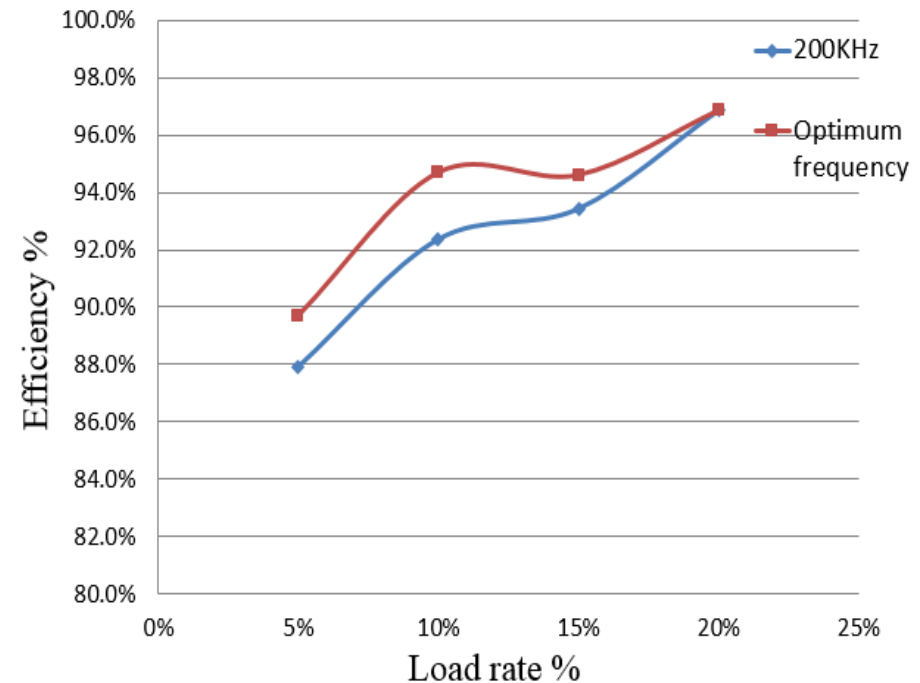
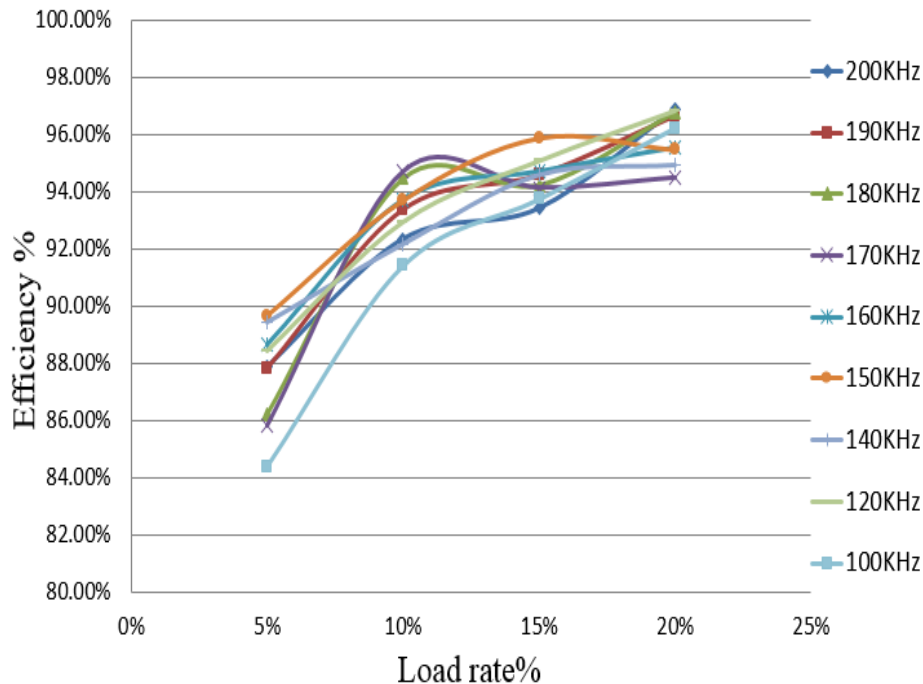
(b) Comparison of efficiency between 200kHz and optimum frequency.

# Experiment Results B:

## Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%

### Experiment environment

- AC input voltage  $V_{in}=100V$
- Link voltage (PFC output voltage) is fixed at **300V**



(a) Variation of efficiency according to frequency at 300V link voltage.

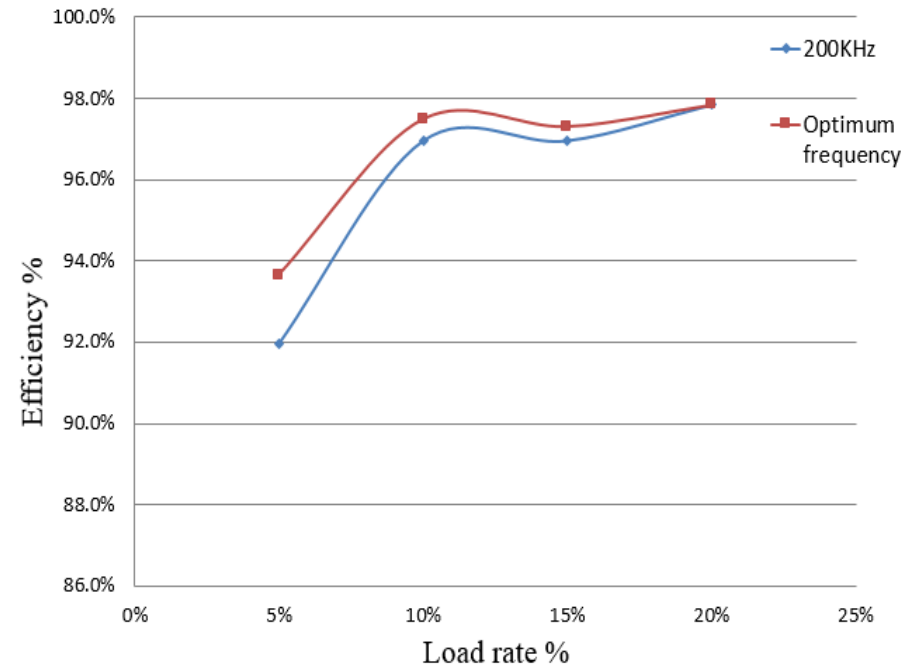
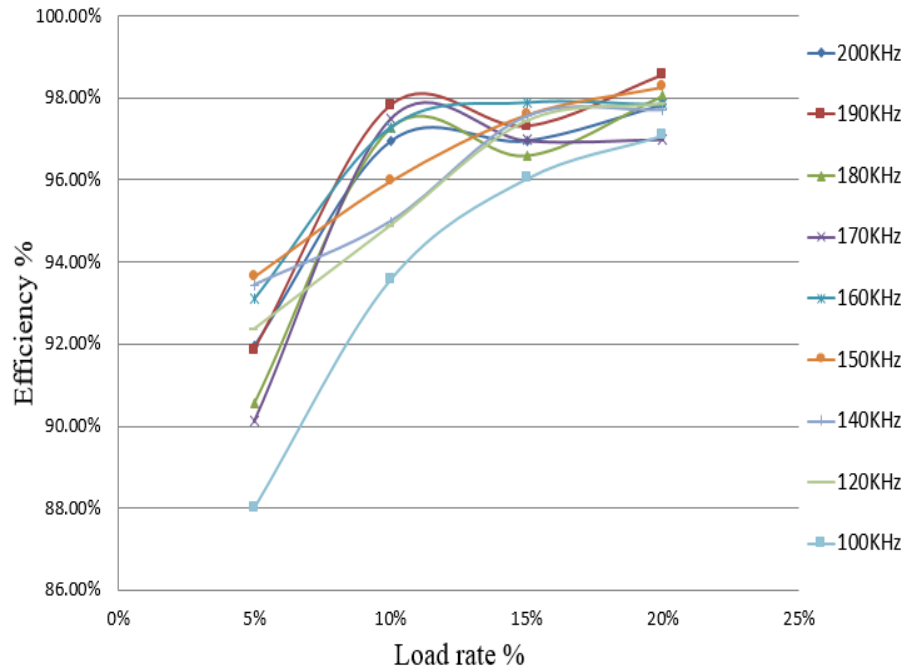
(b) Comparison of efficiency between 200kHz and optimum frequency.

# Experiment Results B:

## Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%

### Experiment environment

- AC input voltage  $V_{in}=100V$
- Link voltage (PFC output voltage) is fixed at **250V**



(a) Variation of efficiency according to frequency at 250V link voltage.

(b) Comparison of efficiency between 200kHz and optimum frequency.

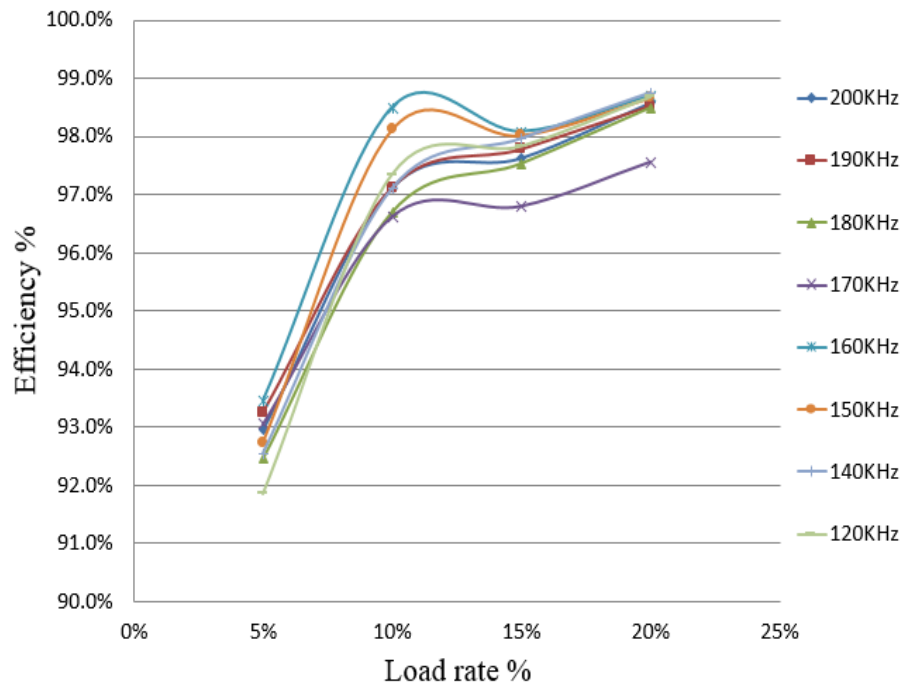


# Experiment Results B:

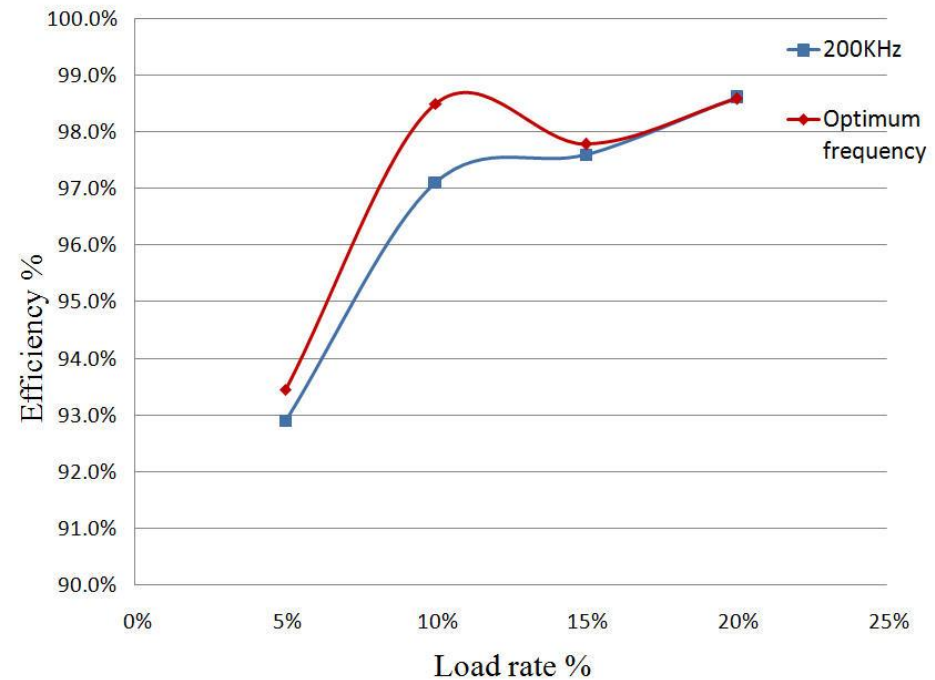
## Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%

### Experiment environment

- AC input voltage  $V_{in}=100V$
- Link voltage (PFC output voltage) is fixed at **200V**



(a) Variation of efficiency according to frequency at 200V link voltage.



(b) Comparison of efficiency between 200kHz and optimum frequency.

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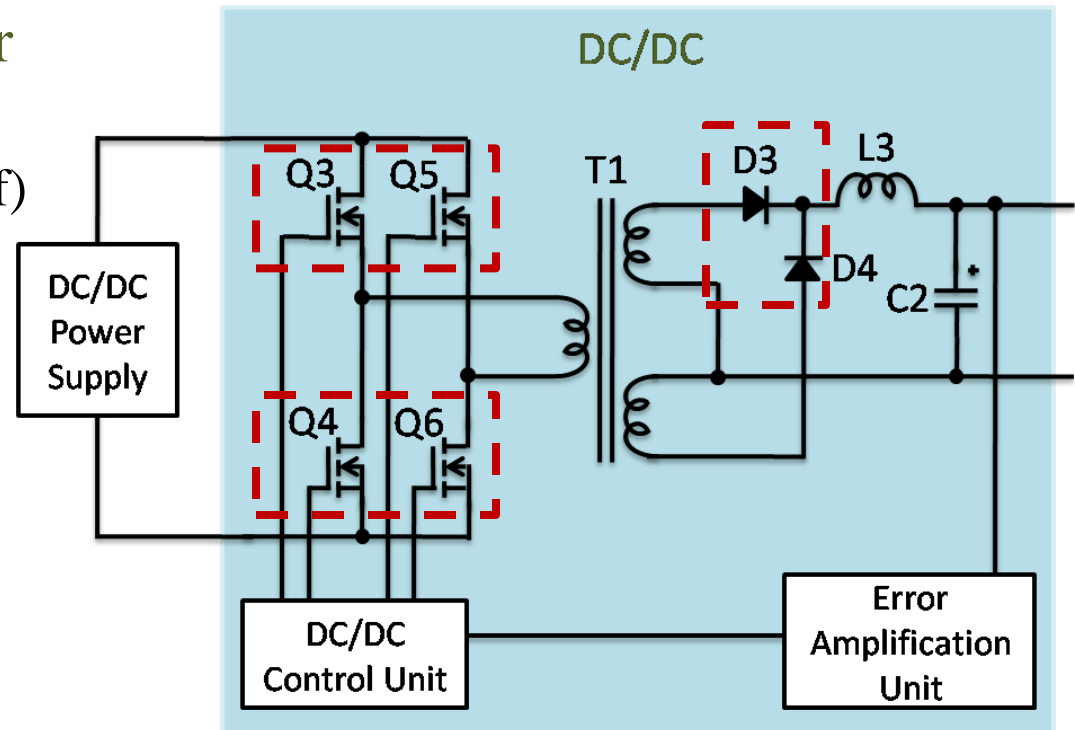
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# Analysis of PSFB DC/DC part

- Loss Mechanisms of Server Power Supply ②

(Diode loss & MOSFET loss  $\propto f$ )

- A variable PWM switching frequency using digital control can also benefit the efficiency of the PSFB DC/DC circuit.

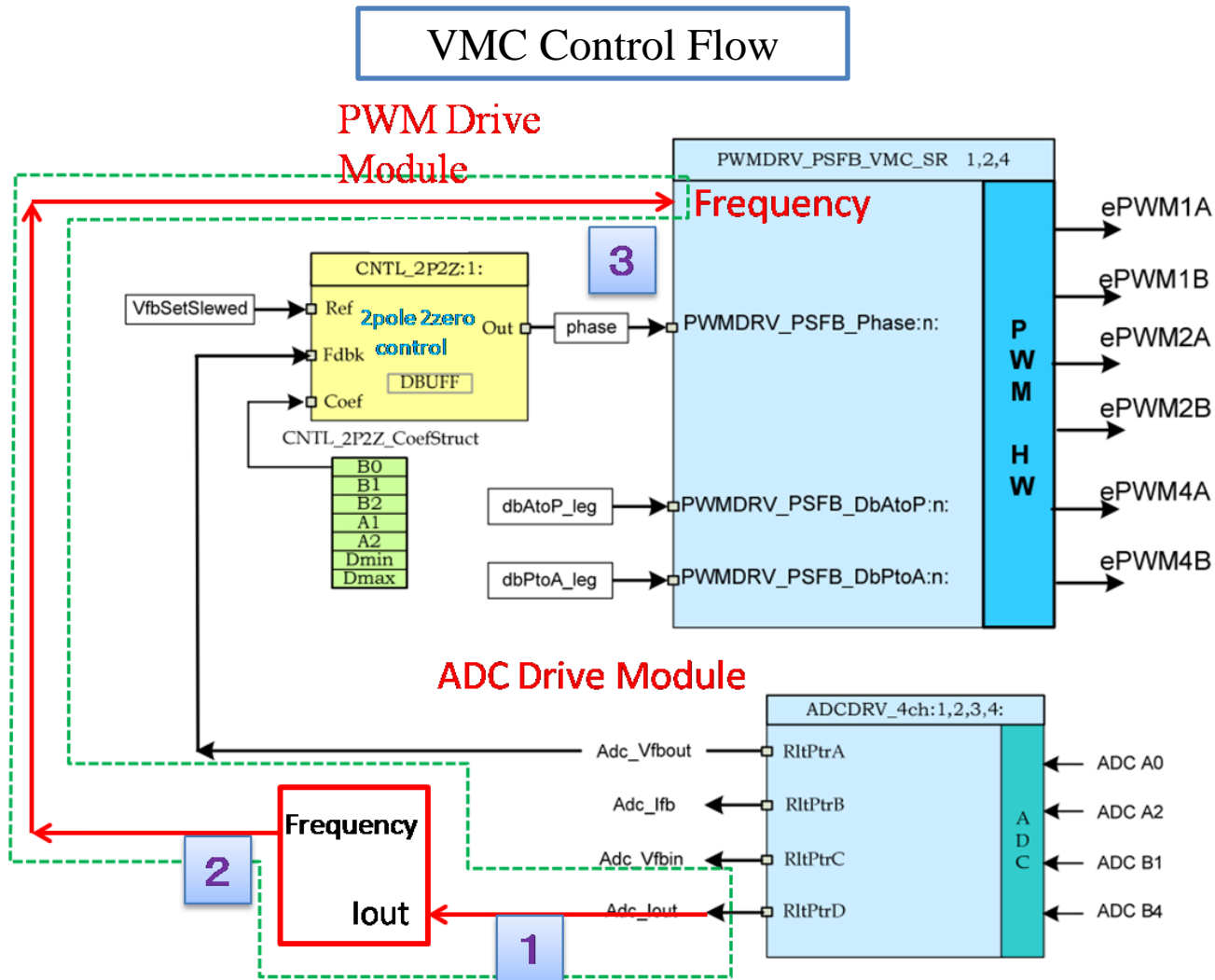


Light load + Fixed frequency

Light load + Variable frequency

Proposed

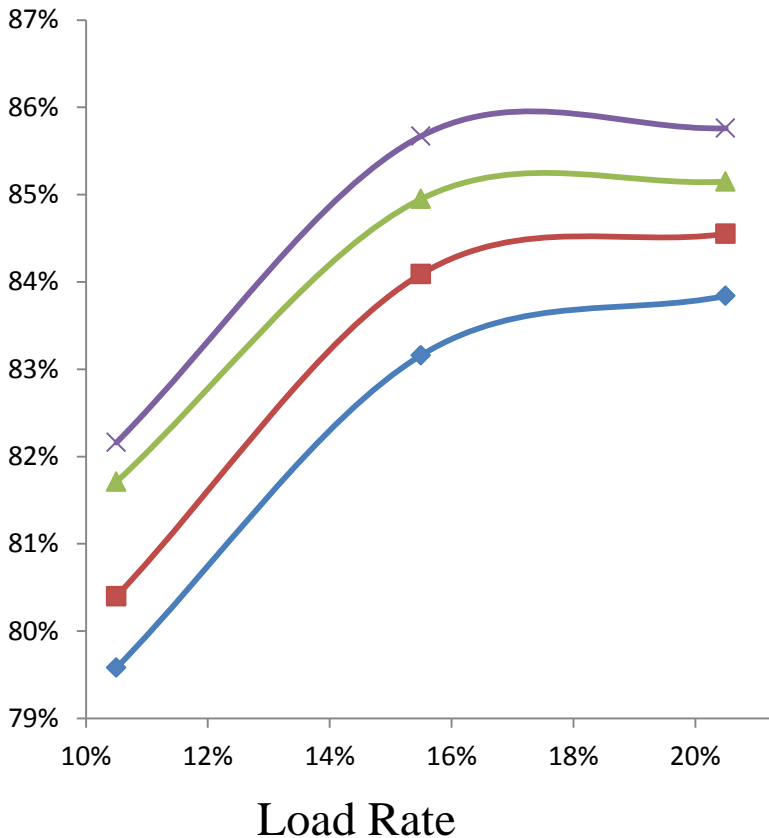
# Analysis of PSFB DC/DC part



The left **feedback part (red)** is added to the control unit by the proposed method.

# Experiment Results C:

## Optimization of PWM Frequency of PSFB DC/DC at a Load Rate of 5% to 20%



Conventional fixed frequency 200kHz is **not always efficient.**

- **Light load**: settled to a working frequency of 70kHz
- **50% load rate**: back to 100kHz

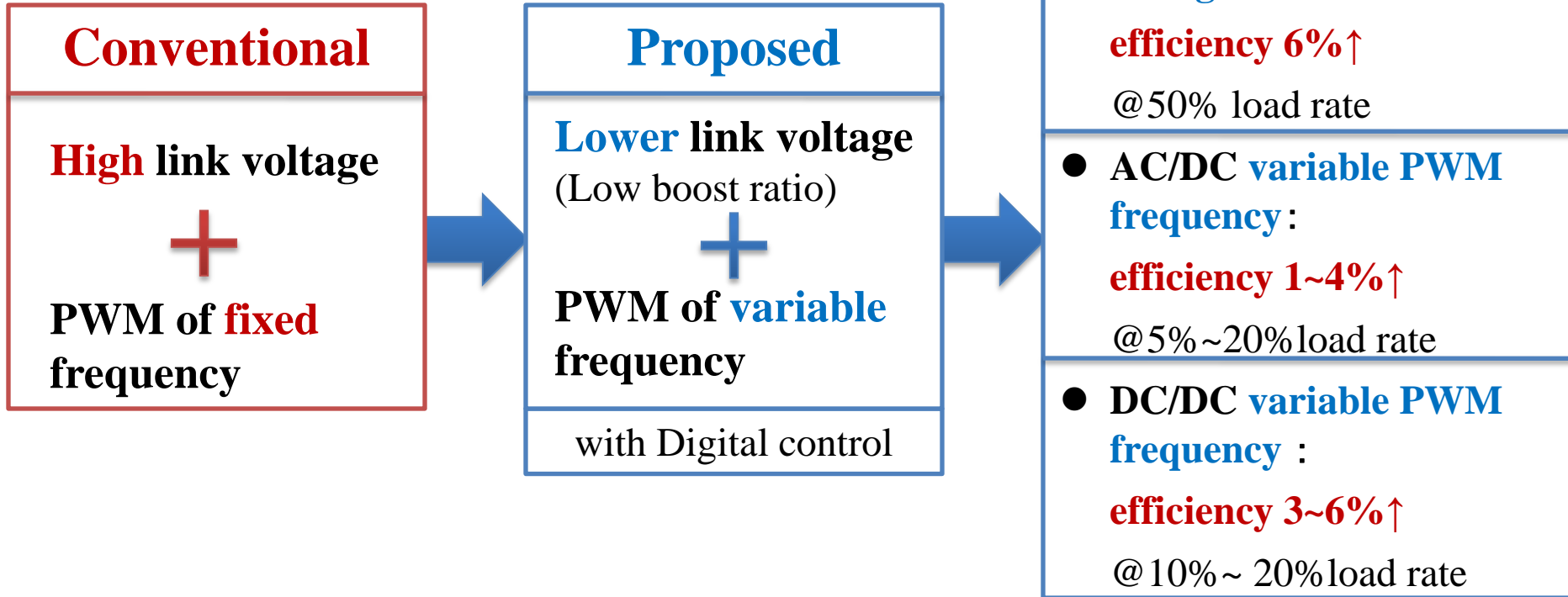
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# Conclusion

What we have done:



**Final goal:**

Server Power supply (PFC AC/DC+DC/DC)



% of Rated Load	10%	20%	50%	100%
TITANIUM	90%	94%	96%	91%

**Problem to be solved:**

The efficiency behavior and mechanism when combining the PFC AC/DC board and DC/DC board.

Thank you for your attention !

We would like to contribute  
to make the Earth green.



Kobayashi  
Laboratory



群馬大学  
GUNMA UNIVERSITY



# Question

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- Q: How much does efficiency increase?
- A: By lowering the link voltage from 400V to 200V if possible, there is a nearly 4% efficiency increase. And by adopting appropriate PWM switching frequency, efficiency increases by 1~2% of each part.