Efficiency Improvement for Switching Power Supply at Light Load Using DSP Control

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***Abstract*—This paper describes a digital control method for efficiency improvement of switching power circuit at light load with C2000 Series DSP (Texas Instruments Inc.). In this work, we use the DSP to adjust the link voltage between a bridgeless PFC AC/DC converter and a phase shift full bridge DC/DC converter, as well as control the PWM frequency of power circuit in order to improve the power efficiency in a suitable way. Our experiment results show that the efficiency of the power circuit at half load / light load improves with adjusting the link voltage and/or PWM frequency.**

Keywords—DSP, C2000, Power Circuit, Power Efficiency, Light Load, Digital Control.

I. INTRODUCTION

With a rising consideration toward "Green IT", it is becoming important to improve the energy efficiency of electrical systems especially the server power supply. Actually the power supplies rarely operate at a full load, and the 20%~30% loads show their necessity as the power supplies usually run at light load rate. In this paper we mainly attempt to improve the efficiency of power supplies at half-load and light load under 20% using digital control.

II. LOSS MECHANISMS OF PFC AC/DC CONVERTER AND DC/DC CONVERTER

In this section, we will discuss the features and loss mechanisms of the Power Factor Correction (PFC) AC/DC Circuit and DC/DC Converter Circuit which can help guide the approach to a better efficiency performance.

A. Power Factor Correction (PFC) AC/DC Circuit

The PFC circuit is used to improve the power factor to approach 1, and the reason for introducing the PFC circuit is the existence of high frequency radio regulation. Since the impedance of the capacitor to high frequency current is low, the risk of damage to power transmission and distribution appliances due to high frequency current would become evident. What the PFC circuit does is to lower as well as extend the current waveform, and the power factor is improved.

Despite the improvement of the power factor, the PFC circuit also brings some disadvantages such as a more complicated circuit and the degradation of conversion efficiency. First, we notice that the output voltage is higher than the input voltage through the boost chopper circuit topology. The input voltage of the conventional analog PFC is 85~265V, so the output voltage (link voltage) is 265*√2=390V. That is to say, despite of the possible range of input voltage, the output voltage is fixed at the peak value of 390V. This can be seen as one of the reasons to the deterioration of the efficiency of the light load. Secondly, the iron loss of the inductor, which is also called reactor loss, is also supposed to be seen a factor that influences the efficiency, which can be divided into hysteresis loss and eddy current loss. The hysteresis loss P_h is raised by the alternating magnetic field which can be represented by the Steinmetz formula. Here B_m is the maximum magnetic flux density, k'_h and k'_e are proportional constants, $e_L=V_o-V_i$ and f stands for the frequency.

$$P_h = k_h f B_m^{1.6} = k_h' \frac{e_L^{1.6}}{f^{0.6}}$$

The eddy current loss P_e is generated by the eddy current in the iron core.

$$P_e = k_e' \frac{(te_L)^2}{f^{0.6}}$$

As we can see, both the hysteresis loss P_h and the eddy current loss P_e is in proportion to e_L, thus the loss is related to the difference between the output voltage and input voltage.[1] The other factors for the loss lie in the other components in the PFC circuit such as diode loss and MOSFET loss (Fig.1), which will be discussed along with the loss analysis of DC /DC converter circuit below.

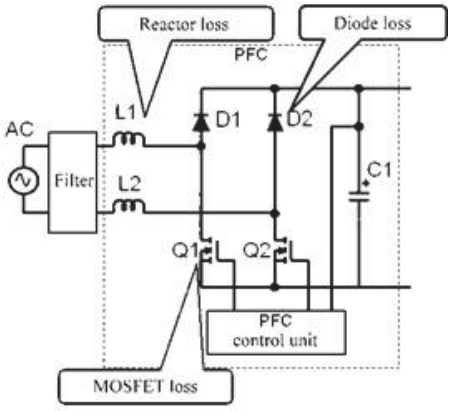


Fig. 1. Power losses at components in a PFC AD/DC circuit.

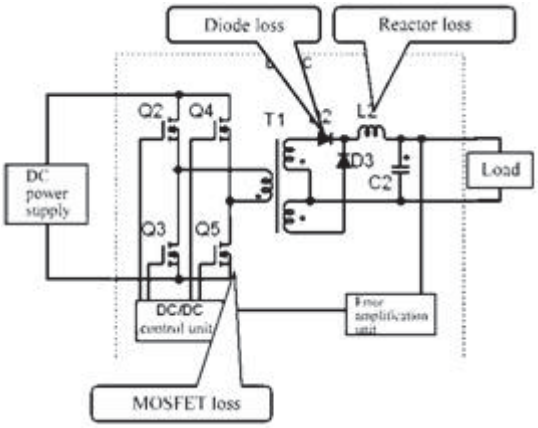


Fig. 2. The component loss in a DC/DC converter circuit.

B. DC/DC Converter Circuit

In many cases, the PFC circuit is followed by a DC/DC converter to achieve a desired DC output voltage. Chopper type buck converter utilizes the switching device to control the value of output voltage, which is also called PWM (pulse-width modulation).

The factors that degrade the efficiency of DC/DC converter circuit mainly include the loss due to the MOSFETs, diodes, inductors and capacitors in the circuit (Fig.2) which can be briefly shown as the following equations:

$$P_{SW(MOSFET)} = 0.5 \times V_D \times I_D \times (t_{SW(ON)} + t_{SW(OFF)}) \times f_s$$
$$P_{SW(DIODE)} = 0.5 \times V_{REVERSE} \times I_{RP(PEAK)} \times t_{RR2} \times f_s$$
$$P_{L(DCR)} = [\, I_{L(AVG)^2} + (I_P - I_Y)^2/12] \times DCR$$
$$P_{CAP(ESR)} = I_{CAP(RMS)^2} \times ESR$$

Here, $T_{SW(ON)}$ and $t_{SW(OFF)}$ are the transition time of the MOSFET. t_{RR2} is the reverse recovery time of the diode. I_P and I_Y are the peak and valley points of the inductor current waveform. DCR is defined by the division of the length and cross section area of the coil line. ESR is the equivalent series resistance of the condenser. [2]

In conclusion, the main reasons for the loss of the PFC AD/DC circuit and DC/DC converter circuit are the unnecessary high value of the link voltage and the components' loss in the circuits. As for the components loss, we will mainly discuss the MOSFET loss and capacitor loss since they directly connect with the switching frequency. It is difficult to realize the improvement of the circuit topology. Therefore, we will discuss the software approach of controlling the DSP to improve the efficiency performance.

III. Experimental Environment

In this section, we will give a brief introduction of the software development environment and two experiment boards that we use.

A. Development tools: CCS v5 (Code Composer Studio v5)

CCS v5 is an integrated development environment for embedded processor provided by TI (Texas Instruments) with the feature of low cost, wide range of products of small size, high speed and scalability. The main features of C2000 series DSP are shown below:

- 32bits DSP embedded with flash memory which fits digital DSP optimum power control.
- Supported by flexible and various power supply topology with high resolution (150psec) PWM output.
- High speed interrupt response and AD converter make fast control loop possible. [3]

B. Experiment Boards

The first board is a high voltage BLPFC (bridgeless PFC) kit (Fig. 3), which is controlled by the microcomputer of Piccolo series. The main features are shown below:

- Input Voltage (AC line): 85V(Min) to 265V(Max), 47~63Hz
- 400Vdc Output
- 300 Watts Output Power
- Full Load efficiency greater than 93%
- Power factor at 50% or greater load – 0.98(Min)
- PWM frequency 200kHz. [4]

It can be seen that the output voltage (link voltage) is fixed at the value of 400V.

The second board is a PSFB DC/DC kit (Fig. 4), which is under the control of a TMS320F28027 DSP. The main features are shown below:

- 400V DC input (370Vdc to 410Vdc operation), 12V DC output
- Peak efficiency greater than 95%
- 50A (600Watt) rated output.
- Phase Shifted Full Bridge Circuit topology
- 100kHz switching frequency. [5]

It can be seen that the PWM frequency is fixed at the value of 100kHz.

IV. Experiment Results

The experiment is conducted in three steps. In step 1, we monitor and adjust the link voltage the in order to improve the efficiency of the PFC AC/DC circuit. In step 2, we monitor and adjust the PWM frequency in order to improve the efficiency of PFC AC/DC circuit. In step 3, we monitor and adjust the PWM frequency in order to improve the efficiency of the DC/DC circuit.


Fig. 3. BLPFC AC/DC circuit (Bridgeless Power Factor Correction AC/DC).

Fig. 4. PSFB DC/DC circuit (Phase Shift Full Bridge DC/DC).

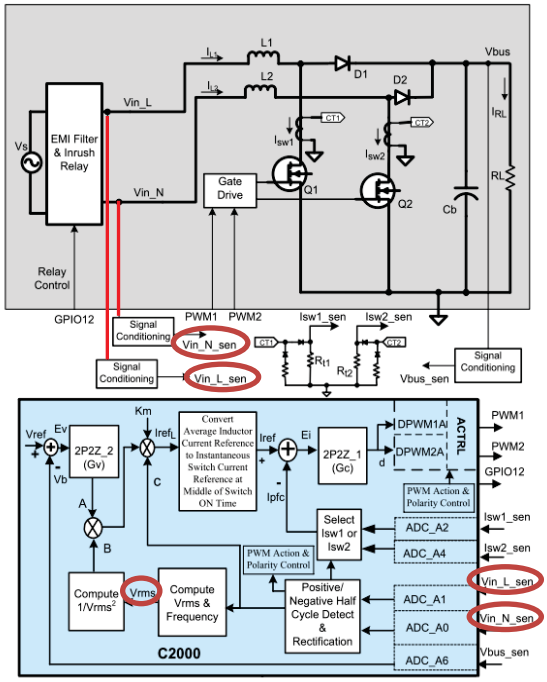


Fig. 5. BLPFC converter control using C2000 micro-controller.

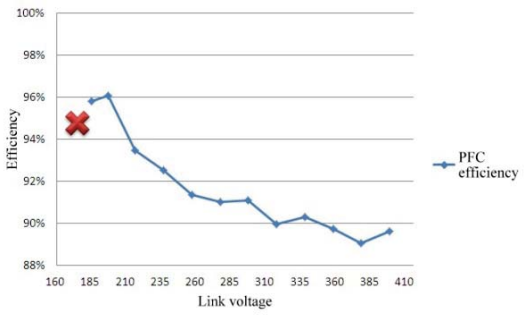


Fig. 6. Efficiency of PFC board according to link voltage at half-load.

A. Link Voltage Optimization of BLPFC AC/DC at a Half-Load

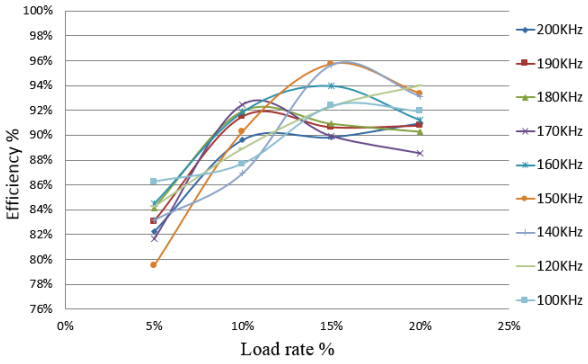
As the efficiency degradation is caused by the link voltage, the solution is to reduce the link voltage. As the signal flow diagram is shown in Fig. 5, first the input voltage (Vin_L_Sen and Vin_N_Sen) is detected. Then the two input voltages are converted into digital signals by the AD converters (ADC_A1 and ADC_A0) and passed into the DSP. Finally the DSP calculates the value of Vrms and induces the link voltage by multiplying with the optimum boost ratio.

$$\text{Link Voltage} = \text{Optimum Boost Ratio} * \text{Vrms}$$

The experiment results (Fig.5) confirmed the supposition that by lowering the link voltage instead of fixed 400V output link voltage, efficiency can be improved. However, problems come out when the link voltage is reaching under 190V (Fig.6). As described above, as for an input voltage of 100V, the output of PFC circuit must be larger than the maximum value of the input $100\sqrt{2}$. In other words, the link voltage should be more than 142V. While as the link voltage is set to below 190V, we find that the output voltage becomes unstable, and noise becomes unable to be ignored. Therefore we set the optimal boost ratio to 2, and thus the optimal link voltage is 200V corresponding to 100V input voltage.

B. Optimization of PWM Frequency of BLPFC AC/DC at a Load Rate of 5% to 20%

In the case of light load, the power supply circuit of a fixed frequency of PWM control suffers from a degraded efficiency. Therefore, a variable PWM switching frequency by digital control has been tested. The experimental results are shown in the following (Fig.7~Fig.11).



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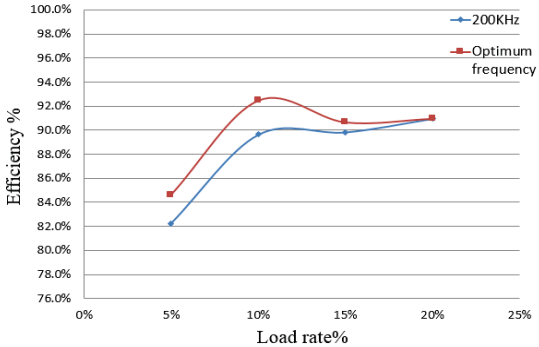

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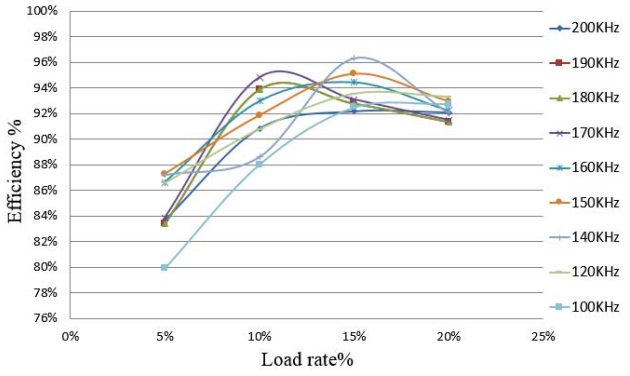
Fig. 7. (a) Variation of efficiency according to frequency at 400V link voltage. (b) Comparison of efficiency between 200kHz and optimum frequency.



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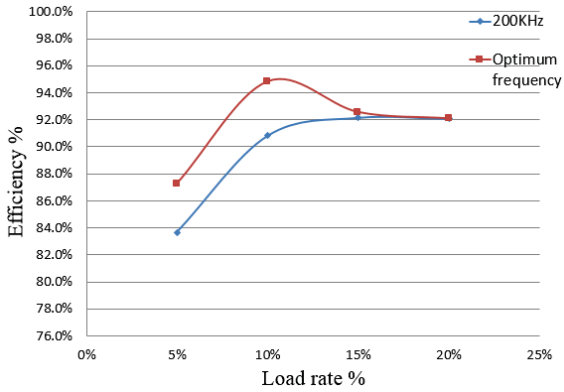

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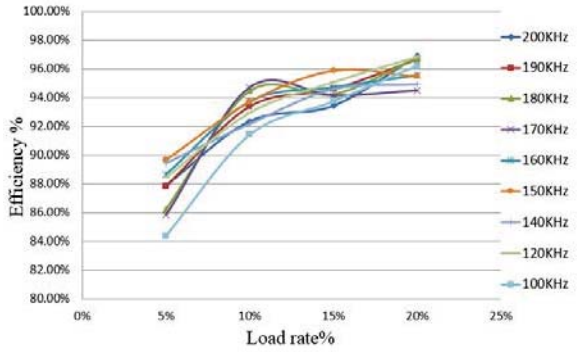
Fig. 8. (a) Variation of efficiency according to frequency at 350V link voltage. (b) Comparison of efficiency between 200kHz and optimum frequency.



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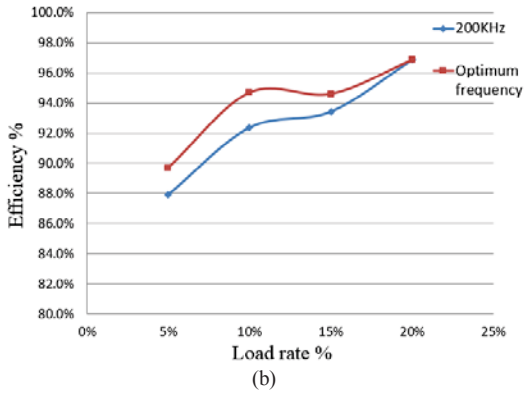

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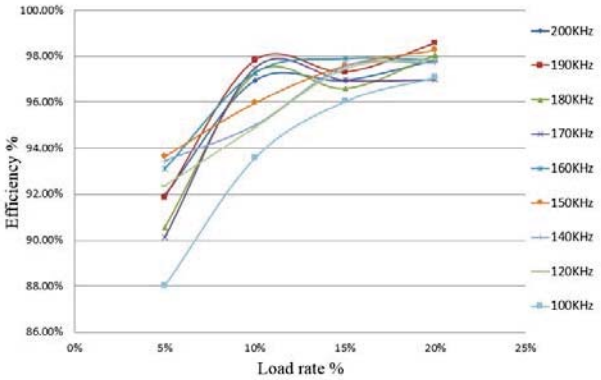
Fig. 9. (a) Variation of efficiency according to frequency at 300V link voltage. (b) Comparison of efficiency between 200kHz and optimum frequency.



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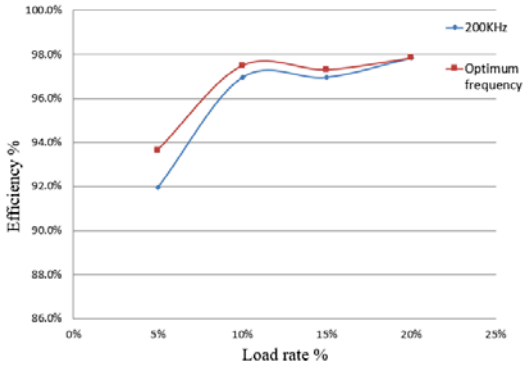
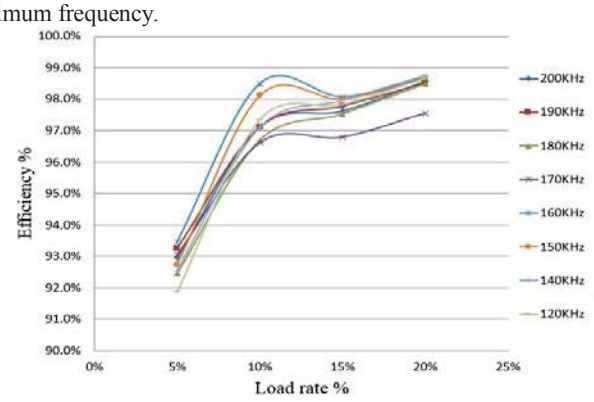


(b)

Fig. 10. (a) Variation of efficiency according to frequency at 250V link voltage. (b) Comparison of efficiency between 200kHz and optimum frequency.



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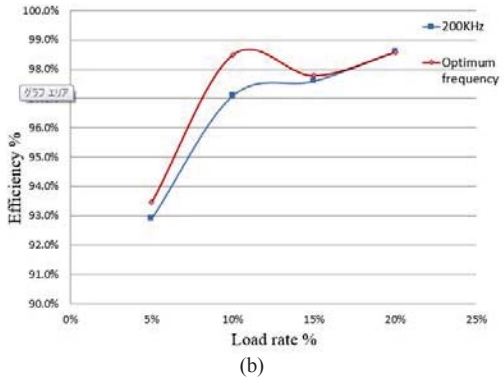


(b)

Fig. 11. (a) Variation of efficiency according to frequency at 200V link voltage. (b) Comparison of efficiency between 200kHz and optimum frequency.

TABLE I. OPTIMUM PWM FREQUENCY ACCORDING TO LOAD RATE

Load Rate (%)	PWM Frequency (kHz)
5% - 10%	150kHz
10% - 15%	170kHz
15% - 20%	190kHz
20%～	200kHz

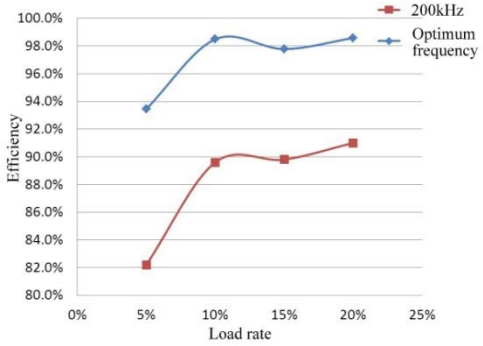


Fig. 12. Comparison of the efficiency of the conventional method (fixed 400V link voltage and 200kHz PWM frequency) and the proposed method (variable link voltage and optimum frequency).

Our experiments are implemented by changing the PWM frequency from 100kHz to 200 kHz with a step of 10kHz at the link voltage from 400V down to 200V. The current waveform degrades when the PMW frequency is set below 100kHz. Therefore, we examined the PWM frequency with the minimum value of 100kHz. The chosen optimum frequency which covering the light load range is shown in TABLE I. Fig.12 is the result of the combined efficiency improvement of two optimal control methods of link voltage and PWM frequency. A notable improvement of efficiency can be recognized at low load.

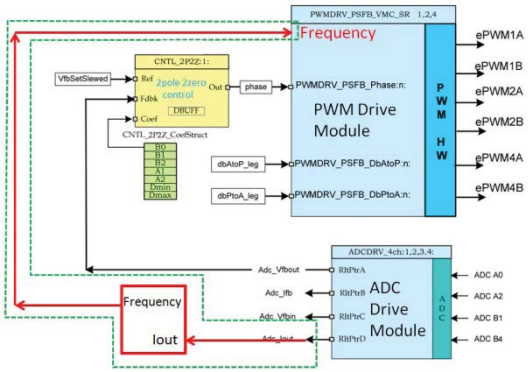
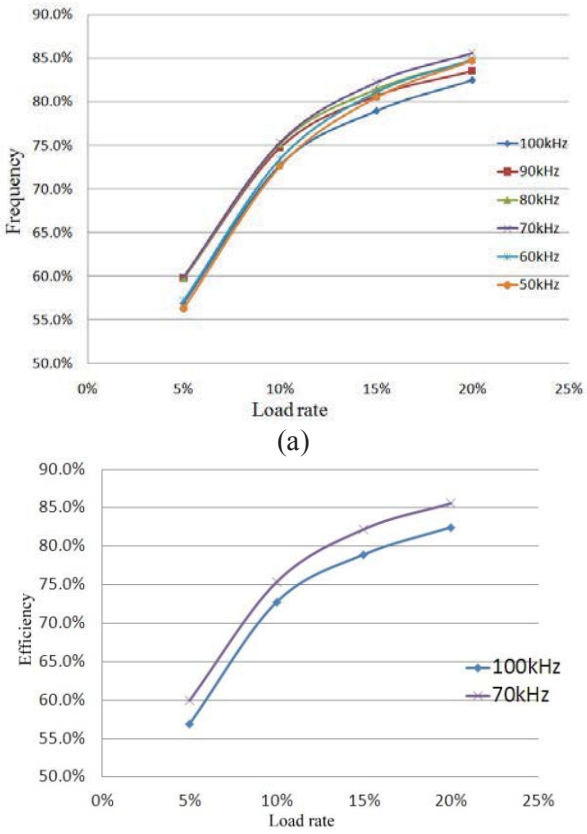


Fig. 13. Control flow of PWM frequency.



(a)

(b)

Fig. 14. (a) Variation of efficiency according to PWM frequency at light load with a input voltage of 400V. (b) Comparison of PWM efficiency between 100kHz and optimum frequency of 70kHz.

C. Optimization of PWM Frequency of PSFB DC/DC at a Load Rate of 5% to 20%

In the same manner as described in the previous section, we tested how a variable PWM switching frequency using digital control can benefit the efficiency of the PSFB DC/DC circuit.

The left feedback part (red) is added to the control unit by the proposed method (Fig.13). As the output voltage of the DC/DC board is fixed at 12V, the PWM frequency is controlled according to the output current.[6]

As defined in the board specification, the conventional switching frequency is 100 kHz. In the case of light load shown in Fig.14, 70kHz switching frequency shows a more satisfactory efficiency than 100kHz does.

V. CONCLUTION

In this paper, we have examined how the TI C2000 DSP series can be used to improve the efficiency of power supply circuit with a light load. As the power supply circuit with digital controller like DSP or CPU is becoming the mainstream. DSP digital control begins to show its merits.

It is possible to change the link voltage and PWM frequency without altering the hardware topology of the power supply circuit. Moreover, the link voltage and PWM frequency have been set into function modules which can be

added to the system. These make the modification can be applied in a much easier way, and we have shown experimentally that the digital control of the link voltage and the PWM frequency improves the efficiency at light load.

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