Single Inductor Dual Output Buck Converter with Rippled-Based Serial Control

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Abstract: This paper describes a new control method for the "Single Inductor Dual Output Converter" which is called Serial Control Method. And this time we choose buck converter as a sample. This control methods use a unique Priority Switch to judge the order of converters' work. We divide the inductor's charge current and discharge current to supplies the power to different converters. Finally we will show the results of simulation with the output voltage ripples and the dynamic load regulations.

Keywords: DC-DC Converter, Buck Converter, Single Inductor Dual Output, Ripple-Based, Serial Control.

I.INTRODUCTION

DC-DC converters are indispensable for virtually all-electronic devices, from cell phones to large manufacturing machinery. In many applications, multiple output voltages are required.

In a conventional system, the DC-DC converter needs a single inductor for each output; hence many inductors are needed in the system as a whole. In order to reduce cost and volume of the system, it is desirable to reduce the number of required inductors. So we have reported single inductor dual output (SIDO) DC-DC converters [1]~[4]. Now we have developed the SIDO converter with ripple-based serial control.

Ⅱ.SINGLE INDUCTOR DUAL OUTPUT CONVERTERS WITH EXCLUSIVE CONTROL METHOD

As shown in figure 1, the converter with an exclusive control method is a very simple method with a few additional components, a comparator and a selector. In this SIDO converter, the comparator makes the select signal SEL by comparing two amplified error voltages in order to select one of the converters shown in figure 2. Two converters are selected with controlling the switch S2 in the converter 2. When S2 is ON, the converter 2 is selected because the diode D1 is cut off (V1 > V2). The amplified error voltages are selected with the SEL signal to make the PWM signal shown in figure 2, which controls the main switch SW0.

In this exclusive control method, only one converter is selected exclusively to be supplied the current from the inductor controlled by the SEL signal, which is determined at the timing of the clock for the saw tooth signal generator. So control timing is not continuous, sometimes waiting for several periods when the load current of other converter is changed large. The control speed for each converter is a little bit delayed and the characteristics of the dynamic load regulations are not the best condition.

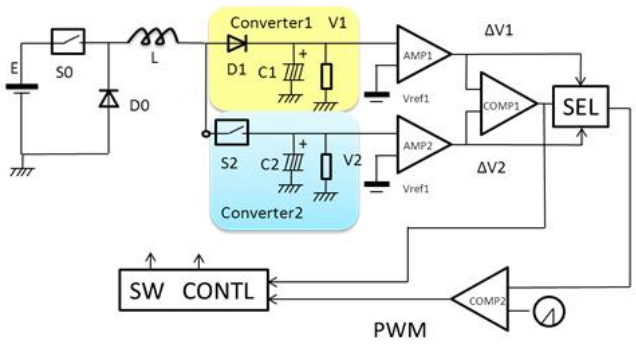

Figure 1. Circuit of exclusive control method

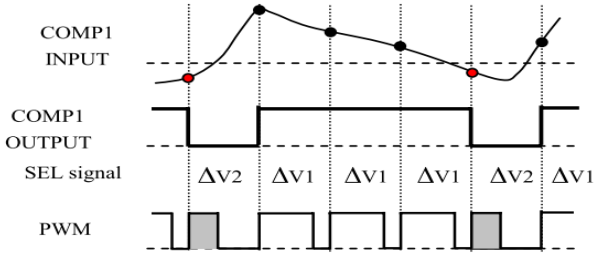

Figure 2. Wave of SEL and Comparator

Ⅲ.SIDO CONVERTER WITH SERIAL CONTRAL

As shown in figure 3, SIDO converter has two sub-converters, which are controlled by the SW1 and SW2.Every period the system chooses one converter and just supplies power to it from the inductor exclusively. This main power stage is the buck converter, which consists of the main switch SW0, the diode and the inductor, where the serial resistor is the equivalent serial resistor ESR of the inductor. The two converters and the comparator for generating the select signal SEL is the same as that of figure 1. In this system, each converter generates the PWM signal, which is selected by SEL signal.

The main switch SW0 is controlled by the selected PWM signal and each switch of the sub-converter is exclusively controlled by the priority control circuit in order to supplies current from the inductor. For example, when the SEL signal is "H", that is the error voltage ⊿V1 is larger than ⊿V2, the switch 1 (SW1) is selected first and the switch2(SW2) is selected later then power source supplies the current to the converter 1 first. In this case, for the "H" period of the PWM signal, the SW1 is ON. Next, for the "L" period after "H" period, the SW1 turns OFF and the SW2 is ON in order to supply the current from the converter 1 to the converter 2.

In this case, the converter 2 is not always need for a full "L" period of the PWM signal. So when the amplified error voltage ⊿V2 goes to higher than the reference voltage, the priority control circuit turns both SW1 and SW2 to OFF. Here, the diode across the SW0 and the inductor works in order to regenerate the current of the inductor back to the voltage source.

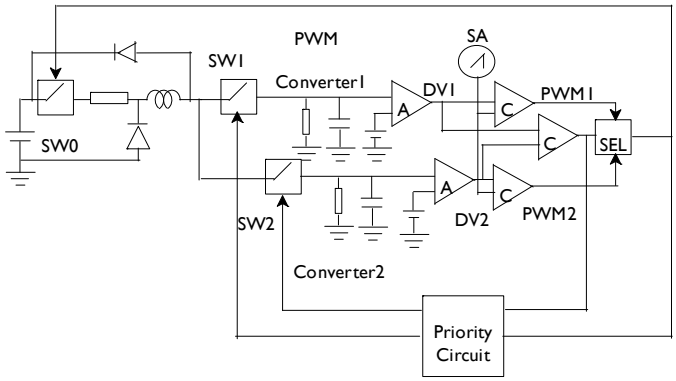

Figure 3. Block graph of SIDO converter

Ⅳ.PRIORITY CONTROL CIRCUIT

Figure 4shows the circuit of the priority control circuit. It has two SR Flip-Flops (without clock signal type) and some logic gates. The PWM signal is supplied to S inputs of two SR Flip-Flops and their R inputs are connected to the output of each comparator, which compares between each error voltage of each converter and the reference voltage (that is 3 V). The output of each flip-flop is connected to each 2-input AND gate G1 and G2, the other input of AND gate which is connected to the selected PWM signal supplied from the PWM selector.

When the PWM signal turns to "H", two SR Flip-Flops turn their outputs (Q)"H" and keep them "H". When error voltage (DV1 or DV2) becomes higher than 3V, the output of the comparator turns "H" and the flip-flop is reset to make its output "L". Then the And-Gate turns "L" to control the switch (SW1 or SW2) OFF.

In this system, the error voltage of each converter is lower than the reference voltage when circuit start to work. So the outputs of both SR Flip-Flops keep the outputs "H", when the PWM signal turns "H". In this timing, PWM selector supplies the PWM signal from the converter which is selected and the And-Gate connect with "H" input is selected and makes the switch ON.

For example, when the SEL signal is "H", G1 outputs the PWM signal and SW1 is selected to supply current in order to make the output voltage DV1 higher. When the DV1 becomes higher than the reference voltage among "H" period of the PWM signal, the FF1 is reset to make its output "L". Then the gate G1 turns "L" and makes the SW1 OFF.

After the PWM signal turns "L", the output of the PWM selector turns "L". Then the output of the gate G1 turns "L" and the SW1 is OFF and the output of the gate G2 turns "H" and the SW2 is selected to supply current to the converter 2. When the DV2 becomes higher than the reference voltage, the SW2 becomes OFF. After SW1 and SW2 both turn OFF, they'll keep OFF till the PWM signal turns "H" to set both flip-flops. When both switches are OFF, current of the inductor flows to the voltage source through the diode as the regenerated current.

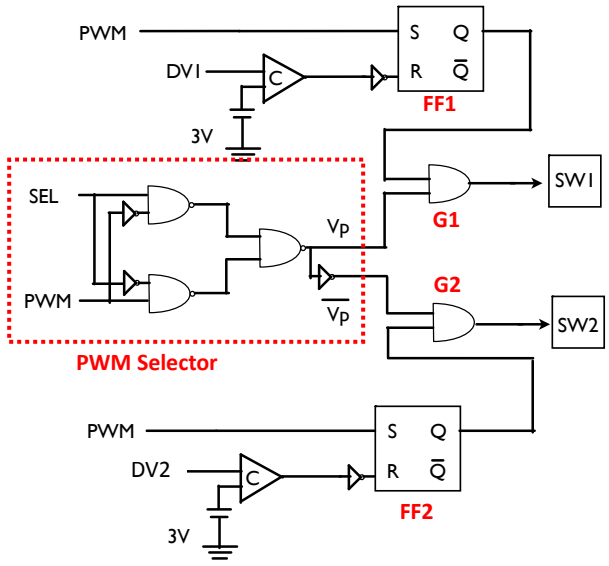

Figure 4. Circuit of Priority Switch

Ⅴ.WAVEFORM

Figure 5shows the waveform of SIDO buck converter and figure 6shows the directions of inductor current. The SEL signal is set at the start timing of the PWM signal to be kept for a period. In next period, comparing two output voltages catches new select signal.

In figure 5, atT1＜t＜T2, error voltage DV1 is bigger than DV2,so the SEL signal is “H” and the PWM1 signal is selected to control the main switch SW0. In this case, the SW1 works same as SW0 and current of the inductor increases and supplies to the converter1.

AtT2＜t＜T3,the PWM signal turns “L” and the SW2 is selected to be turn ON. Current of the inductor decreases to discharge energy to supplies its current to the converter 2.

At T3＜t＜T4,the error voltage of the converter 2becomes higher than the reference voltage 3V and the SW2 turns OFF. Then current of the inductor flows back to the power source through the diode.

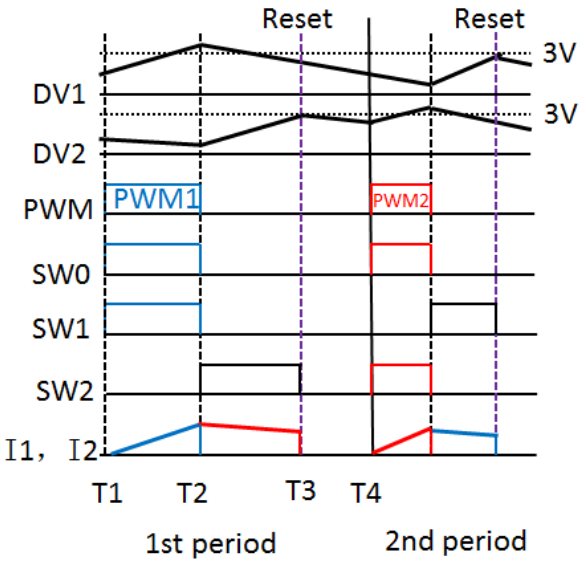

Figure 5. Waveform of circuit

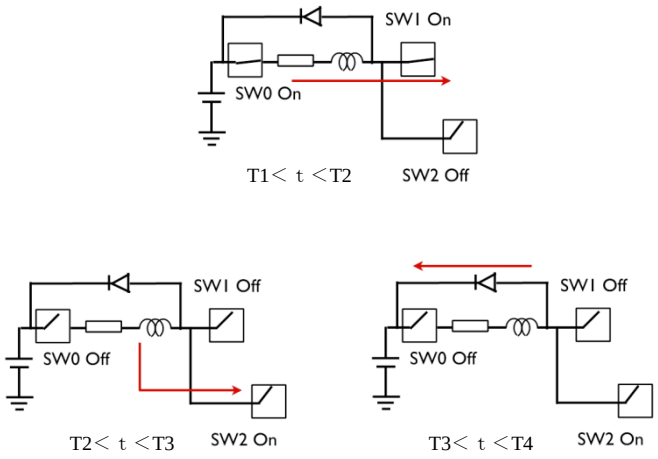

Figure 6. Direction of inductor current

Ⅴ.SIMULATION RESULTS

Table 1 shows the parameters of the simulation circuit of tha SIDO converter with ripple-based control. Figure 7 shows the inductor current and supplied current to each sub-converter, which is dicribed togather with blue lines for the converter1and red lines for the converter2. Figure 8 separately shows each current to the onverter with the SEL signal. In this figure, two currents of I1 and I2 appear alternately and serially in a period and the order in a period of the SEL signal is changed. For example when the SEL signal is “H”, current I1 appears first and next shows current I2. When the SEL signal is “L”, the order of each current is inverse.

Table 1 Parameters of circuit

Vi	10 V
V1	5.0 V
V2	4.5 V
Io	0.5 A
L	1uH
C	470uF
F	500KHz

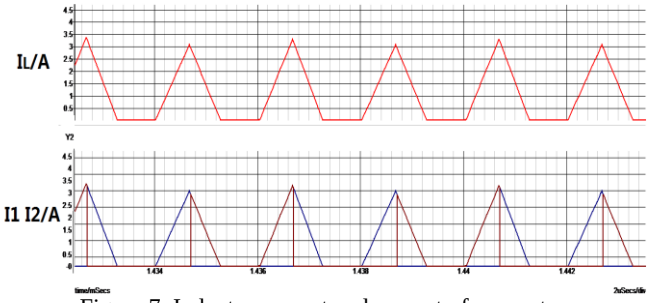

Figure 7. Inductor current and current of converters

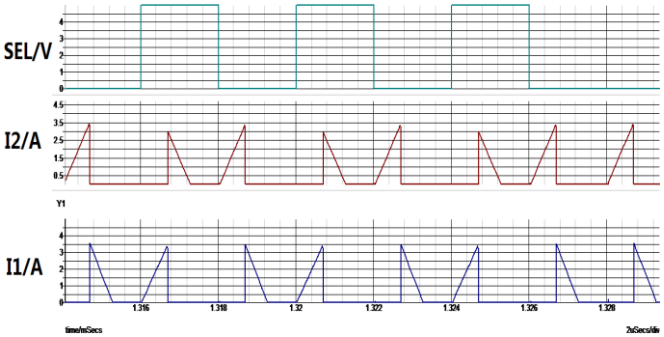

Figure 8. SEL signal and current of converters

Figure 9 and Figure 10 show the current wave of sub-converterswhen the load current of one converter increases from o.5A to 1.oA. Figure 9 shows current waves when I1 increases and Figure 10 shows current waves when I2 increases.

As shown in figure 9, current I1 first flows and the peak current becomes high of 4A, but current I2 flows for a while and suddenly

stops on the way of the period. It means that large current flows to the converter 2 and its voltage becomes higher than the reference voltage 4.5V, so the flip-flop 2 in figure 4 turns its output to "L" and the switch SW2 turns OFF.

On the other hand, shown in figure 10, when current of the converter 2 changes large, current I1 first increases and its peak is about 4A, then next flows current I2. The flow of current I2 suddenly stops like I1 in Figure 9.

Figure 11 shows the output voltage ripples and the dynamic load regulations of both converters when the load current changes from 0.5A to 1.oA or vice versa. The static ripples of both converters are less than 5mVpp at Io=0.5A or Io=1.0A. The overshoots or under shoots of the dynamic regulation of both conberters are little bit large. The cross regulations of both converters are less than ±5mV, but the self regulations of both converters are abut ±10mV.

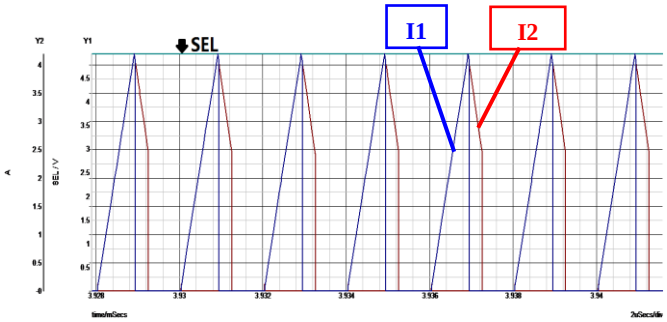

Figure 9. Current wave of converters when I1 increase

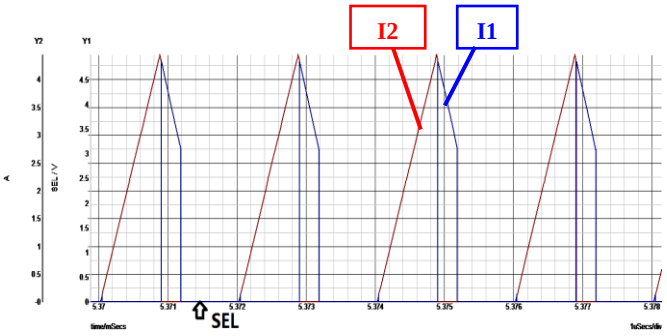

Figure 10. Current wave of converters when I2 increase

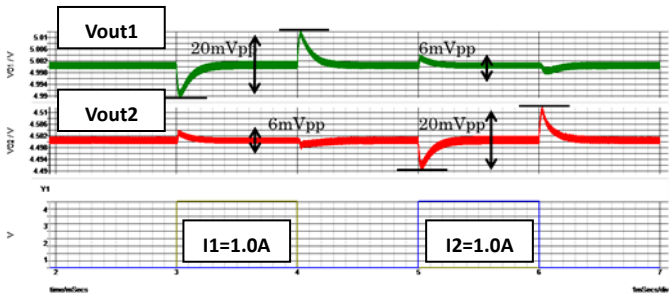

Figure11. Output ripples and dynamic load regulations

Ⅵ.CONCLUSION

In this paper we have discribed new single inductor dual output SIDO DC-DC buck converter with ripple-based serial control. We have serially controlled both sub-converters in a period. With the priority control circuit, this converter provies the inductor current first to the converter the error voltage of which is larger than other converter.

As the simulation results, the output ripples of both converters are less than 5mVpp at Io=1.0A. About the dynamic load regulations of both converters at the load current step of from 0.5A to 1.0A or vice versa, the cross regulations are less than ±5mV and the self regulations are about ±10mV.

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