Time-to-Digital Converter Architecture with Residue Arithmetic and its FPGA Implementation

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Abstract

This paper describes a time-to-digital converter (TDC) architecuture with residue arithmetic or Chinese Remainder theorem. It can reduce the hardware and power significantly compared to a flash type TDC while keeping comparable performance. Its FPGA implementation and measurement resuts show the effectiveness of our proposed architecture.

Keywords- Timing Measurement, Time to Digital Converter, Residue, Chinese Remainder Theorem, FPGA

Introduction

A Time-to-Digital-Converter (TDC) measures the time interval between two edges, and time resolution of several picoseconds can be achieved when the TDC is implemented with an advanced CMOS process. TDC applications include phase comparators of all-digital PLLs, sensor interface circuits, modulation circuits, demodulation circuits, as well as TDC-based ADCs. The TDC will play an increasingly important role in the nano-CMOS era, because it is well suited to implementation with fine digital CMOS processes. [1,2,3].

There are various kinds of TDC circuits, and here we focus on a flash-typeTDC (Fig.1) [1]. It uses a delay line which consists of CMOS inverter buffer delays. Baesd on this flash-type TDC, we will introduce a new type TDC---Residue Arithmetic TDC to reduce the hardware and power significantly compared to a flash-type TDC while keeping comparable performance.Then we have implemtened it on an FPGA to verify the operation and performance.

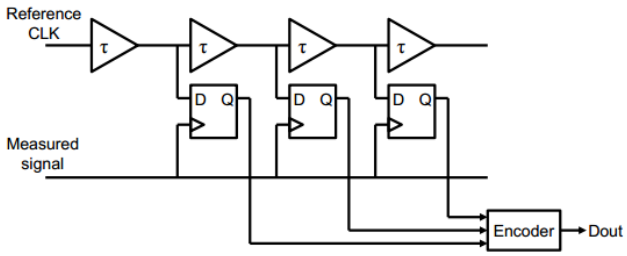

Fig 1. Flash-type TDC

Residue Arithmetic

Suppose that m1,…,mr are positive integers and coprime each other. Then there is unique positive interger x for given integers (a1,…,ar) which satisfy the following:

$$x \equiv a_k \pmod{m_k}, \quad k = 1, 2, \ldots, r$$

where $0 \leqq a_k < m_k$, $0 \leqq x < N$ ($N = m_1 \cdot m_2 \cdots m_r$). Table I shows the case of m1= 2, m2= 3, m3 = 5 and N=2 x 3 x 5=30, and we see that each k is mapped to residues of (m1, m2, m3) one to one [3,4].

Table I. An integer k and residues of (m1, m2, m3)

m1	m2	m3	k	m1	m2	m3	k
0	0	0	0	1	0	0	15
1	1	1	1	0	1	1	16
0	2	2	2	1	2	2	17
1	0	3	3	0	0	3	18
0	1	4	4	1	1	4	19
1	2	0	5	0	2	0	20
0	0	1	6	1	0	1	21
1	1	2	7	0	1	2	22
0	2	3	8	1	2	3	23
1	0	4	9	0	0	4	24
0	1	0	10	1	1	0	25
1	2	1	11	0	2	1	26
0	0	2	12	1	0	2	27
1	1	3	13	0	1	3	28
0	2	4	14	1	2	4	29

Residue Arithmetic TDC Architecture

We consider to use this residue arithmetic for TDC implementation, because obtaining the residue is relatively easy for time signal (used in TDC design) while it is difficult for voltage signal. (used in ADC design). Fig.2 shows the proposed residue arithmetic TDC in the case of m1= 2, m2= 3, m3 = 5 and N=2 x 3 x 5=30, where the residues a (mod 2), b

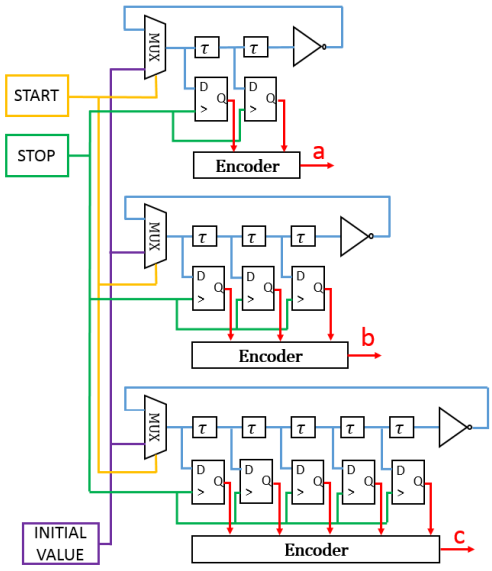

Fig2. Proposed residue arithmetic TDC architecture.

(mod 3), c (mod 5) are obtained with ring oscillators.

Note that the proposed TDC uses only 10 delay cells and 10 flip-flops (because 2+3+5=10) while the corresponding flash TDC requires 30 delay cells and 30 flip-flops; in general, the proposed TDC uses M delay cells and M flip-flops (where M=m1+m2+···+mr) while the corresponding flash-type TDC uses N delay cells and N flip-flops (where N = m1·m2···mr), and hence the circuit and power reduction of the proposed TDC can be significant for a large N with proper choice for M<<N compared to the flash TDC.

FPGA Implementation

We have implemented our proposed TDC with an FPGA (Fig.3) [5, 6, 7], and Table II and Fig.4 show its measurement results. We see that the proposed TDC works with good linearity as expected.

Conclusion

This paper describes residue arithmetic TDC and its FPGA implementation, and the measurement results verify its operation principle.

Acknowledgements

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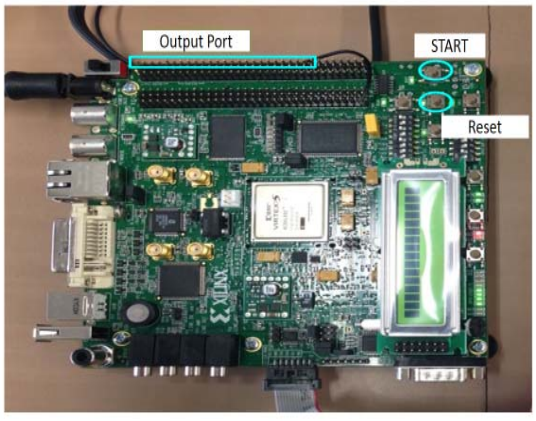

Fig.3 Proposed TDC implementation on FPGA.

Table II Measurement results of the proposed TDC.

Sample in Window	Elapsed Time (ns)	a	b[0]	b[1]	c[0]	c[1]	c[2]	k
0	0.00	0	0	0	0	0	0	0
3	30.30	1	1	0	1	0	0	1
6	60.60	0	0	1	0	1	0	2
9	90.90	1	0	0	1	1	0	3
12	121.20	0	1	0	0	0	1	4
15	151.50	1	0	1	0	0	0	5
18	181.80	0	0	0	1	0	0	6
21	212.10	1	1	0	0	1	0	7
24	242.40	0	0	1	1	1	0	8
27	272.70	1	0	0	0	0	1	9
30	303.00	0	1	0	0	0	0	10
33	333.30	1	0	1	1	0	0	11
36	363.60	0	0	0	0	1	0	12
39	393.90	1	1	0	1	1	0	13
42	424.20	0	0	1	0	0	1	14
45	454.50	1	0	0	0	0	0	15
48	484.80	0	1	0	1	0	0	16
51	515.10	1	0	1	0	1	0	17
54	545.40	0	0	0	1	1	0	18
57	575.70	1	1	0	0	0	1	19
60	606.00	0	0	1	0	0	0	20
63	636.30	1	0	0	1	0	0	21
66	666.60	0	1	0	0	1	0	22
69	696.90	1	0	1	1	1	0	23
72	727.20	0	0	0	0	0	1	24
75	757.50	1	1	0	0	0	0	25
78	787.80	0	0	1	1	0	0	26
81	818.10	1	0	0	0	1	0	27
84	848.40	0	1	0	1	1	0	28
87	878.70	1	0	1	0	0	1	29

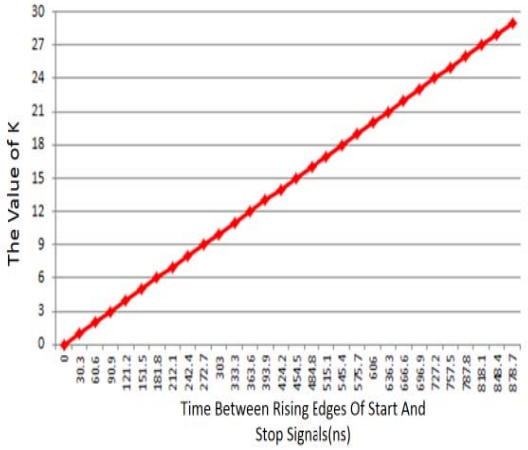

Fig.4 Measurement results of the proposed TDC.